

Features

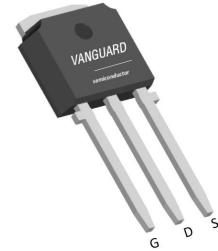
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- Fast Switching and High efficiency
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant



Part ID	Package Type	Marking	Tape and reel information
VS4080AI	QIPAK	4080AI	75pcs/Tube

V_{DS}	40	V
$R_{DS(on),TYP}@ V_{GS}=10\text{ V}$	5	m Ω
$R_{DS(on),TYP}@ V_{GS}=4.5\text{ V}$	6	m Ω
I_D	80	A

QIPAK



Drain Pin 2



Source Pin 3

Maximum ratings, at $T_A=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	40	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_C=25^\circ\text{C}$	80 A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$	$T_C=25^\circ\text{C}$	80 A
		$T_C=100^\circ\text{C}$	56 A
I_{DM}	Pulse drain current tested ①	$T_C=25^\circ\text{C}$	320 A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A=25^\circ\text{C}$	10 A
		$T_A=70^\circ\text{C}$	8 A
EAS	Avalanche energy, single pulsed ②	240	mJ
P_D	Maximum power dissipation	$T_C=25^\circ\text{C}$	75 W
		$T_C=100^\circ\text{C}$	38 W
P_{DSM}	Maximum power dissipation ③	$T_A=25^\circ\text{C}$	1.3 W
		$T_A=70^\circ\text{C}$	0.8 W
T_{STG}, T_J	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current (T _j =125°C)	V _{DS} =40V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.6	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =20A	--	5	7.5	mΩ
		T _j =100°C	--	7	--	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =4.5V, I _D =15A	--	6	8.5	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	--	1400	--	pF
C _{oss}	Output Capacitance		--	220	--	pF
C _{rss}	Reverse Transfer Capacitance		--	150	--	pF
Q _g (10V)	Total Gate Charge	V _{DS} =20V, I _D =10A, V _{GS} =10V	--	37	--	nC
Q _g (4.5V)	Total Gate Charge		--	26	--	nC
Q _{gs}	Gate-Source Charge		--	7	--	nC
Q _{gd}	Gate-Drain Charge		--	18	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =9A, R _G =6.8Ω, V _{GS} =10V	--	16	--	ns
t _r	Turn-on Rise Time		--	15	--	ns
t _{d(off)}	Turn-Off Delay Time		--	20	--	ns
t _f	Turn-Off Fall Time		--	12	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =20A, V _{GS} =0V	--	0.8	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =20A, V _{GS} =0V	--	29	--	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	16	--	nC

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.3mH, R_G = 25Ω, I_{AS} = 40A, V_{GS} = 10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycles ≤ 2%.

Typical Characteristics

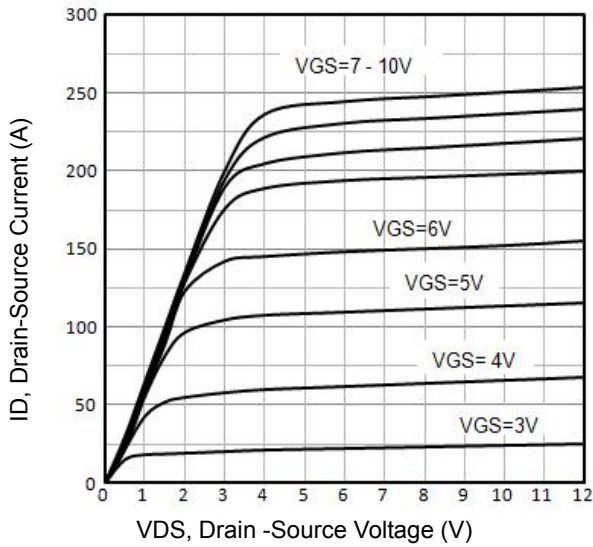


Fig1. Typical Output Characteristics

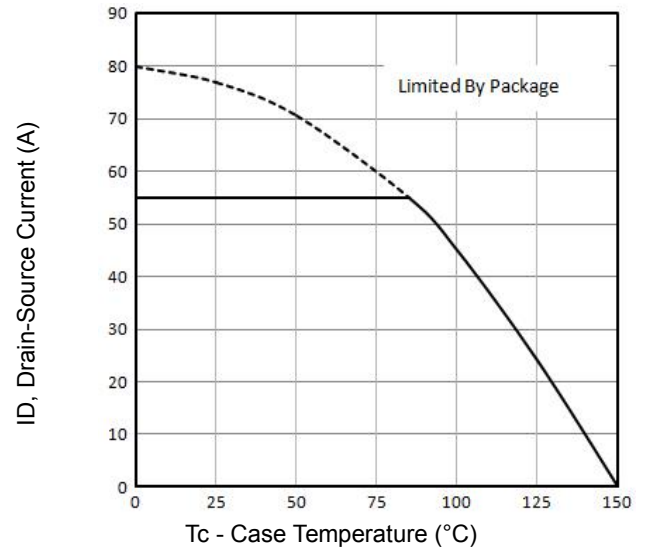


Fig2. Maximum Drain Current Vs. Case Temperature T_c ,

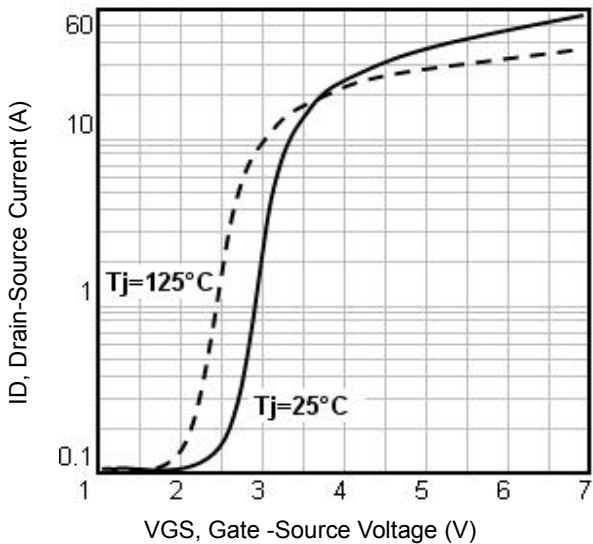


Fig3. Typical Transfer Characteristics

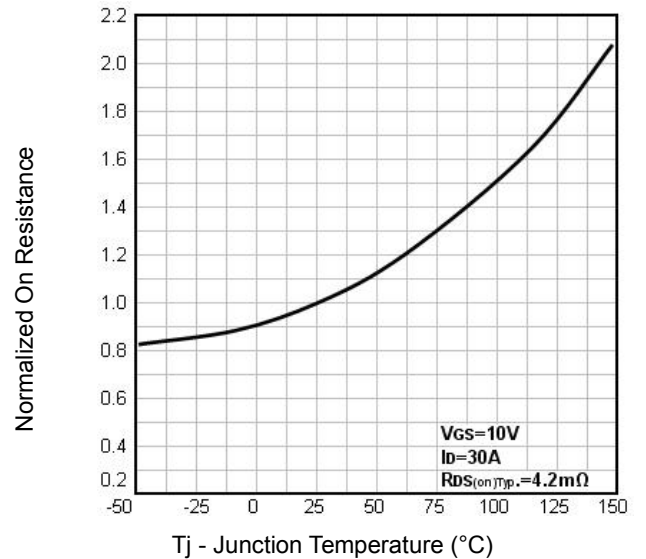


Fig4. Normalized On-Resistance Vs. T_j

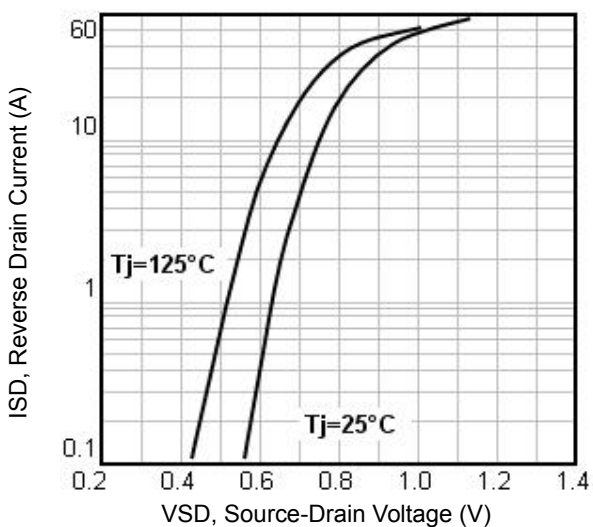


Fig5. Typical Source-Drain Diode Forward Voltage

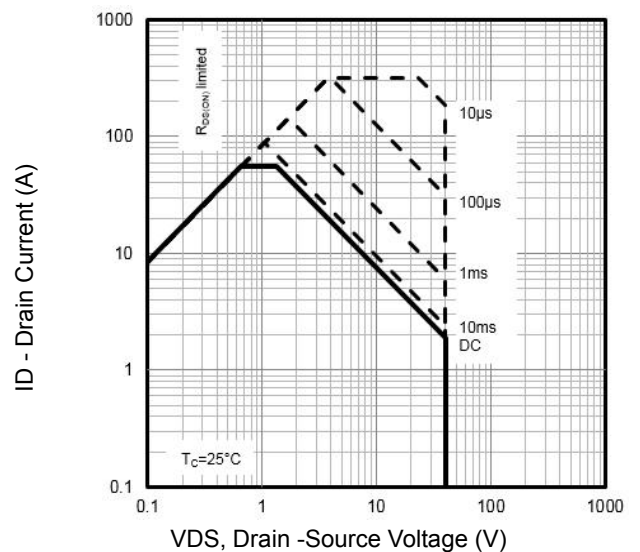


Fig6. Maximum Safe Operating Area

Typical Characteristics

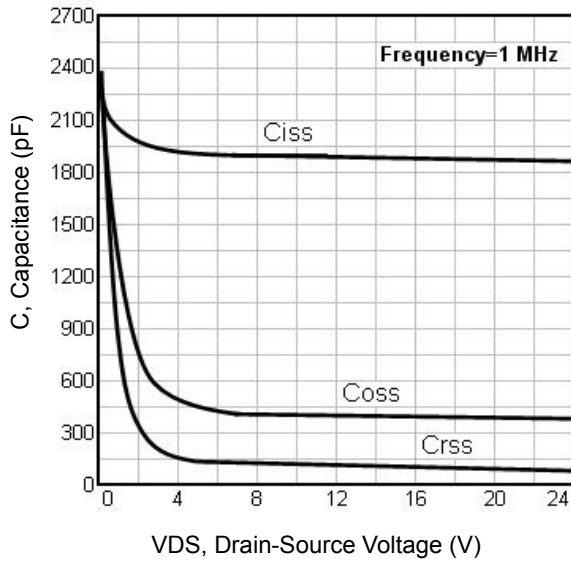


Fig7. Typical Capacitance Vs. Drain-Source Voltage

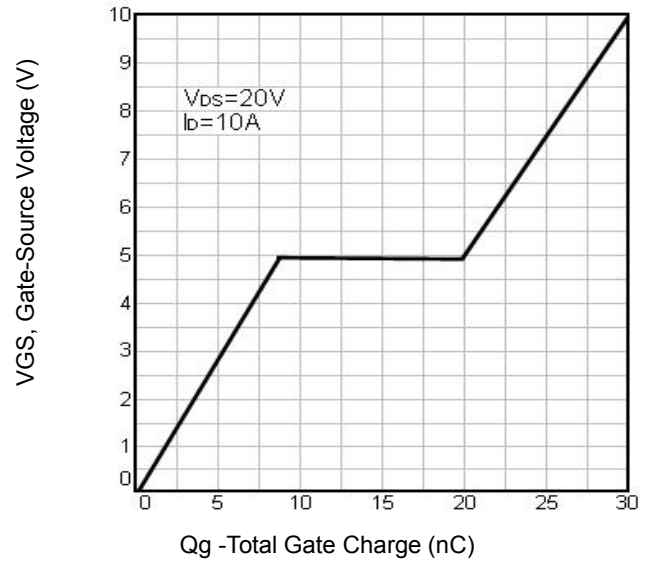


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

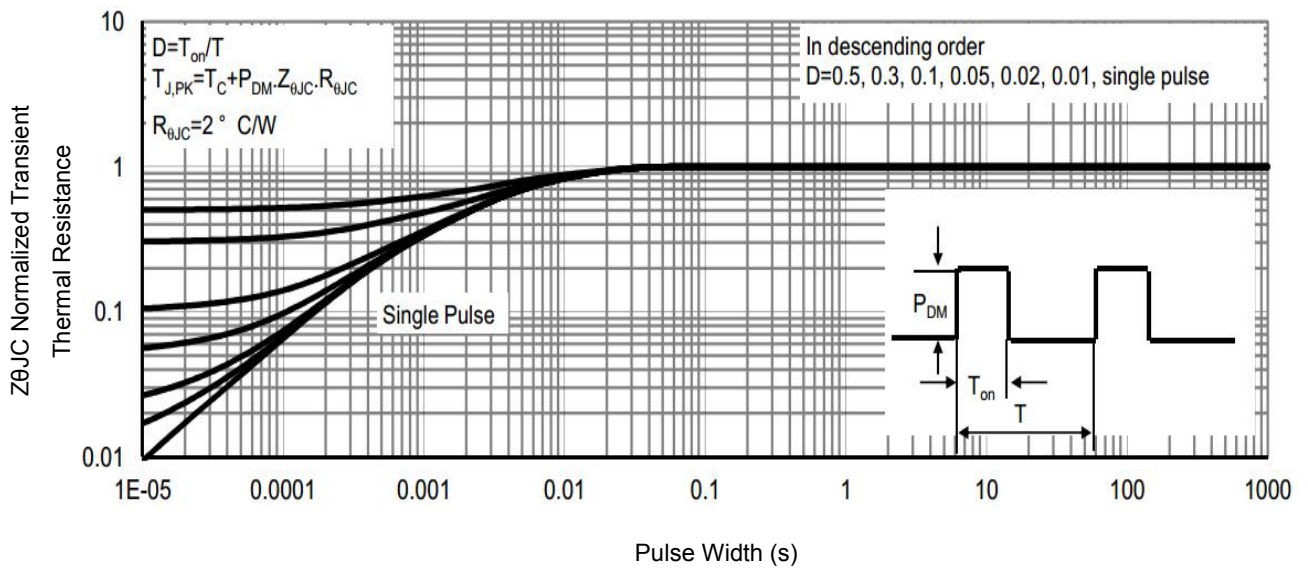


Fig9. Normalized Maximum Transient Thermal Impedance

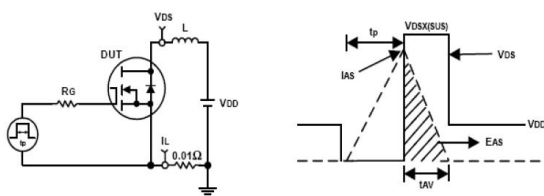


Fig10. Unclamped Inductive Test Circuit and waveforms

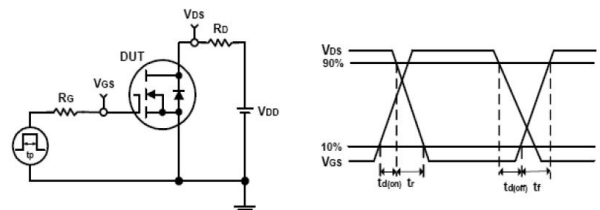
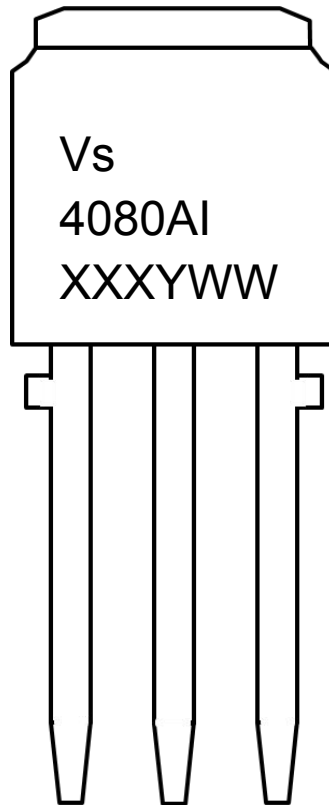


Fig11. Switching Time Test Circuit and waveforms



Marking Information



1st line: Vanguard Code (Vs)

2nd line: Part Number (4080AI)

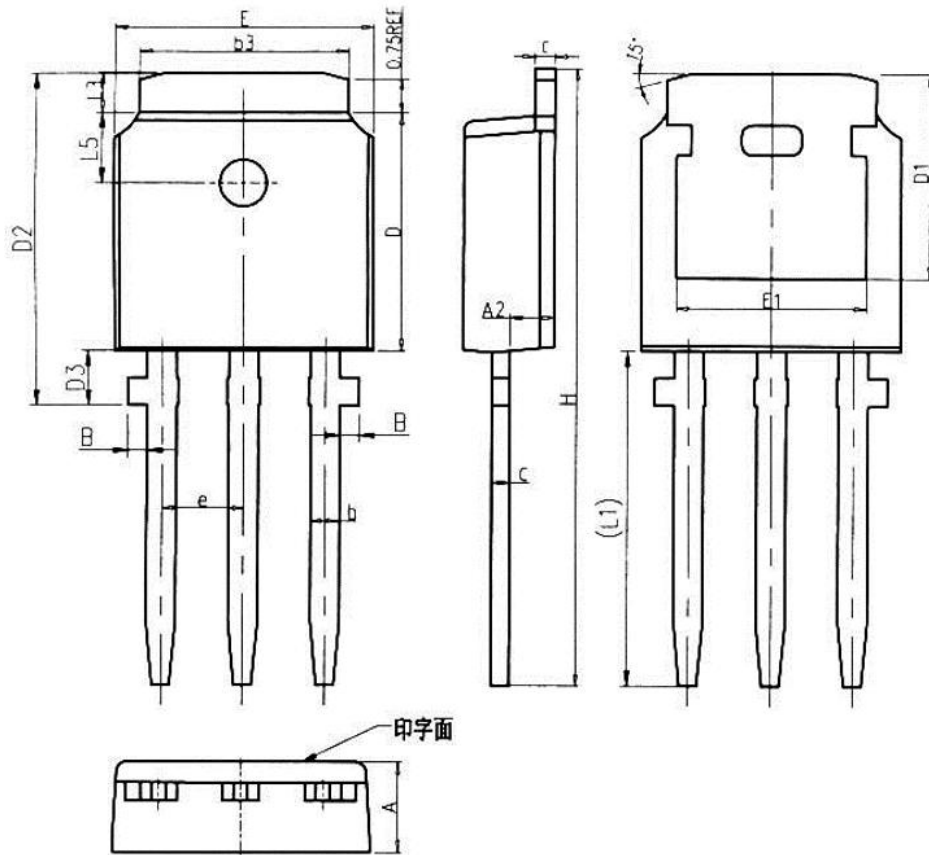
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code (e.g. E=2017, F=2018, G=2019, H=2020, etc)

WW: Week Code (01 to 53)

QIPAK Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.40
A2	0.97	1.07	1.17
B	0.25	0.40	0.55
b	0.68	0.78	0.90
b3	5.20	5.33	5.50
c	0.43	0.53	0.63
D	5.98	6.10	6.22
D1	5.30 REF		
D2	7.96	8.16	8.36
D3	0.85	1.05	1.25
E	6.40	6.60	6.80
E1	4.63	--	--
e	2.286 BSC		
H	16.22	16.52	16.82
L1	9.15	9.40	9.65
L3	0.88	1.02	1.28
L5	1.65	1.80	1.95

Note:

Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

Customer Service

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