

Features

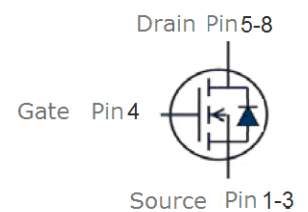
- N-Channel, 10V Logic Level Control
- Enhancement mode
- Advanced Package for Low RDS(on) and High Efficiency
- 100% Avalanche test
- Applicable to DC/DC and AC/DC converters
- Pb-free lead plating; RoHS compliant



Part ID	Package Type	Marking	Tape and reel information
VS4602AP	PDFN5x6	4602AP	3000PCS/Reel

V_{DS}	40	V
$R_{DS(on),TYP} @ V_{GS}=10\text{ V}$	1.6	m Ω
I_D	220	A

PDFN5x6



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	40	V
V_{GS}	Gate-Source voltage	± 25	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	220 A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$	$T_C = 25^\circ\text{C}$	220 A
		$T_C = 100^\circ\text{C}$	139 A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	40 A
		$T_A = 70^\circ\text{C}$	32 A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	880 A
EAS	Avalanche energy, single pulsed ②	365	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	125 W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	4 W
T_{STG}, T_J	Storage and Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	30	$^\circ\text{C/W}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =40V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±25V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.4	3	3.9	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =30A	--	1.6	2.5	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	8250	9260	10250	pF
C _{oss}	Output Capacitance		500	720	950	pF
C _{rss}	Reverse Transfer Capacitance		250	400	550	pF
R _g	Gate Resistance	f=1MHz	--	4.8	--	Ω
Q _g	Total Gate Charge	V _{DS} =20V, I _D =30A, V _{GS} =10V	--	95.3	--	nC
Q _{gs}	Gate-Source Charge		--	15.4	--	nC
Q _{gd}	Gate-Drain Charge		--	18.8	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =30A, R _G =3Ω, V _{GS} =10V	--	13	--	ns
t _r	Turn-on Rise Time		--	9	--	ns
t _{d(off)}	Turn-Off Delay Time		--	101	--	ns
t _f	Turn-Off Fall Time		--	15	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =30A, V _{GS} =0V	--	0.8	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =30A, V _{GS} =0V	--	35	--	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs		24.2		nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 30A, V_{GS} = 10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Characteristics

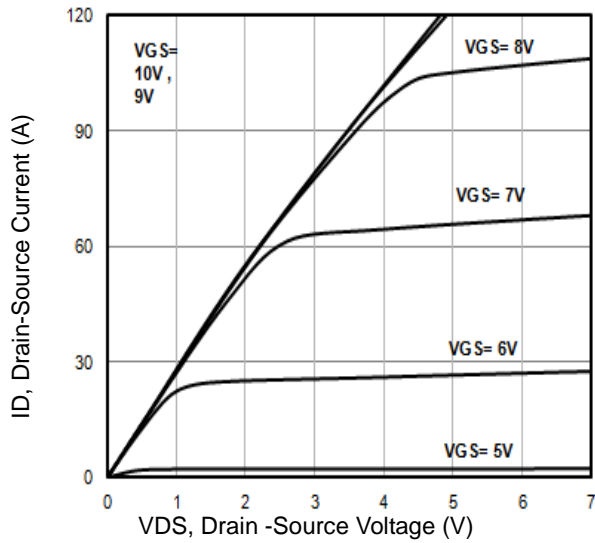


Fig1. Typical Output Characteristics

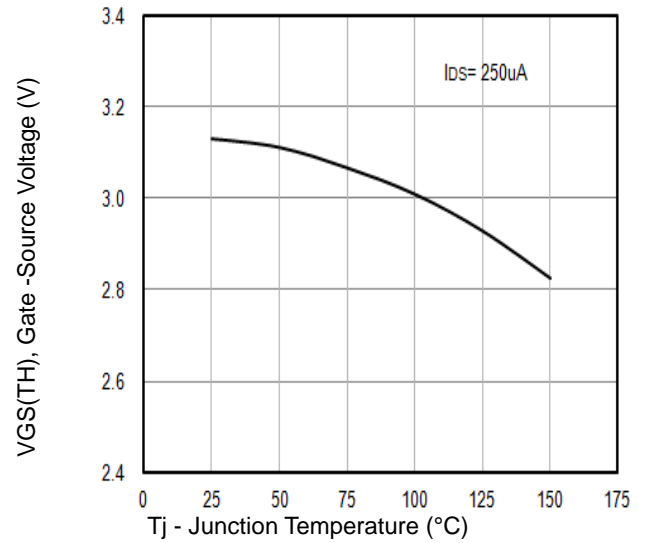


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

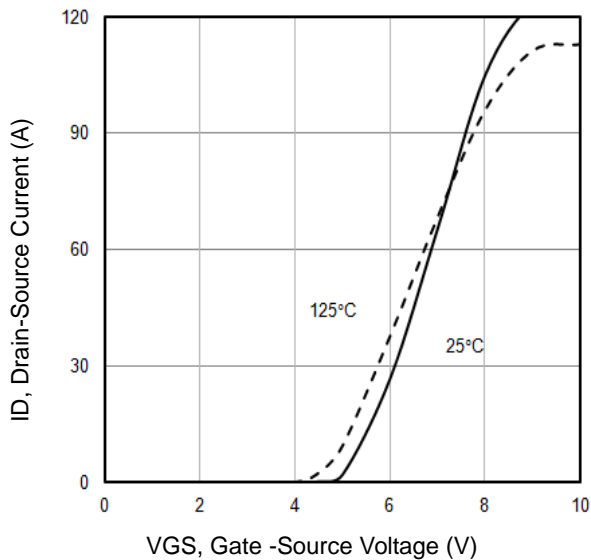


Fig3. Typical Transfer Characteristics

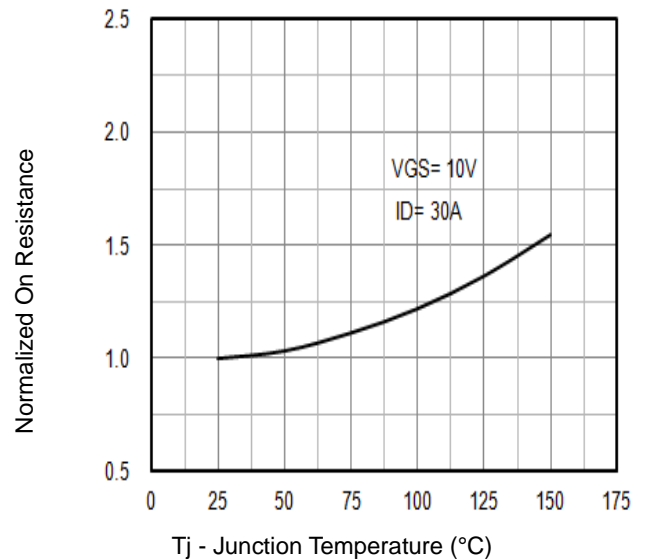


Fig4. Normalized On-Resistance Vs. T_j

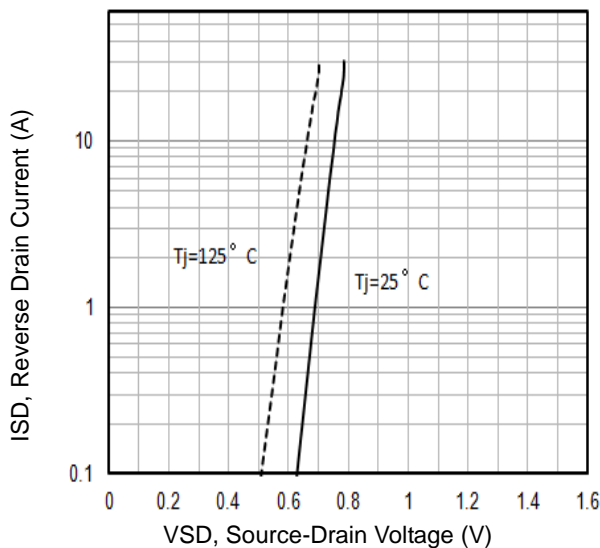


Fig5. Typical Source-Drain Diode Forward Voltage

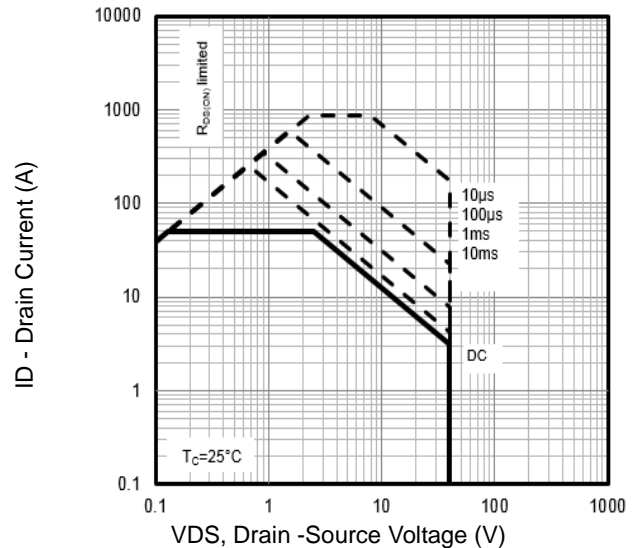


Fig6. Maximum Safe Operating Area

Typical Characteristics

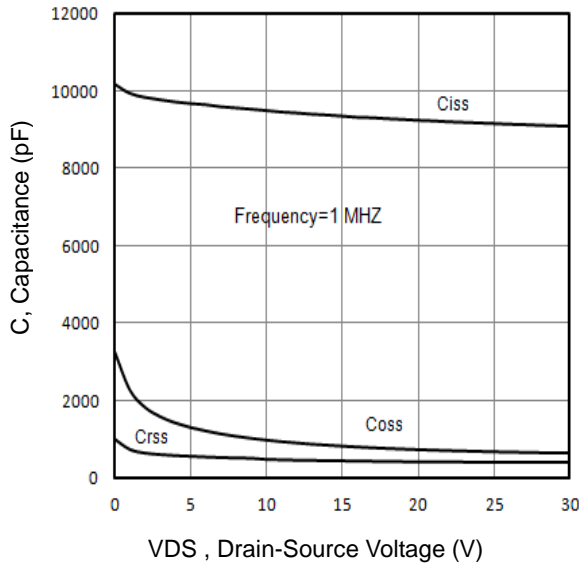


Fig7. Typical Capacitance Vs. Drain-Source Voltage

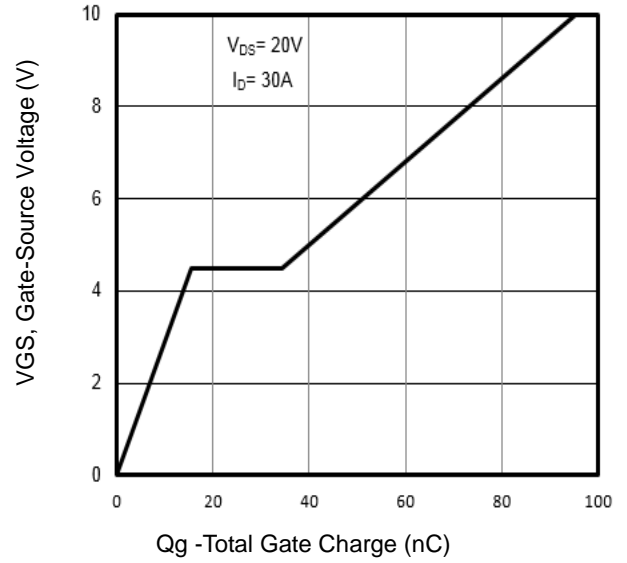


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

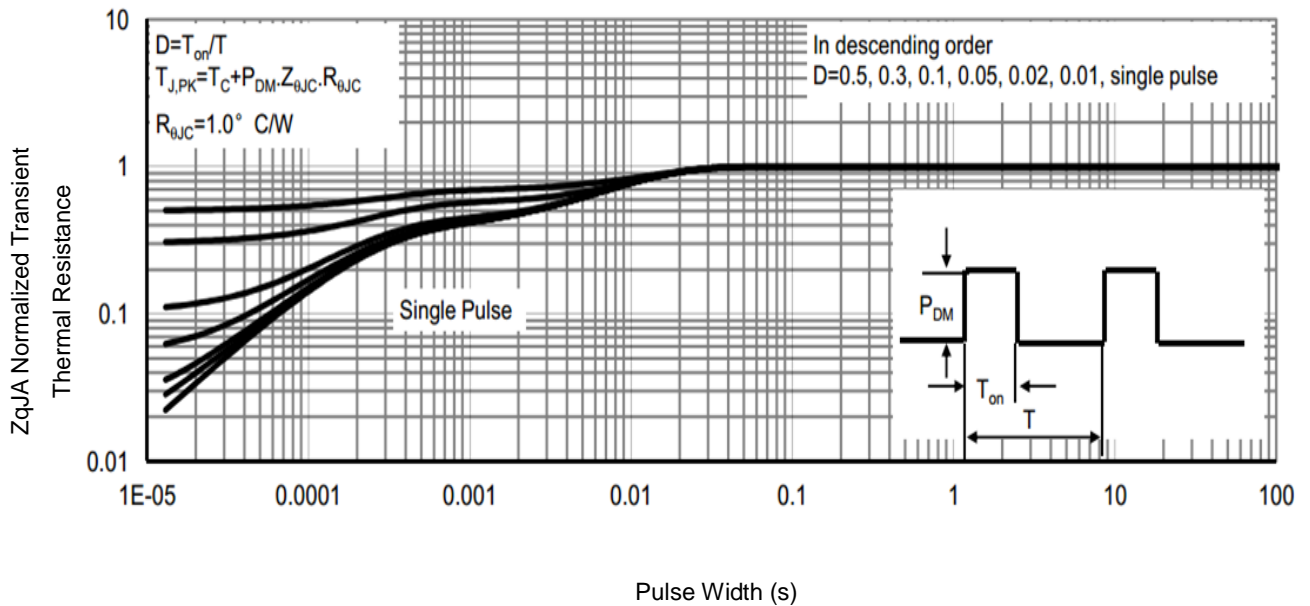


Fig9. Normalized Maximum Transient Thermal Impedance

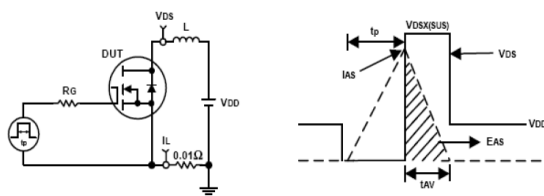


Fig10. Unclamped Inductive Test Circuit and waveforms

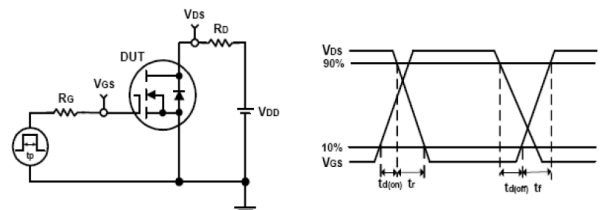
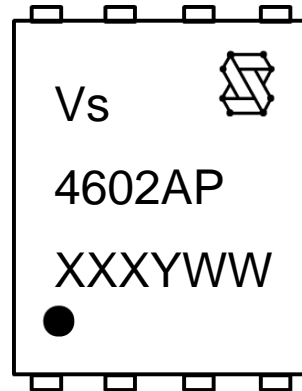
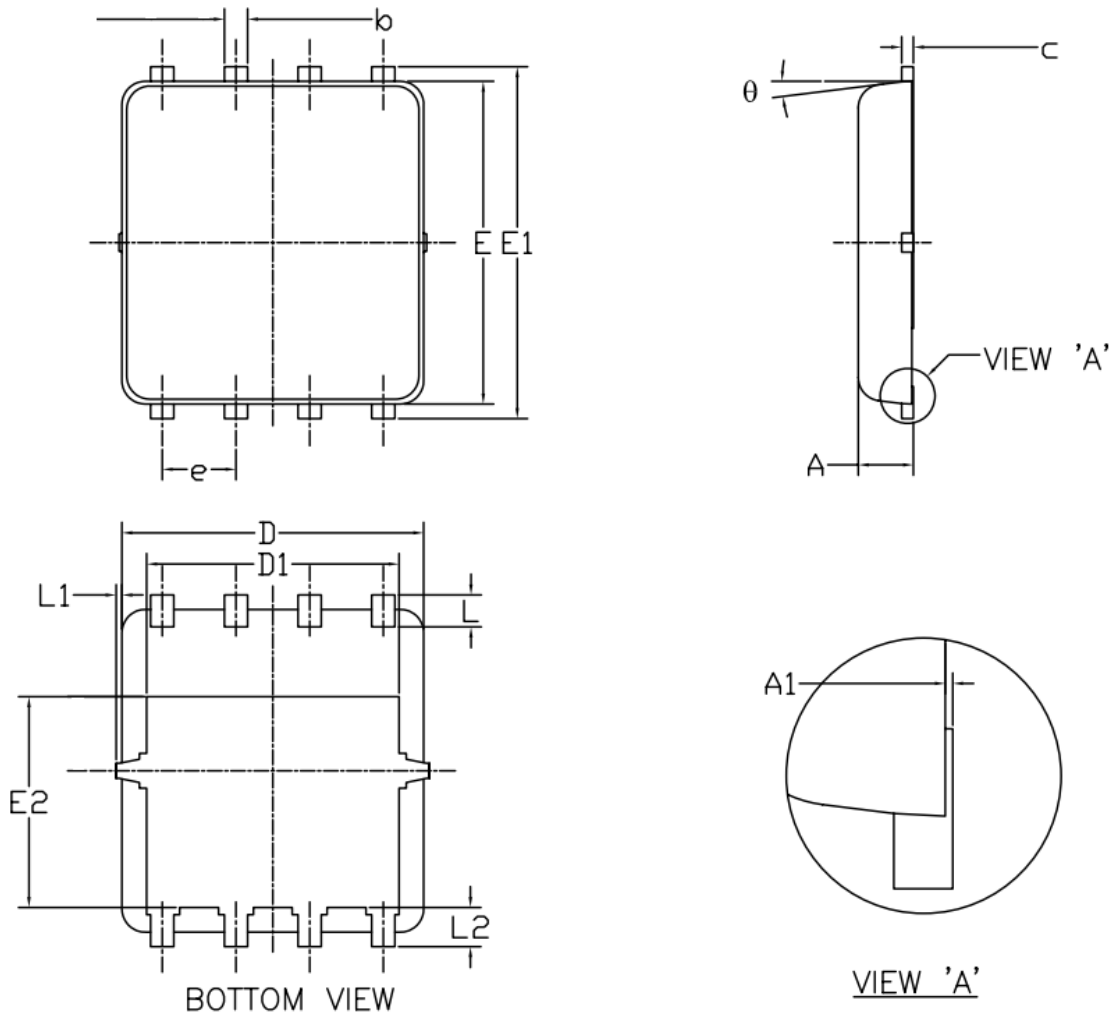


Fig11. Switching Time Test Circuit and waveforms

Marking Information



- 1st line: Vanguard Code (Vs), Vanguard Logo
2nd line: Part Number (4602AP)
3rd line: Date code (XXXYWW)
XXX: Wafer Lot Number
Y: Year Code, e.g. E means 2017
WW: Week Code

PDFN5x6 Package Outline Data


Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.20
A1	0.00	--	0.05
b	0.30	0.40	0.51
c	0.20	0.25	0.33
D	4.80	4.90	5.40
D1	3.61	4.00	4.25
E	5.65	5.80	6.06
E1	5.90	6.10	6.35
E2	3.38	3.58	3.92
e	1.27 BSC		
L	0.51	0.61	0.71
L1	--	--	0.15
L2	0.41	0.51	0.61
θ	0°	--	12°

Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D" and "E" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D" and "E" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service
Sales and Service:
sales@vgsemi.com
Vanguard Semiconductor CO., LTD
TEL: (86-755) -26902410

FAX: (86-755) -26907027

WEB: www.vgsemi.com

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