

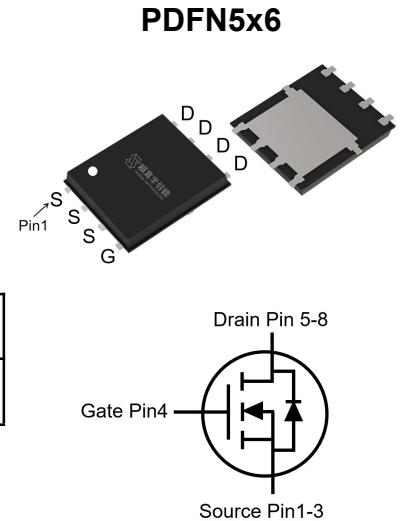
Features

- Enhancement mode
- Very low on-resistance
- VitoMOS[®] II Technology
- Fast Switching and High efficiency
- 100% Avalanche Tested, 100% Rg Tested

V_{DS}	40	V
$R_{DS(on),TYP@ V_{GS}=10V}$	1.3	mΩ
$I_D(\text{Silicon Limited})$	160	A
$I_D(\text{Package Limited})$	100	A



Part ID	Package Type	Marking	Packing
VS4603GPHT	PDFN5x6	4603GPH	3000pcs/Reel



Maximum ratings, at $T_A=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit	
$V_{(BR)DSS}$	Drain-Source breakdown voltage	40	V	
V_{GS}	Gate-Source voltage	± 20	V	
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	160	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 25^\circ\text{C}$	160	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 100^\circ\text{C}$	101	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 25^\circ\text{C}$	100	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	640	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ\text{C}$	32	A
		$T_A = 70^\circ\text{C}$	25	A
E_{AS}	Avalanche energy, single pulsed ②	576	mJ	
P_D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$	66	W
		$T_C = 100^\circ\text{C}$	26	W
P_{DSM}	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$	2.6	W
		$T_A = 70^\circ\text{C}$	1.7	W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 150	$^\circ\text{C}$	

Thermal Characteristics

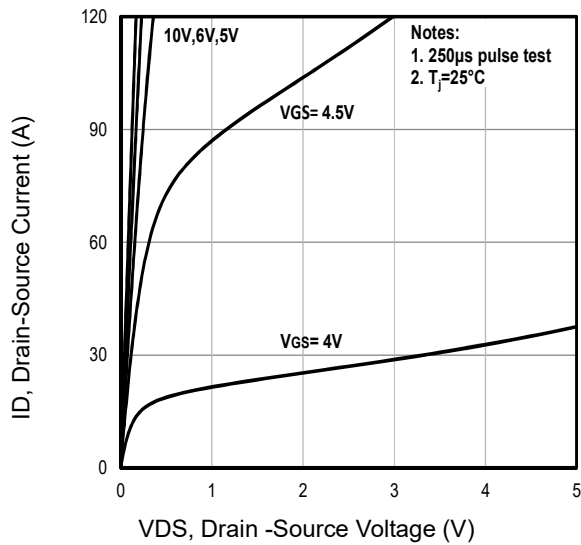
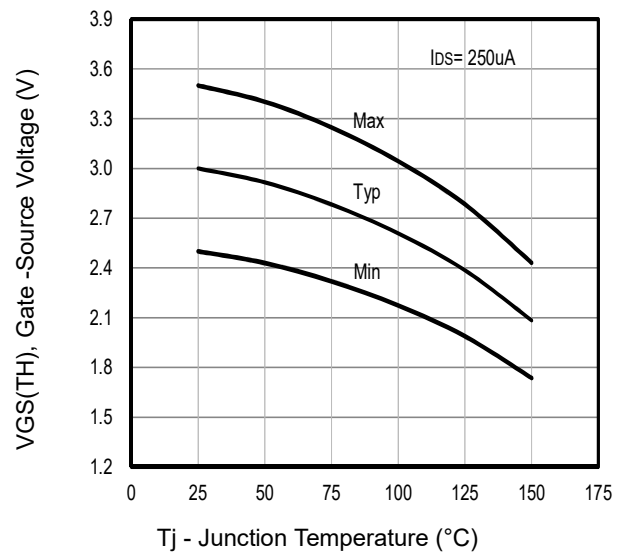
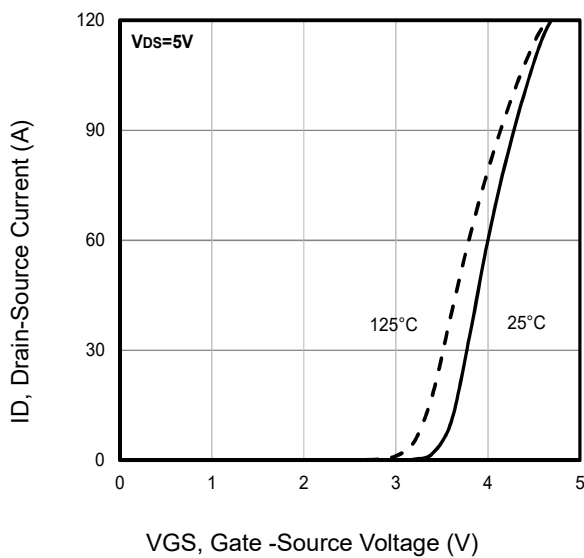
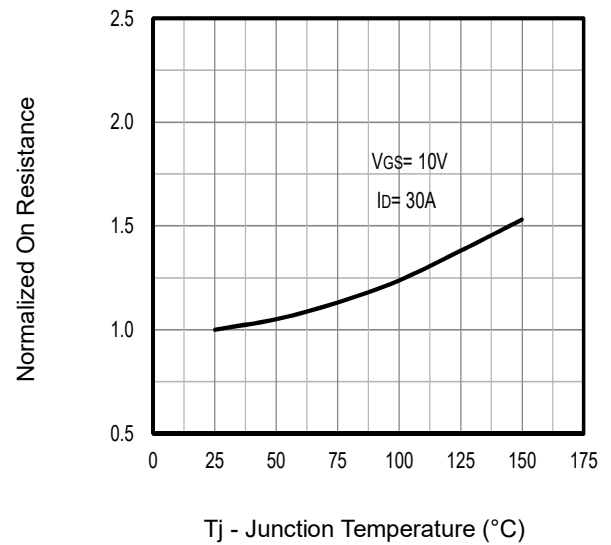
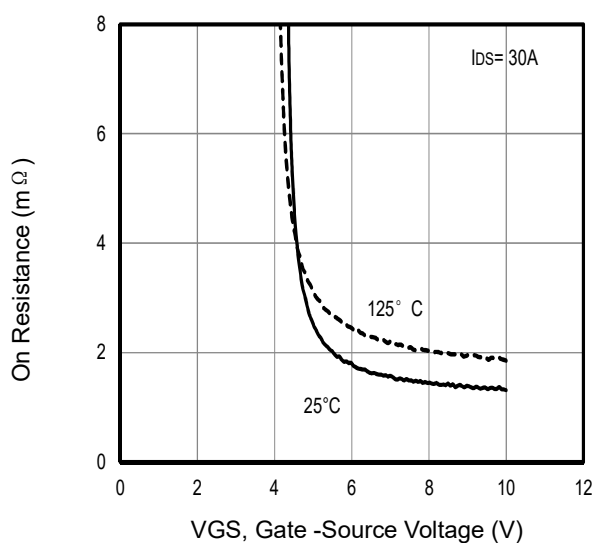
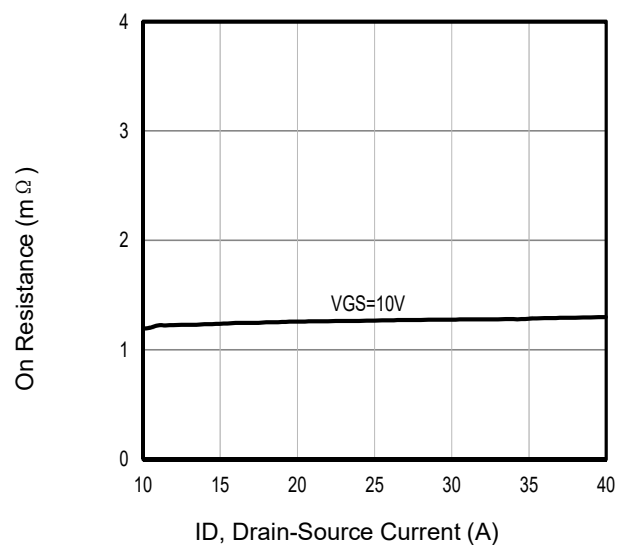
Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	1.6	1.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	40	48	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)⑦	V _{DS} =40V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.5	3.0	3.5	V
R _{DS(on)}	Drain-Source On-State Resistance ⑧	V _{GS} =10V, I _D =30A	--	1.3	1.7	mΩ
		T _j =100°C ⑦	--	1.6	--	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance ⑦	V _{DS} =20V, V _{GS} =0V, f=1MHz	--	6665	--	pF
C _{oss}	Output Capacitance ⑦		--	1680	--	pF
C _{rss}	Reverse Transfer Capacitance ⑦		--	120	--	pF
R _g	Gate Resistance	f=1MHz	--	3.3	--	Ω
Q _g	Total Gate Charge ⑦	V _{DS} =20V, I _D =30A, V _{GS} =10V	--	96	--	nC
Q _{gs}	Gate-Source Charge ⑦		--	27	--	nC
Q _{gd}	Gate-Drain Charge ⑦		--	16	--	nC
Switching Characteristics ⑦						
T _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =30A, R _G =3Ω, V _{GS} =10V	--	13	--	ns
T _r	Turn-on Rise Time		--	70	--	ns
T _{d(off)}	Turn-Off Delay Time		--	85	--	ns
T _f	Turn-Off Fall Time		--	43	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =30A, V _{GS} =0V	--	0.8	1.2	V
T _{rr}	Reverse Recovery Time ⑦	I _{sd} =30A, V _{GS} =0V di/dt=100A/μs	--	44	--	ns
Q _{rr}	Reverse Recovery Charge ⑦		--	31	--	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② EAS of 576mJ is based on starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 48A, V_{GS} = 10V; 100% FT tested at L = 0.5mH, I_{AS} = 24A.
- ③ The power dissipation P_d is based on T_j(max), using junction-to-case thermal resistance R_{θJC}.
- ④ The power dissipation P_{dsm} is based on T_j(max), using junction-to-ambient thermal resistance R_{θJA}.
- ⑤ These tests are performed respectively with the device mounted on a 1 in2 pad and a minimum pad of 2oz. Copper FR-4 board in a still air environment with TA=25°C, using Transient Dual Interface method to acquire R_{θJC}.
- ⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

Fig1. Typical Output Characteristics

Fig2. Typical $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

Fig3. Typical Transfer Characteristics

Fig4. Typical Normalized On-Resistance Vs. T_j

Fig5. Typical On Resistance Vs Gate-Source Voltage

Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

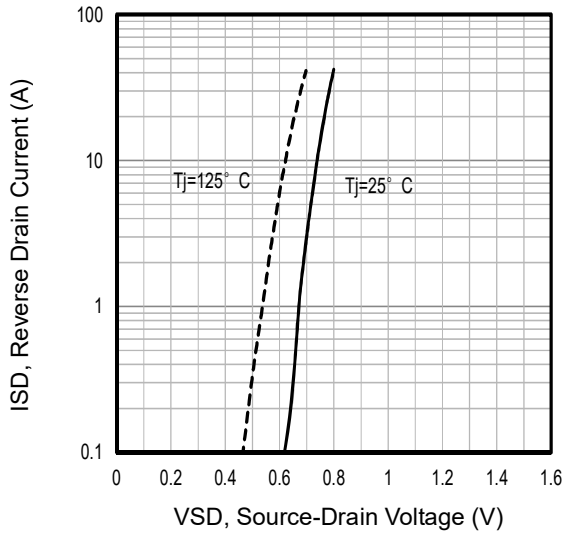


Fig7. Typical Source-Drain Diode Forward Voltage

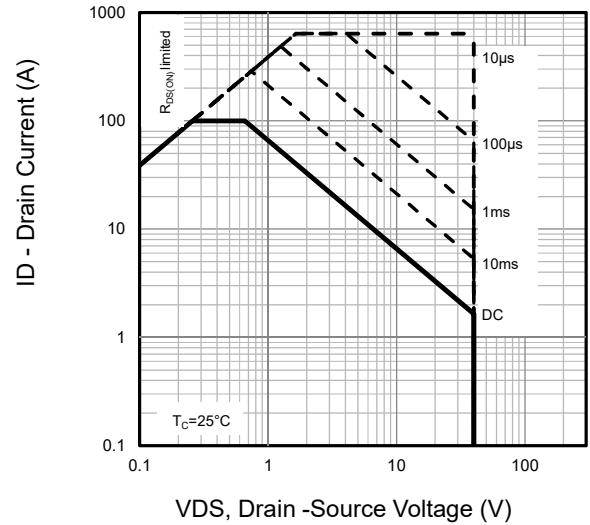


Fig8. Maximum Safe Operating Area

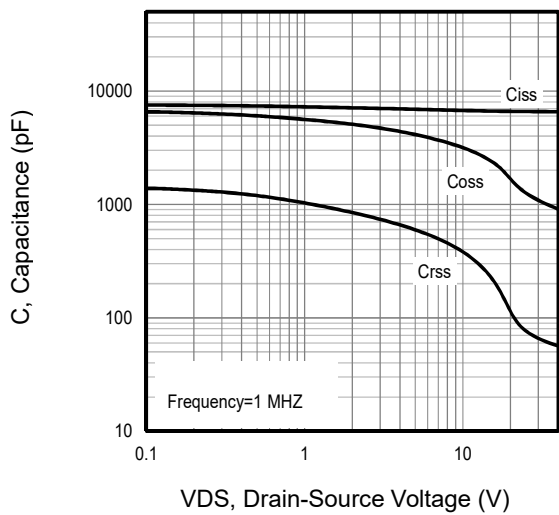


Fig9. Typical Capacitance Vs. Drain-Source Voltage

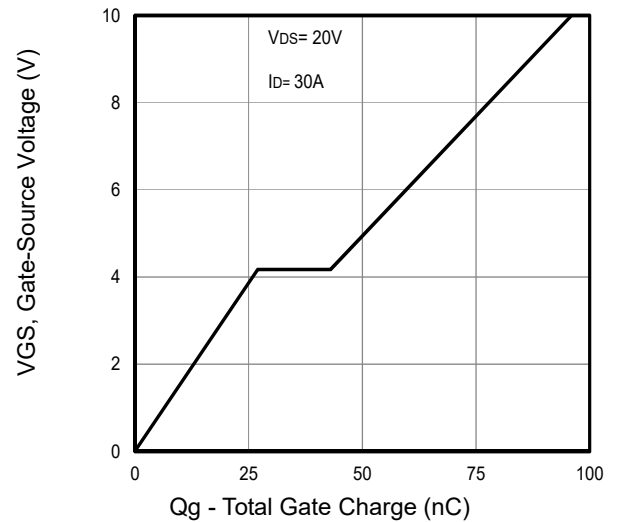


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

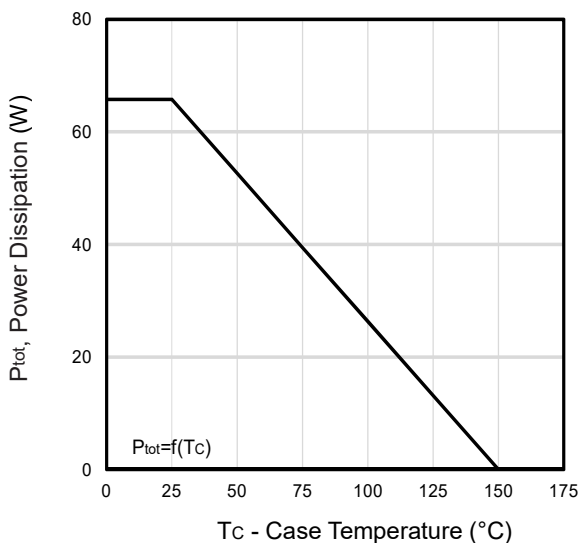


Fig11. Power Dissipation Vs. Case Temperature

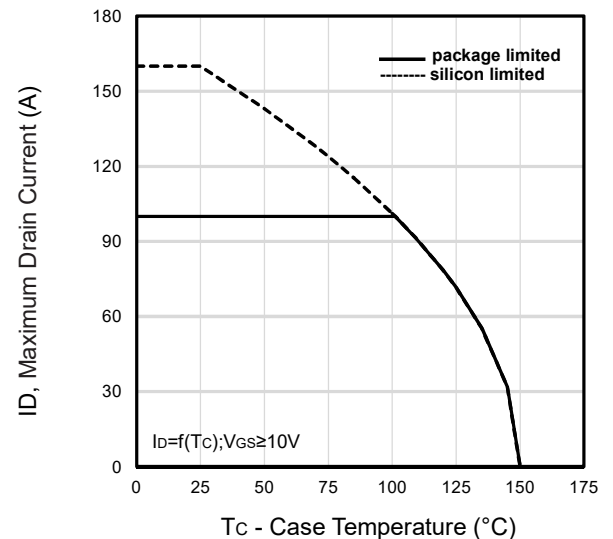


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

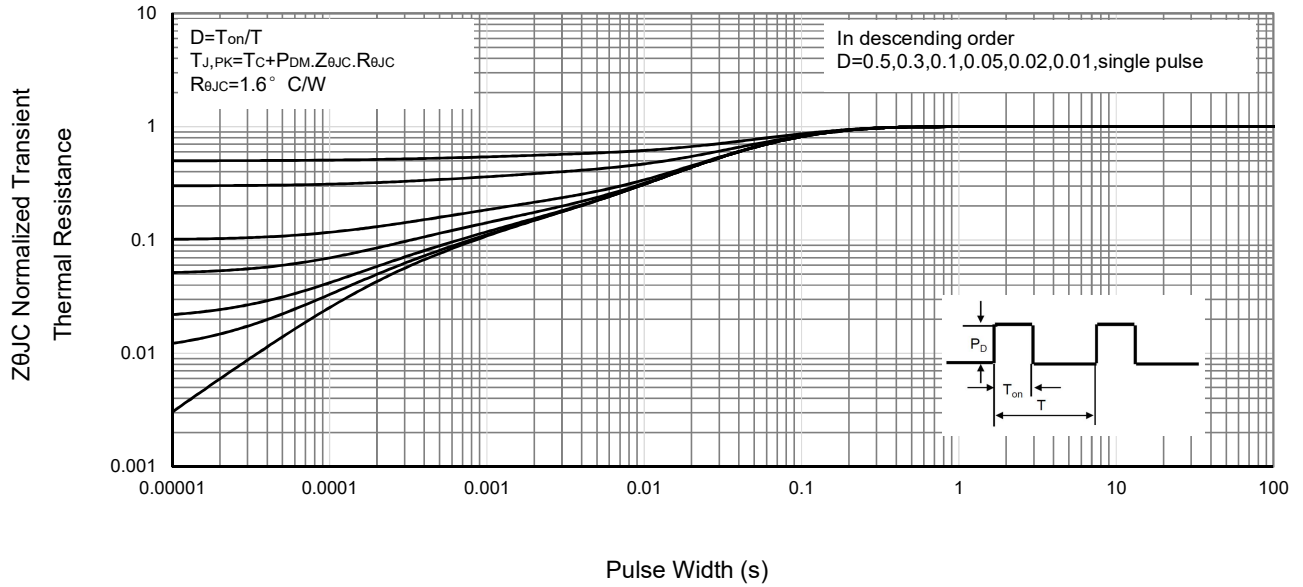


Fig13 . Normalized Maximum Transient Thermal Impedance

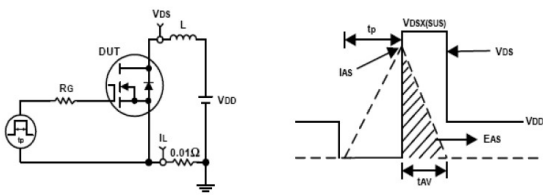


Fig14. Unclamped Inductive Test Circuit and waveforms

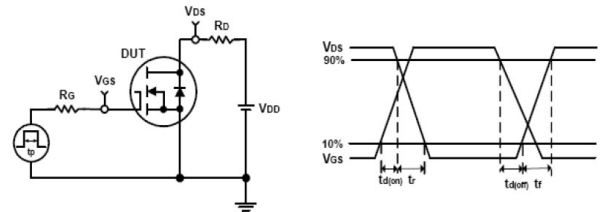
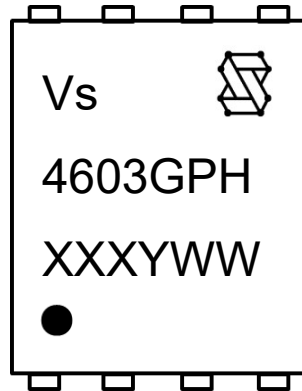


Fig15. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (4603GPH)

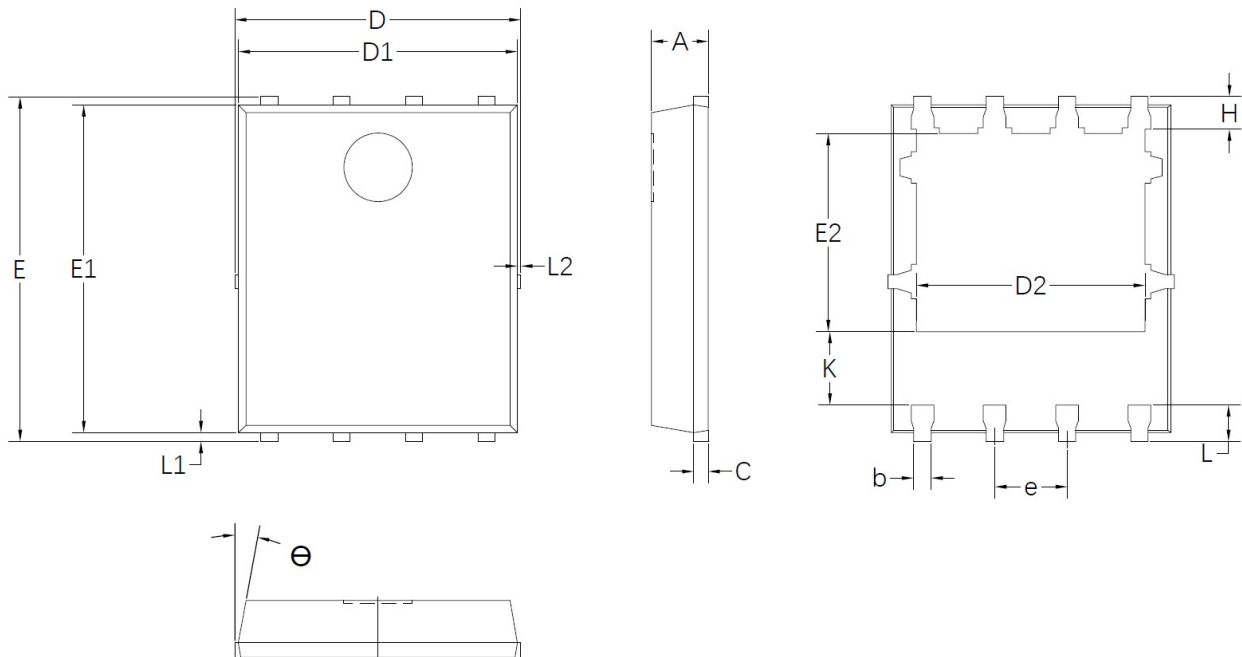
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN5x6 Package Outline Data


Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.10
b	0.35	0.40	0.45
C	0.21	0.25	0.34
D	--	--	5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.27 BSC		
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.375	3.475	3.575
H	0.55	0.65	0.75
K	1.29	--	--
L	0.55	0.65	0.75
L1	0.05	0.15	0.25
L2	--	--	0.12
θ	8°	10°	12°

Notes:

- 1.Refer to JEDEC MO-240 variation AA.
- 2.Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
- 3.Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service
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[TK31J60W5,S1VQ\(O](#) [2SK2614\(TE16L1,Q\)](#) [DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [FCAB21350L1](#) [P85W28HP2F-7071](#) [DMN1053UCP4-7](#)
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[BSS340NWH6327XTSA1](#) [MCM3400A-TP](#) [DMTH10H4M6SPS-13](#) [IRF40SC240ARMA1](#) [IPS60R1K0PFD7SAKMA1](#)
[IPS60R360PFD7SAKMA1](#) [IPS60R600PFD7SAKMA1](#)