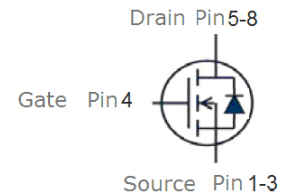**Vanguard Semiconductor**

Features

- N-Channel，5V Logic Level Control

- Enhancement mode

- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V

- VitoMOS$^®$ Technology

- 100% Avalanche test

- Pb-free lead plating; RoHS compliant

Pb-Free · RoHS · (HF) Halogen-Free

V_{DS}	65	V
$R_{DS(on),TYP}$ @ V_{GS}=10 V	19	mΩ
$R_{DS(on),TYP}$ @ V_{GS}=4.5 V	22	mΩ
I_D	30	A

PDFN3333

Drain Pin 5-8
Gate Pin 4
Source Pin 1-3

Part ID	Package Type	Marking	Tape and reel information
VS6412AE	PDFN3333	6412AE	5000PCS/Reel

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		65	V
I_S	Diode continuous forward current	T_C =25°C	30	A
I_D	Continuous drain current @VGS=10V	T_C =25°C	30	A
		T_C =100°C	19	A
I_{DM}	Pulse drain current tested ①	T_C =25°C	120	A
EAS	Avalanche energy, single pulsed ②		121	mJ
P_D	Maximum power dissipation	T_C =25°C	32	W
V_{GS}	Gate-Source voltage		±20	V
T_{STG} T_J	Storage and operating temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	3.9	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	35	°C/W

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250µA	65	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=65V,V_{GS}=0V	--	--	0.1	µA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=65V,V_{GS}=0V	--	--	100	µA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250µA	1.0	1.8	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance③	V_{GS}=10V, I_D=15A	--	19	24	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance③	V_{GS}=4.5V, I_D=10A	--	22	26	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=30V,V_{GS}=0V, f=1MHz	--	1240	--	pF
C_{oss}	Output Capacitance		--	95	--	pF
C_{rss}	Reverse Transfer Capacitance		--	85	--	pF
R_g	Gate Resistance	f=1MHz	--	2.4	--	Ω
Q_g	Total Gate Charge	V_{DS}=30V,I_D=5A, V_{GS}=10V	--	21	--	nC
Q_{gs}	Gate-Source Charge		--	6	--	nC
Q_{gd}	Gate-Drain Charge		--	8.5	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=30V, I_D=5A, R_G=6.8Ω, V_{GS}=10V	--	12	--	nS
t_r	Turn-on Rise Time		--	8.5	--	nS
$t_{d(off)}$	Turn-Off Delay Time		--	42	--	nS
t_f	Turn-Off Fall Time		--	6	--	nS
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=15A,V_{GS}=0V	--	0.8	1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=5A, V_{GS}=0V di/dt=100A/µs	--	22	--	nS
Q_{rr}	Reverse Recovery Charge			86		nC

NOTE:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH,R_G = 25Ω, I_{AS} = 22A, V_{GS} =10V. Part not recommended for use above this value

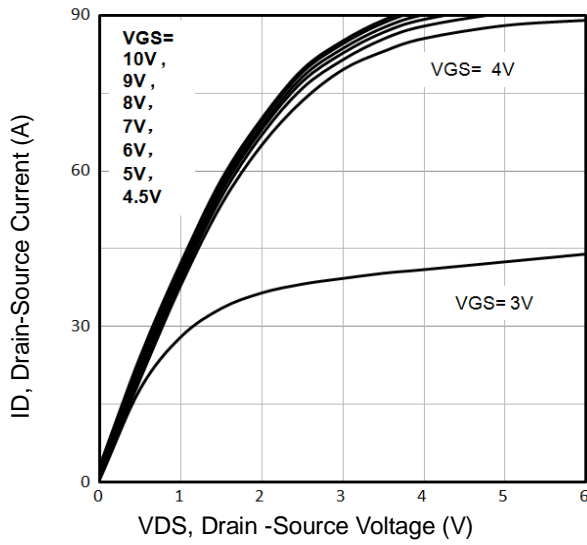③ Pulse width ≤ 300µs; duty cycle≤ 2%.

Typical Characteristics

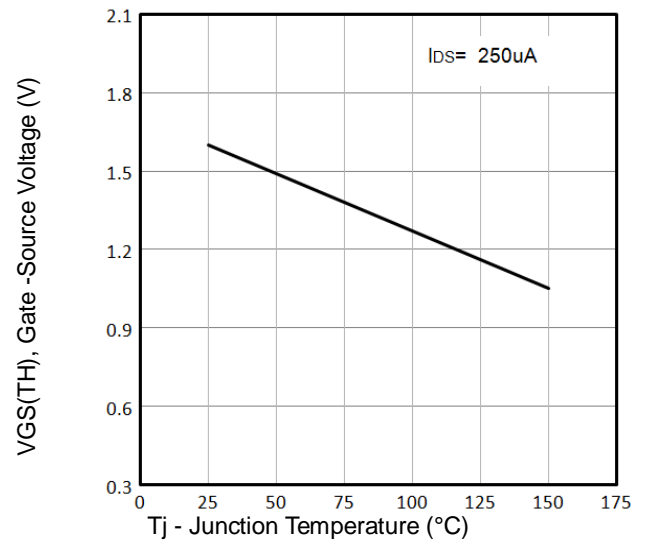**Fig1.** Typical Output Characteristics

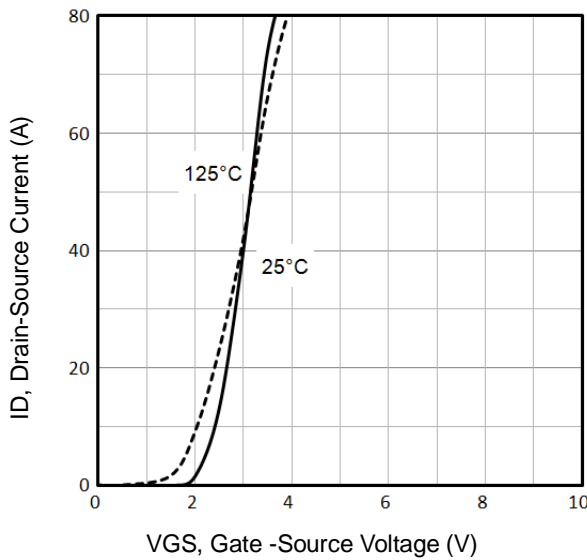**Fig2.** $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

Fig3. Typical Transfer Characteristics
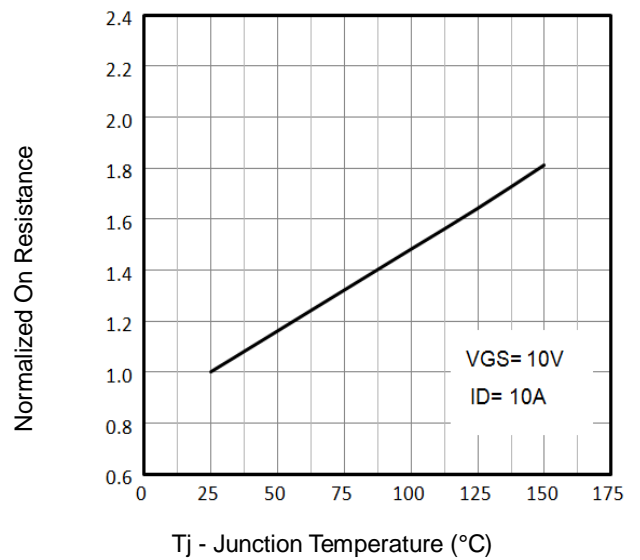

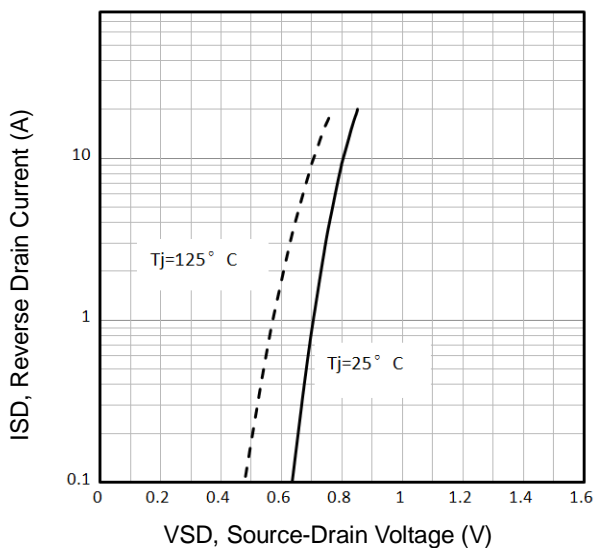**Fig4.** Normalized On-Resistance Vs. Tj

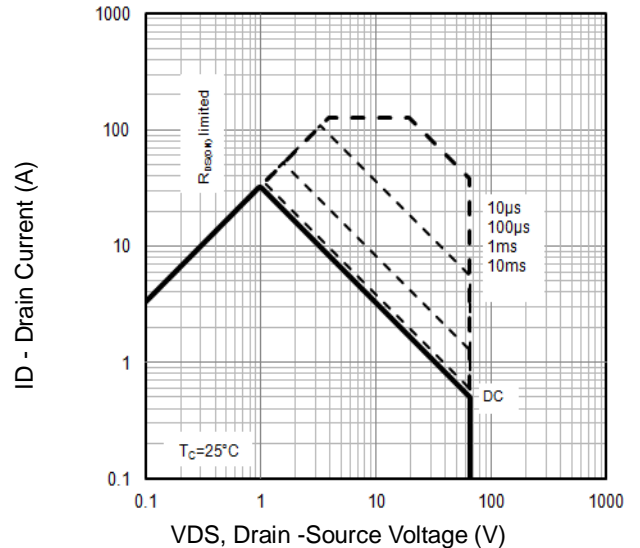**Fig5.** Typical Source-Drain Diode Forward Voltage

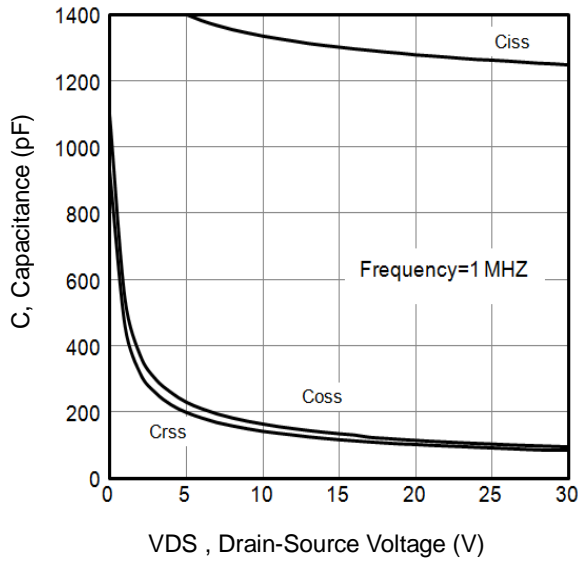**Fig6.** Maximum Safe Operating Area

Typical Characteristics
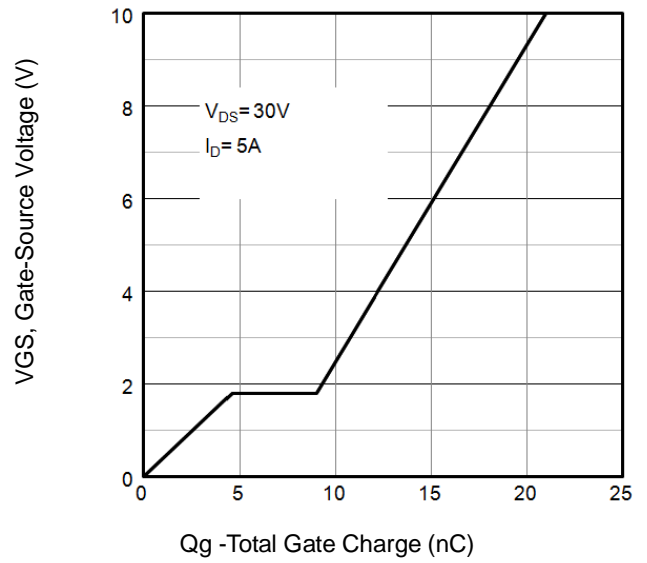

Fig7. Typical Capacitance Vs.Drain-Source Voltage

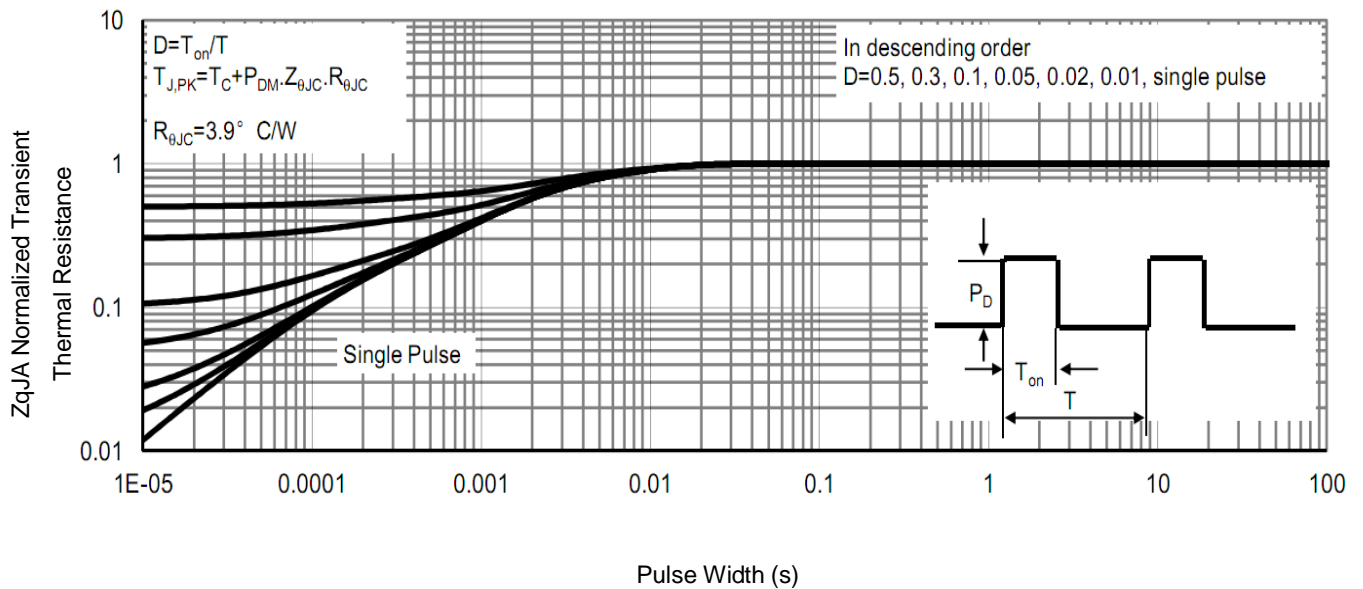**Fig8.** Typical Gate Charge Vs.Gate-Source Voltage

Pulse Width (s)

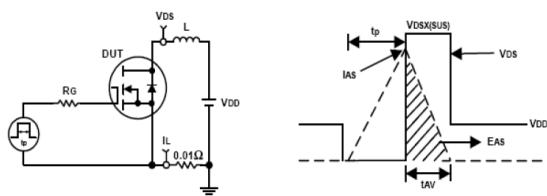**Fig9.** Normalized Maximum Transient Thermal Impedance

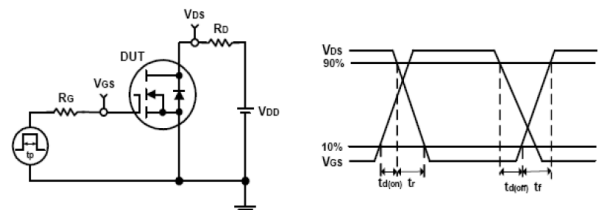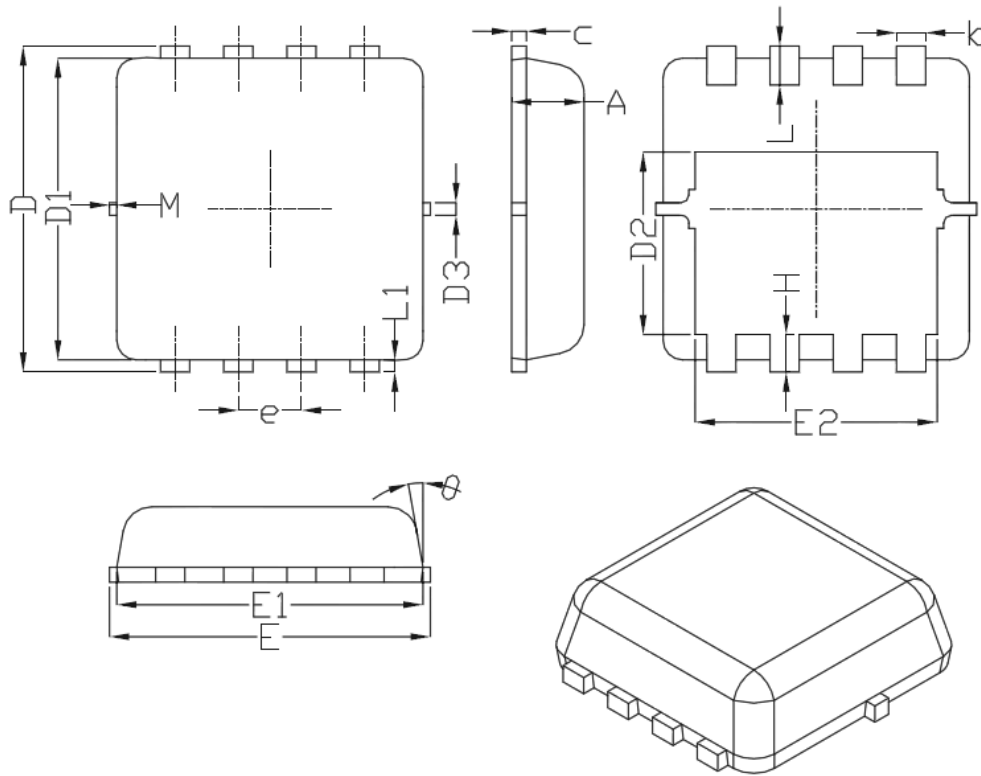**Fig10.** Unclamped Inductive Test Circuit and waveforms

Fig11. Switching Time Test Circuit and waveforms

PDFN3333 Package Outline Data

DIMENSIONS (unit : mm)

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.70	0.75	0.80	**b**	0.25	0.30	0.35
C	0.10	0.15	0.25	**D**	3.25	3.35	3.45
D1	3.00	3.10	3.20	**D2**	1.78	1.88	1.98
D3	--	0.13	--	**E**	3.20	3.30	3.40
E1	3.00	3.15	3.20	**E2**	2.39	2.49	2.59
e	0.65BSC			**H**	0.30	0.39	0.50
L	0.30	0.40	0.50	**L1**	--	0.13	--
θ	--	10°	12°	**M**	*	*	0.15
* Not specified							

Customer Service

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