

Features

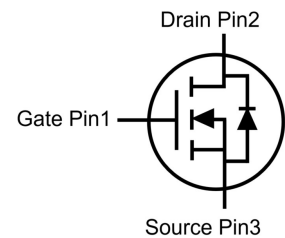
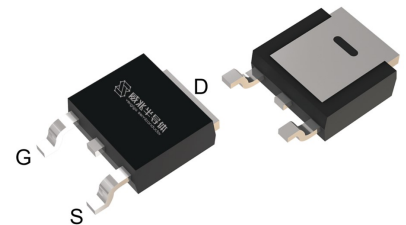
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- VitoMOS[®] II Technology
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant



Part ID	Package Type	Marking	Packing
VSD011N10MS-G	TO-252	011N10M	2500PCS/Reel

V_{DS}	100	V
$R_{DS(on),TYP@ V_{GS}=10\text{ V}}$	10	m Ω
$R_{DS(on),TYP@ V_{GS}=4.5\text{ V}}$	13.5	m Ω
I_D	58	A

TO-252



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	100	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	58 A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$	$T_C = 25^\circ\text{C}$	58 A
		$T_C = 100^\circ\text{C}$	41 A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	232 A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	8 A
		$T_A = 70^\circ\text{C}$	6 A
EAS	Avalanche energy, single pulsed ②	25	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	73 W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	1.3 W
T_{STG}, T_J	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.05	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	$^\circ\text{C/W}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =100V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.4	1.7	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =35A	--	10	13	mΩ
		T _j =100°C	--	13	--	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =4.5V, I _D =10A	--	13.5	18	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	1260	1480	1700	pF
C _{oss}	Output Capacitance		590	690	790	pF
C _{rss}	Reverse Transfer Capacitance		15	25	35	pF
R _g	Gate Resistance	f=1MHz	--	0.9	--	Ω
Q _g (10V)	Total Gate Charge	V _{DS} =50V, I _D =35A, V _{GS} =10V	--	25	--	nC
Q _g (4.5V)	Total Gate Charge		--	13	--	nC
Q _{gs}	Gate-Source Charge		--	5	--	nC
Q _{gd}	Gate-Drain Charge		--	5.2	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =50V, I _D =30A, R _G =3Ω, V _{GS} =10V	--	7.8	--	ns
t _r	Turn-on Rise Time		--	35	--	ns
t _{d(off)}	Turn-Off Delay Time		--	21	--	ns
t _f	Turn-Off Fall Time		--	26	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =35A, V _{GS} =0V	--	0.9	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =35A, V _{GS} =0V	--	50	--	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	54	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 10A, V_{GS} = 10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

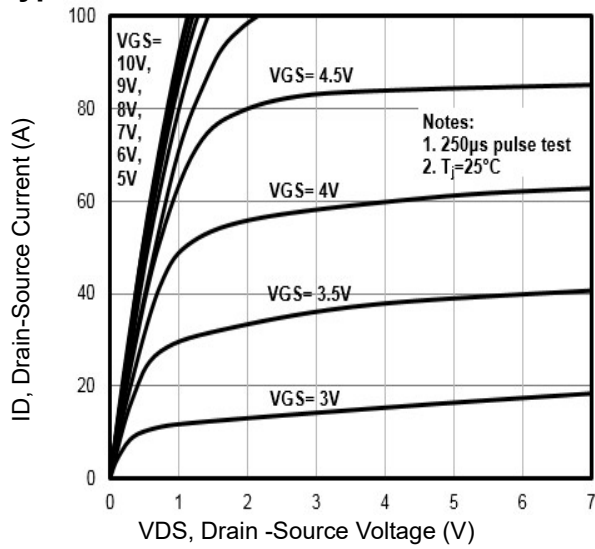


Fig1. Typical Output Characteristics

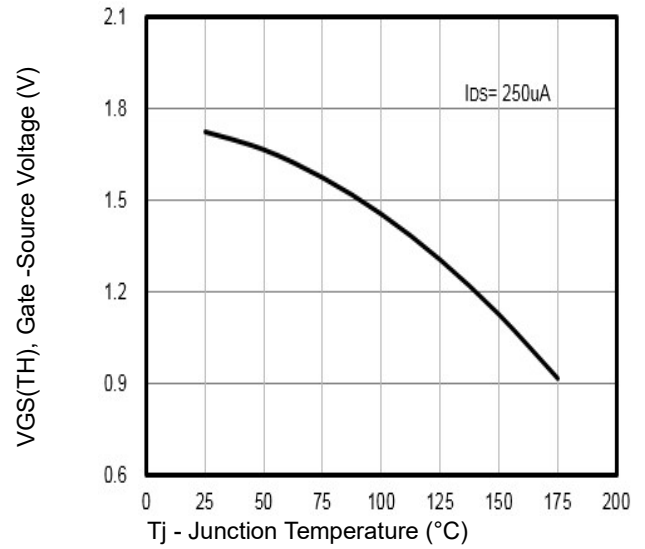


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

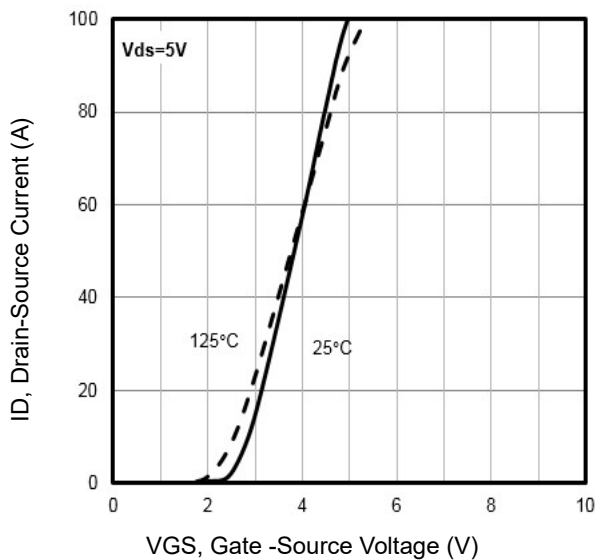


Fig3. Typical Transfer Characteristics

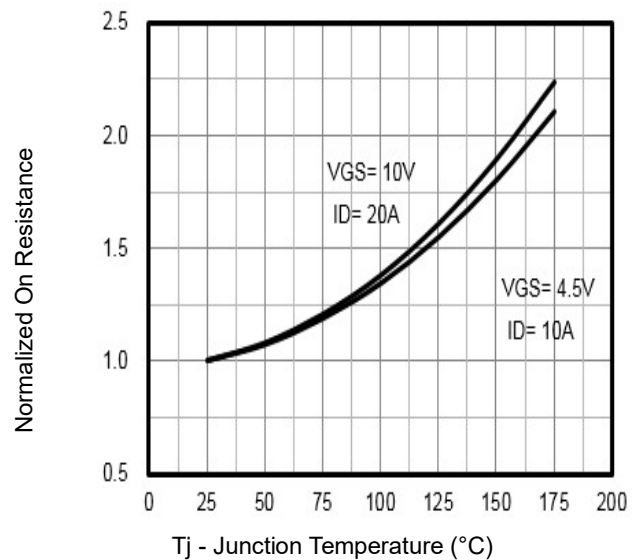


Fig4. Normalized On-Resistance Vs. T_j

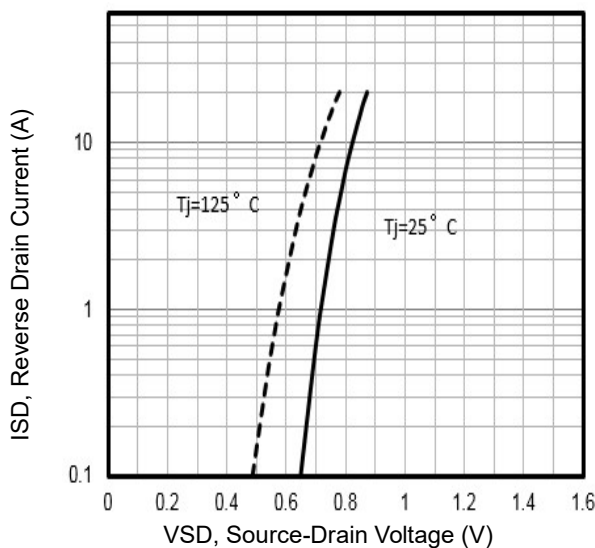


Fig5. Typical Source-Drain Diode Forward Voltage

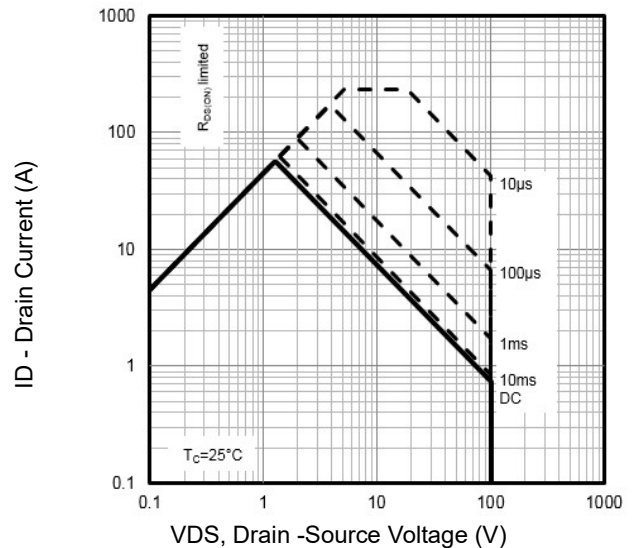
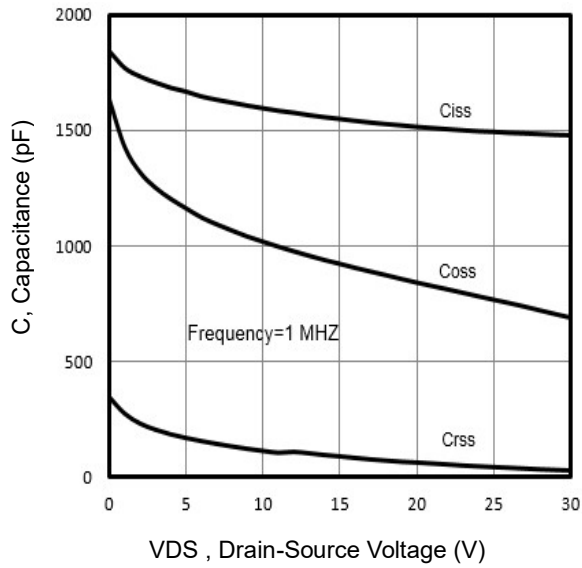
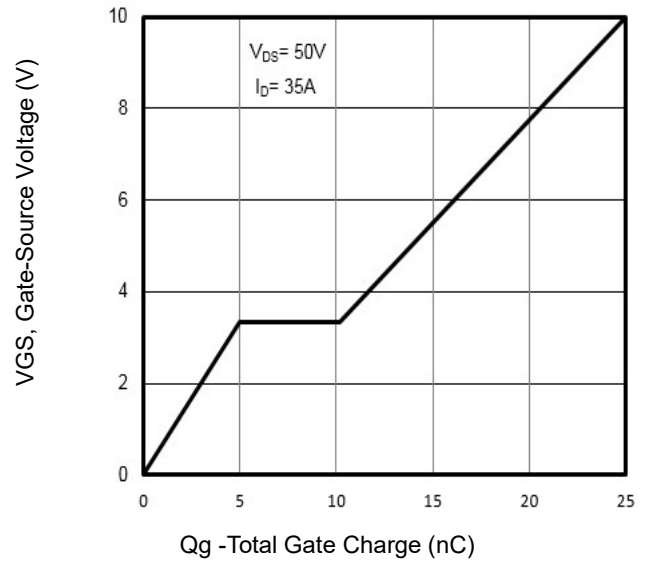
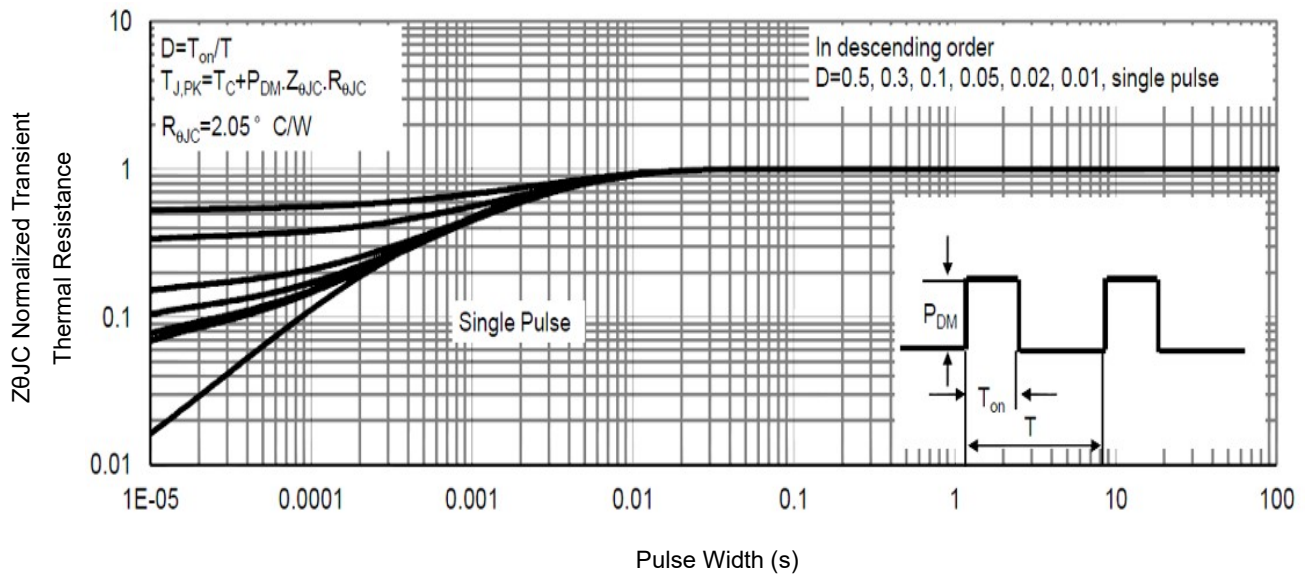
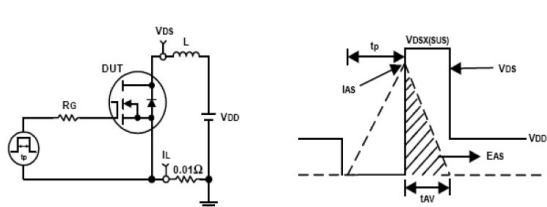
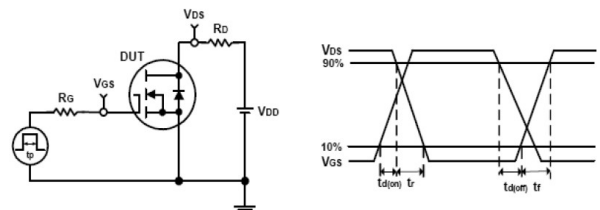
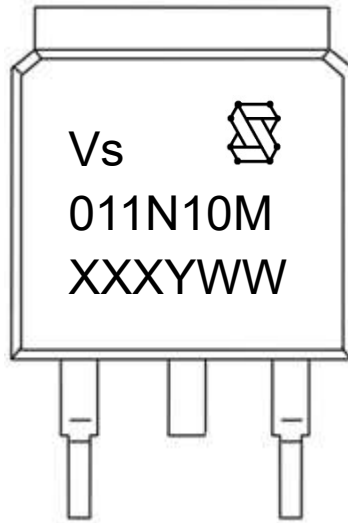


Fig6. Maximum Safe Operating Area

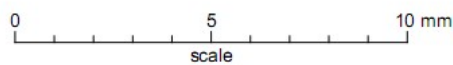
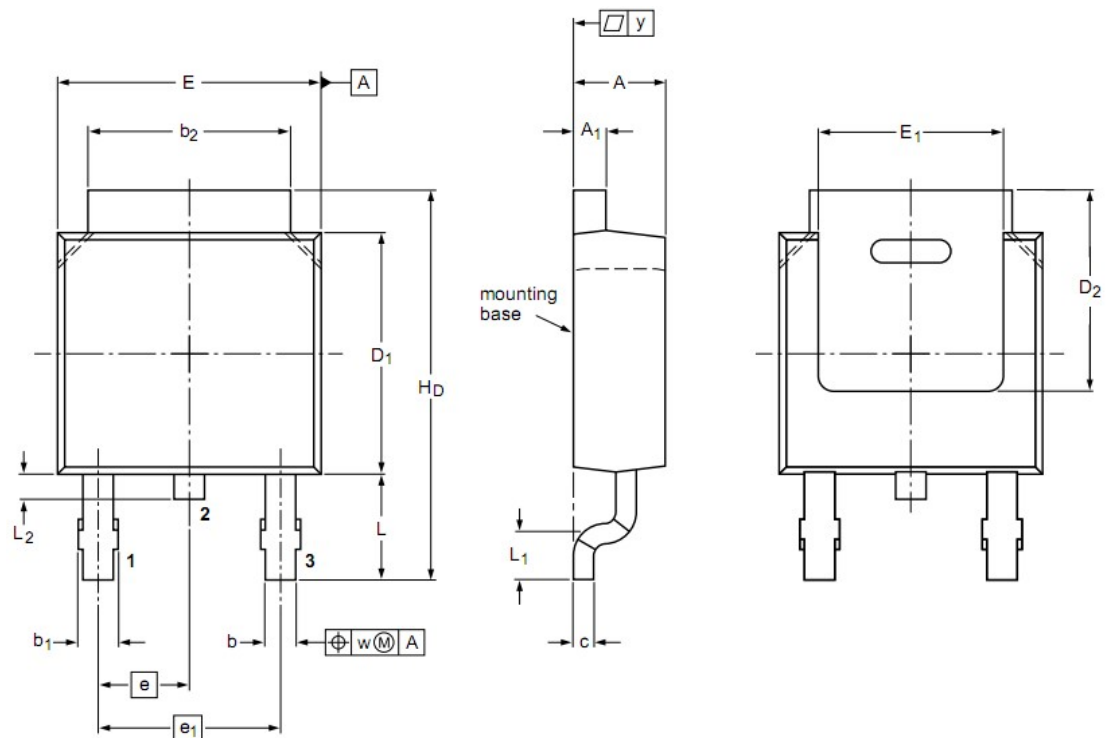
Typical Characteristics

Fig7. Typical Capacitance Vs. Drain-Source Voltage

Fig8. Typical Gate Charge Vs. Gate-Source Voltage

Fig9. Normalized Maximum Transient Thermal Impedance

Fig10. Unclamped Inductive Test Circuit and waveforms

Fig11. Switching Time Test Circuit and waveforms

Marking Information



- 1st line: Vergiga Code (Vs), Vergiga Logo
- 2nd line: Part Number (011N10M)
- 3rd line: Date code (XXXYWW)
 - XXX: Wafer Lot Number Code , code changed with Lot Number
 - Y: Year Code , refer to table below
 - WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-252 Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A₁	0.46	0.50	0.63
b	0.64	0.76	0.89
b₁	0.77	0.85	1.14
b₂	5.00	5.33	5.46
c	0.458	0.508	0.558
D₁	5.98	6.10	6.223
D₂	5.21	--	--
E	6.40	6.60	6.731
E₁	4.40	--	--
e	2.286 BSC		
e₁	--	4.57	--
H_D	9.40	10.00	10.40
L	2.743 REF		
L₁	1.40	1.52	1.77
L₂	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

Customer Service
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