

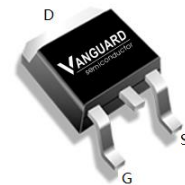
Features

- P-Channel, -5V Logic Level Control
- Low on-resistance RDS(on) @ VGS=-4.5 V
- Fast Switching and High efficiency
- Enhancement mode
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant


Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VSD050P10MS	TO-252	050P10M	2500PCS/Reel

V_{DS}	-100	V
$R_{DS(on),TYP} @ V_{GS}=-10\text{ V}$	47	m Ω
$R_{DS(on),TYP} @ V_{GS}=-4.5\text{ V}$	49	m Ω
I_D	-34	A

TO-252


Drain Pin 2



Gate Pin 1

Source Pin 3

Maximum ratings, at T_A=25 °C, unless otherwise specified

Symbol	Parameter	Rating	Unit	
$V_{(BR)DSS}$	Drain-Source breakdown voltage	-100	V	
V_{GS}	Gate-Source voltage	±20	V	
I_S	Diode continuous forward current	$T_C=25^\circ\text{C}$ -34	A	
I_D	Continuous drain current @ $V_{GS}=-10\text{V}$	$T_C=25^\circ\text{C}$	-34	A
		$T_C=100^\circ\text{C}$	-24	A
I_{DM}	Pulse drain current tested ①	$T_C=25^\circ\text{C}$	-136	A
I_{DSM}	Continuous drain current @ $V_{GS}=-10\text{V}$	$T_A=25^\circ\text{C}$	-3.8	A
		$T_A=70^\circ\text{C}$	-3	A
EAS	Avalanche energy, single pulsed ②	163	mJ	
P_D	Maximum power dissipation	$T_C=25^\circ\text{C}$	100	W
P_{DSM}	Maximum power dissipation ③	$T_A=25^\circ\text{C}$	1.3	W
T_{STG}, T_J	Storage and Junction Temperature Range	-55 to 175	°C	
Thermal Characteristics				
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.5	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	°C/W	



Typical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-100	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-100V, V _{GS} =0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T _J =125°C)	V _{DS} =-100V, V _{GS} =0V	--	--	-100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.3	-1.6	-2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =-10V, I _D =-20A	--	47	61	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =-4.5V, I _D =-10A	--	49	62	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =-30V, V _{GS} =0V, f=1MHz	4345	5110	5875	pF
C _{oss}	Output Capacitance		155	180	205	pF
C _{rss}	Reverse Transfer Capacitance		120	140	160	pF
Q _g (10V)	Total Gate Charge	V _{DS} =-50V, I _D =-20A, V _{GS} =-10V	--	85	--	nC
Q _g (4.5V)	Total Gate Charge		--	49	--	nC
Q _{gs}	Gate-Source Charge		--	17	--	nC
Q _{gd}	Gate-Drain Charge		--	20	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =-50V, I _D =-20A, R _G =3.0Ω, V _{GS} =-10V	--	19.5	--	ns
t _r	Turn-on Rise Time		--	22	--	ns
t _{d(off)}	Turn-Off Delay Time		--	85.5	--	ns
t _f	Turn-Off Fall Time		--	39	--	ns
Source- Drain Diode Characteristics @ T_J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =-20A, V _{GS} =0V	--	-0.9	-1.2	V
t _{rr}	Reverse Recovery Time	T _J =25°C, I _{SD} =-20A, V _{GS} =0V	--	29	--	ns
Q _{rr}	Reverse Recovery Charge	di/dt=-500A/μs	--	167	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = -20A, V_{GS} = -10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Characteristics

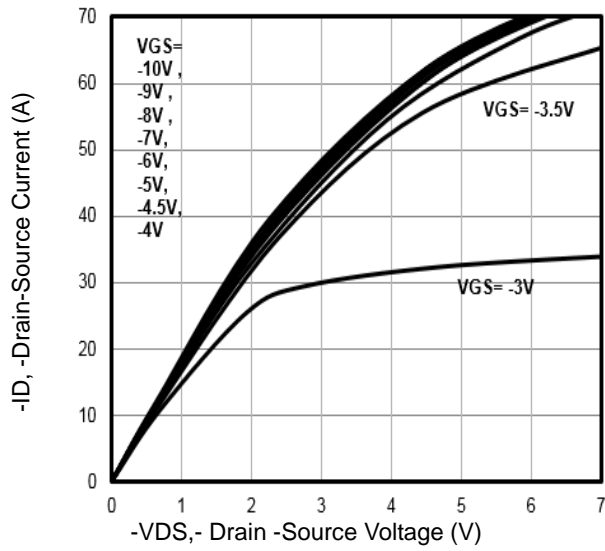


Fig1. Typical Output Characteristics

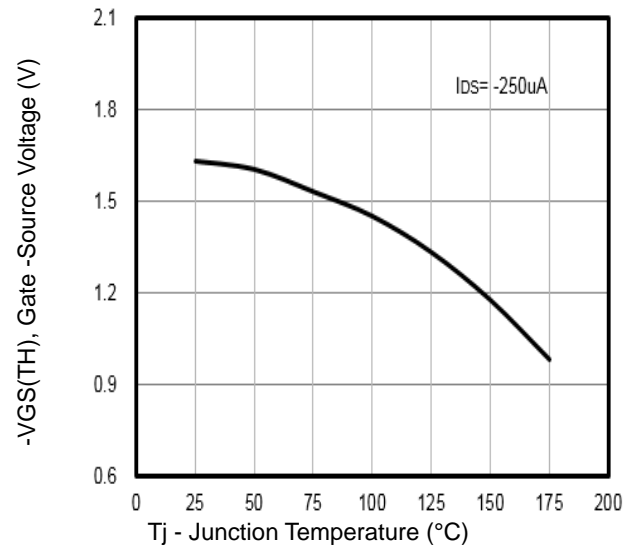


Fig2. $-V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

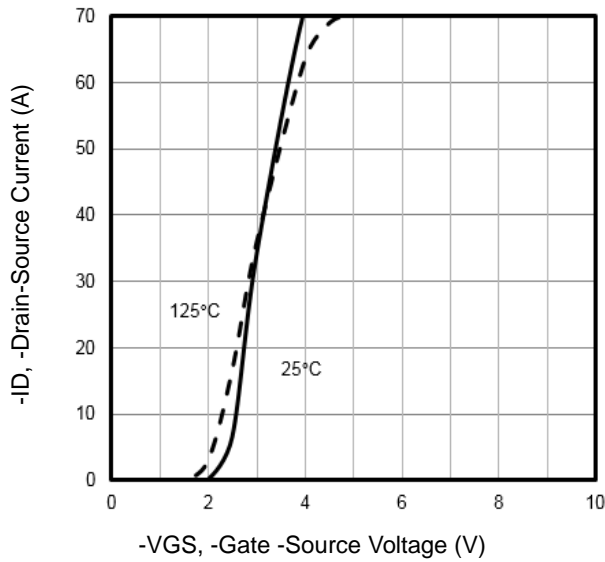


Fig3. Typical Transfer Characteristics

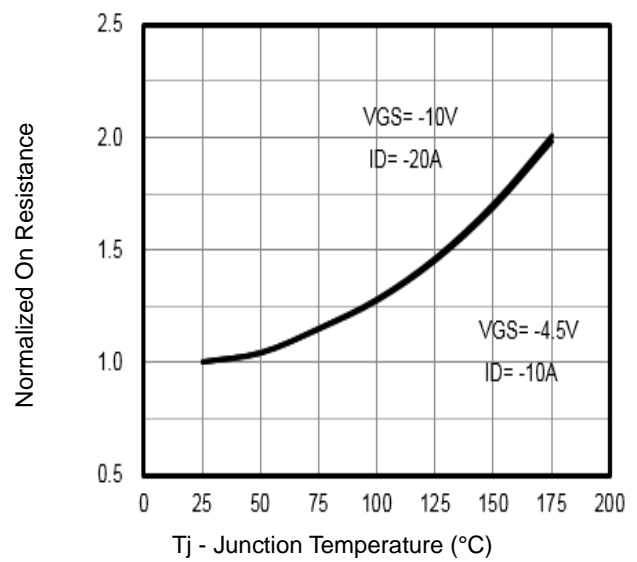


Fig4. Normalized On-Resistance Vs. T_j

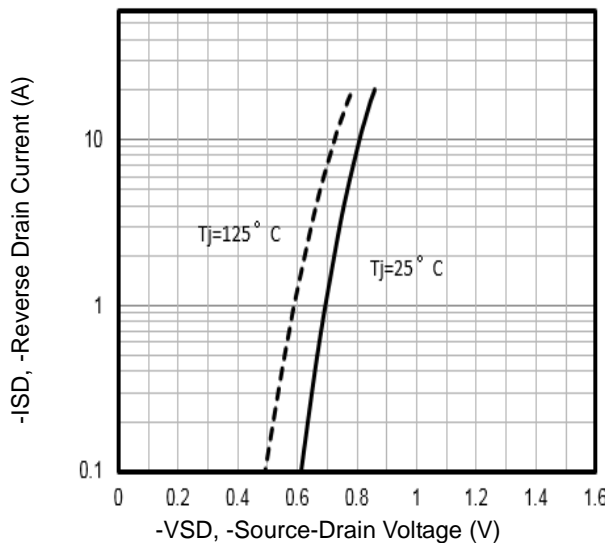


Fig5. Typical Source-Drain Diode Forward Voltage

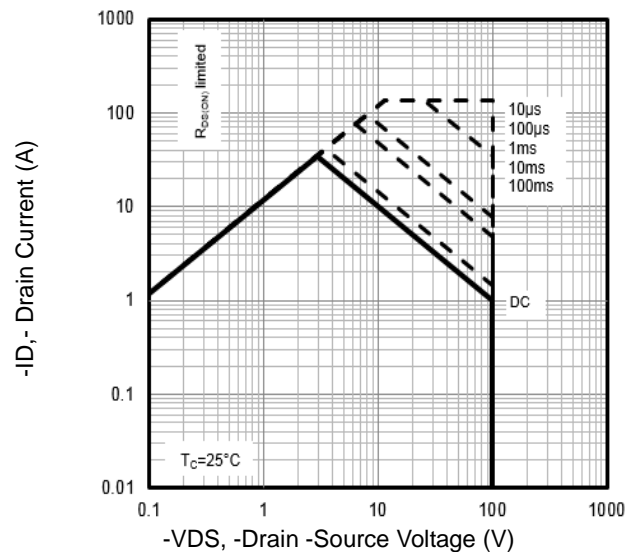


Fig6. Maximum Safe Operating Area

Typical Characteristics

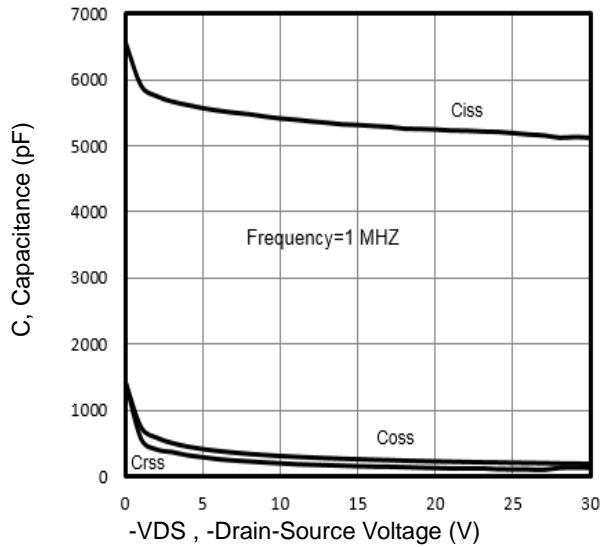


Fig7. Typical Capacitance Vs.Drain-Source Voltage

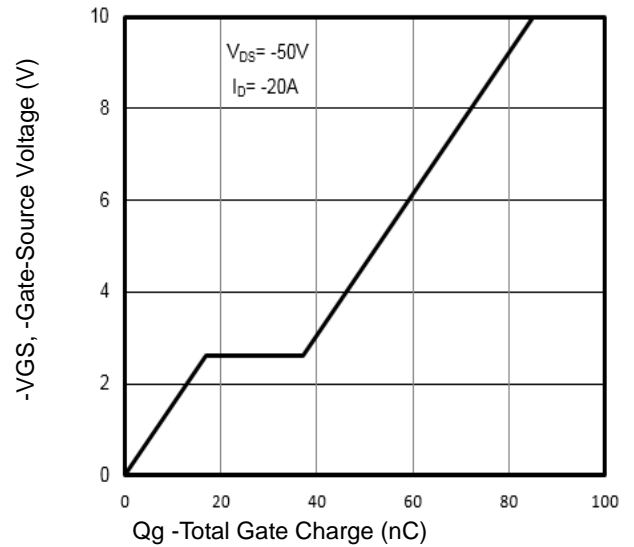


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

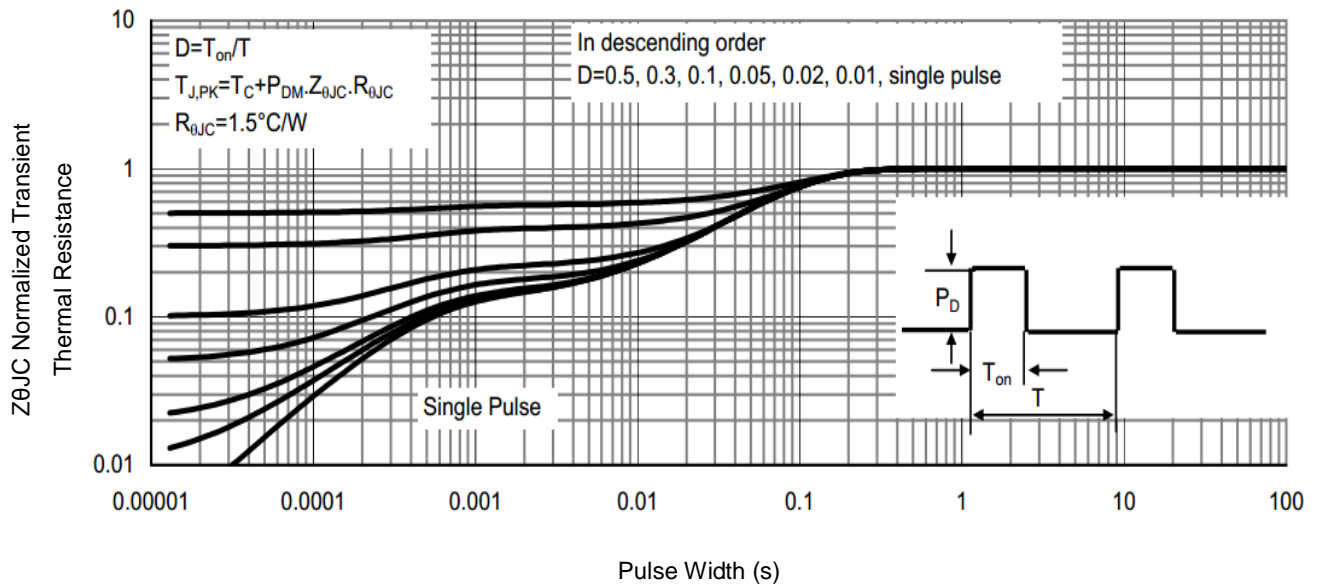


Fig9. Normalized Maximum Transient Thermal Impedance

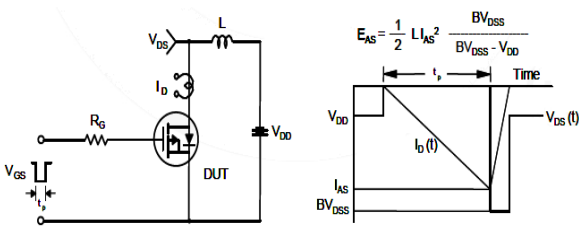


Fig10. Unclamped Inductive Test Circuit and Waveforms

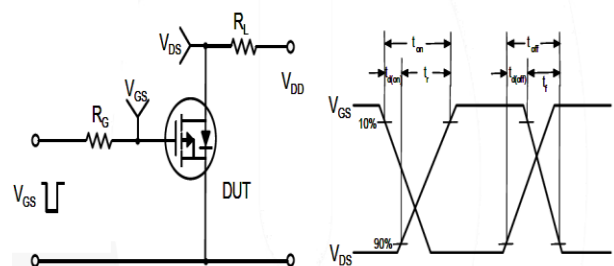
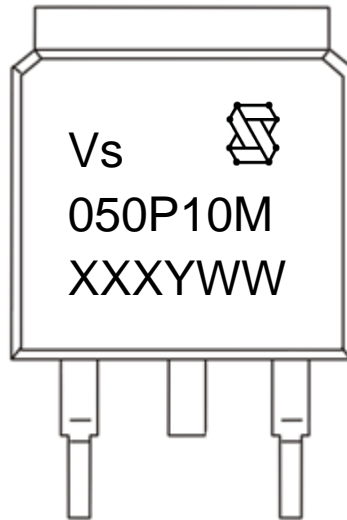


Fig11. Switching Time Test Circuit and waveforms



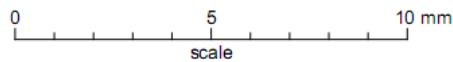
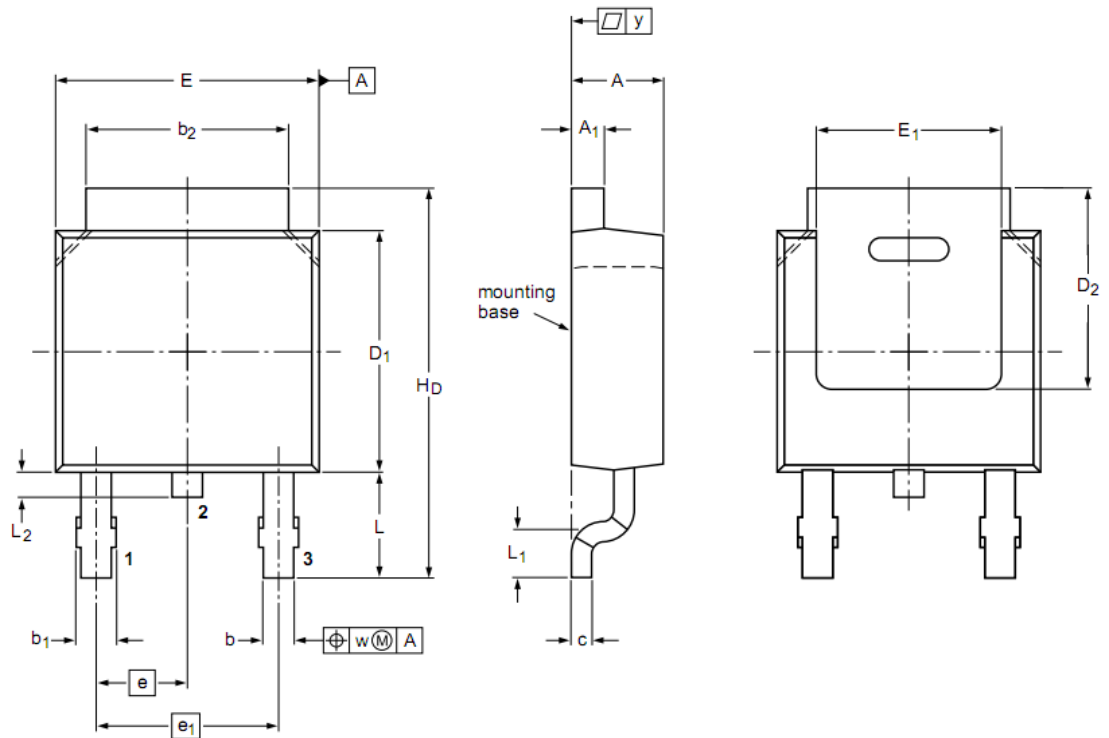
Marking Information



- 1st line: Vanguard Code (Vs), Vanguard Logo
2nd line: Part Number (050P10M)
3rd line: Date code (XXXYWW)
XXX: Wafer Lot Number
Y: Year Code, e.g. E means 2017
WW: Week Code



TO-252 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A ₁	0.46	0.50	0.63
b	0.64	0.76	0.89
b ₁	0.77	0.85	1.14
b ₂	5.00	5.33	5.46
c	0.458	0.508	0.558
D ₁	5.98	6.10	6.223
D ₂	5.21	--	--
E	6.40	6.60	6.731
E ₁	4.40	--	--
e	2.286 BSC		
e ₁	--	4.57	--
H _D	9.40	10.00	10.40
L	2.743 REF		
L ₁	1.40	1.52	1.77
L ₂	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

Customer Service

Sales and Service:

sales@vgsemi.com

Vanguard Semiconductor CO., LTD

TEL: (86-755) -26902410

FAX: (86-755) -26907027

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