

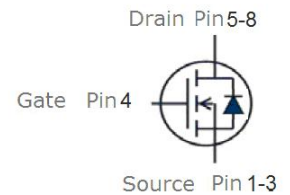
## Features

- Enhancement mode
- VitoMOS<sup>®</sup> II Technology
- Fast Switching and High Efficiency
- 100% Avalanche test

$V_{DS}$	65	V
$R_{DS(on),TYP@ V_{GS}=10V}$	8	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5V}$	13	mΩ
$I_D$	15	A



Part ID	Package Type	Marking	Packing
VSO009N06MS-GA	SOP8	009N06MG	3000PCS/Reel



## Maximum ratings, at $T_A = 25^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	65	V
$V_{GS}$	Gate-Source voltage	$\pm 20$	V
$I_S$	Diode continuous forward current	$T_A = 25^\circ\text{C}$	2.6 A
$I_D$	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ\text{C}$	15 A
		$T_A = 70^\circ\text{C}$	12 A
$I_{DM}$	Pulse drain current tested ①	$T_A = 25^\circ\text{C}$	60 A
$E_{AS}$	Avalanche energy, single pulsed ②	6.3	mJ
$P_D$	Maximum power dissipation	$T_A = 25^\circ\text{C}$	3.1 W
$T_{STG,TJ}$	Storage and junction temperature range	-55 to 150	$^\circ\text{C}$

## Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead	24	29	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	48	$^\circ\text{C/W}$

**Electrical Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics @ T<sub>j</sub>=25°C (unless otherwise stated)</b>						
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	65	--	--	V
IDSS	Zero Gate Voltage Drain Current(T <sub>j</sub> =25°C)	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	--	--	1	uA
	Zero Gate Voltage Drain Current(T <sub>j</sub> =125°C)	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	--	--	100	uA
IGSS	Gate-Body Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	--	--	±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.5	1.8	2.3	V
R <sub>DS(on)</sub>	Drain-Source On-State Resistance ③	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	--	8	11	mΩ
		T <sub>j</sub> =100°C	--	11	--	mΩ
R <sub>DS(on)</sub>	Drain-Source On-State Resistance ③	V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A	--	13	18	mΩ
<b>Dynamic Electrical Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHz	650	1295	2265	pF
C <sub>oss</sub>	Output Capacitance		250	500	875	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		10	20	50	pF
R <sub>g</sub>	Gate Resistance	f=1MHz	0.5	1.0	3	Ω
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>DS</sub> =30V, I <sub>D</sub> =10A, V <sub>GS</sub> =10V	--	19	33	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge		--	8.9	16	nC
Q <sub>gs</sub>	Gate-Source Charge		--	4.2	7.4	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	3	6	nC
<b>Switching Characteristics</b>						
T <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =30V, I <sub>D</sub> =10A, R <sub>G</sub> =3.0Ω, V <sub>GS</sub> =10V	--	7.4	--	ns
T <sub>r</sub>	Turn-on Rise Time		--	16	--	ns
T <sub>d(off)</sub>	Turn-Off Delay Time		--	17	--	ns
T <sub>f</sub>	Turn-Off Fall Time		--	5	--	ns
<b>Source- Drain Diode Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
V <sub>SD</sub>	Forward on voltage	I <sub>SD</sub> =10A, V <sub>GS</sub> =0V	--	0.8	1.2	V
T <sub>rr</sub>	Reverse Recovery Time	I <sub>sd</sub> =10A, V <sub>GS</sub> =0V	--	20	40	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	--	7.7	15	nC

**NOTE:**

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.5mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 5A, V<sub>GS</sub> = 10V. Part not recommended for use above this value
- ③ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

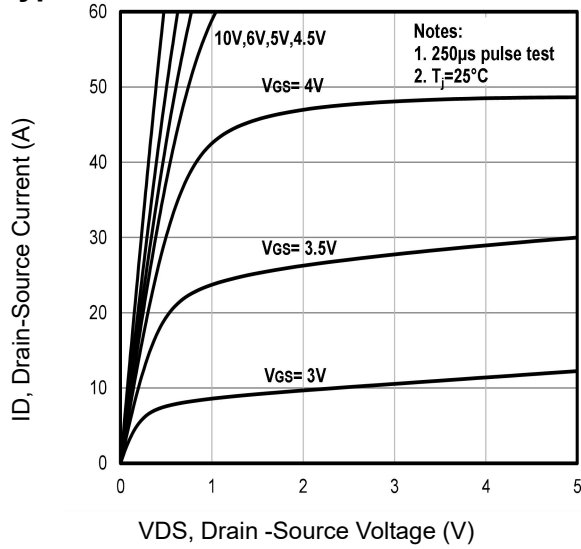


Fig1. Typical Output Characteristics

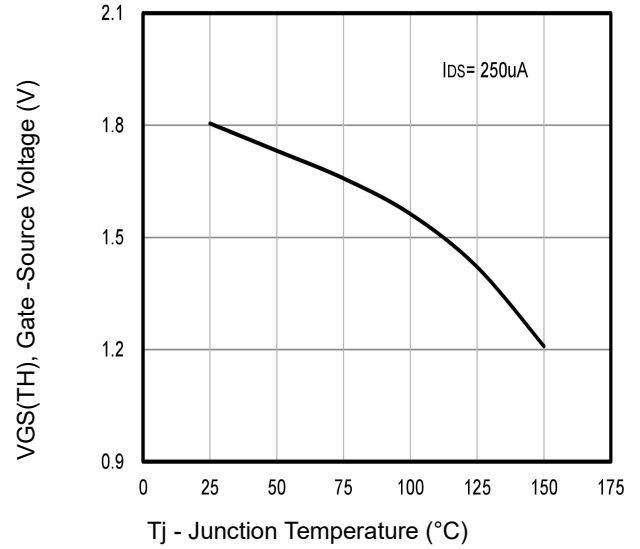


Fig2.  $V_{GS(TH)}$  Gate -Source Voltage Vs.  $T_j$

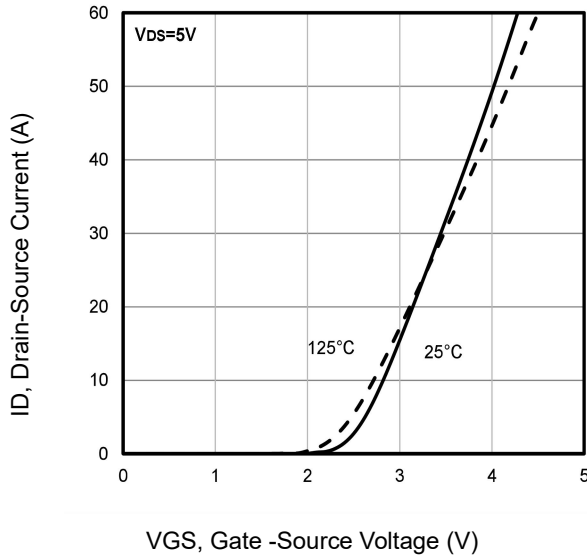


Fig3. Typical Transfer Characteristics

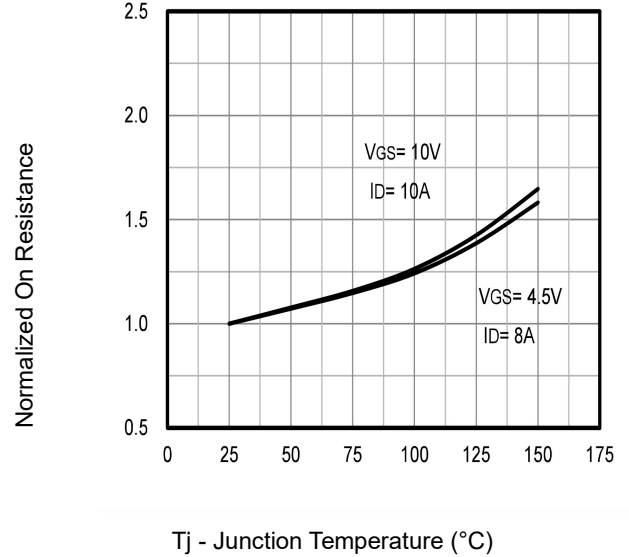


Fig4. Normalized On-Resistance Vs.  $T_j$

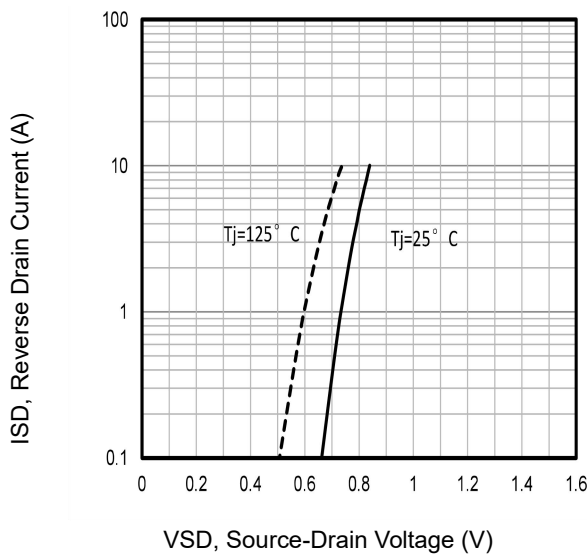


Fig5. Typical Source-Drain Diode Forward Voltage

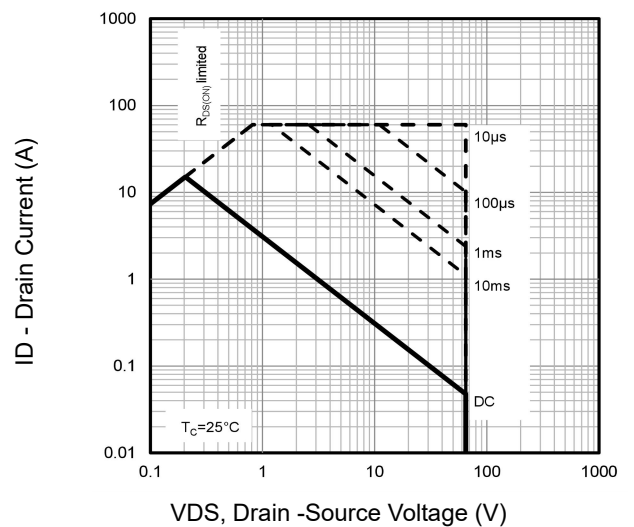


Fig6. Maximum Safe Operating Area

Typical Characteristics

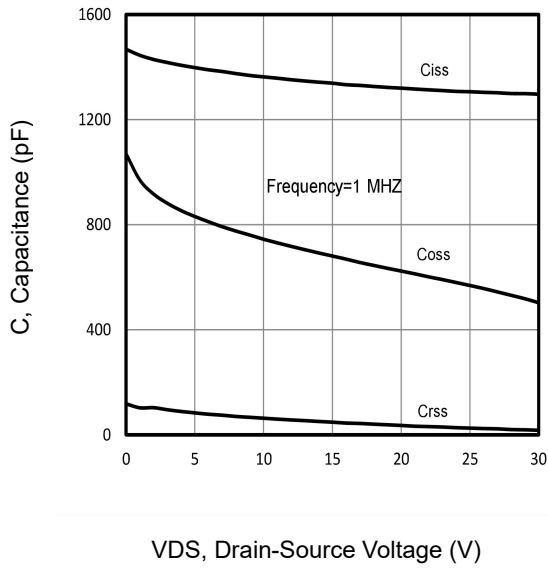


Fig7. Typical Capacitance Vs. Drain-Source Voltage

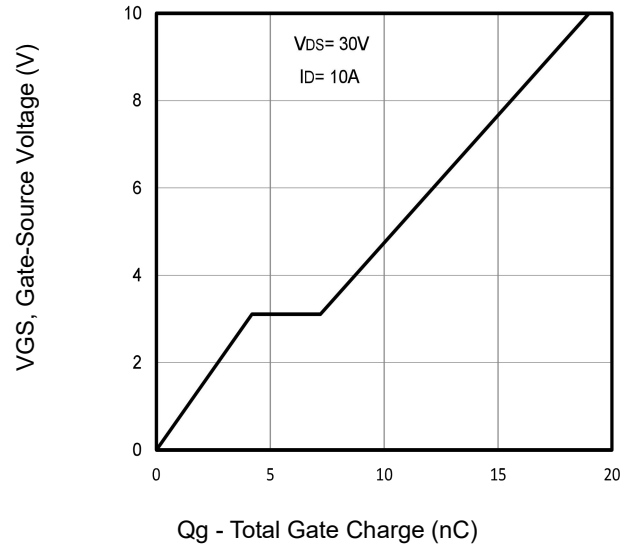


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

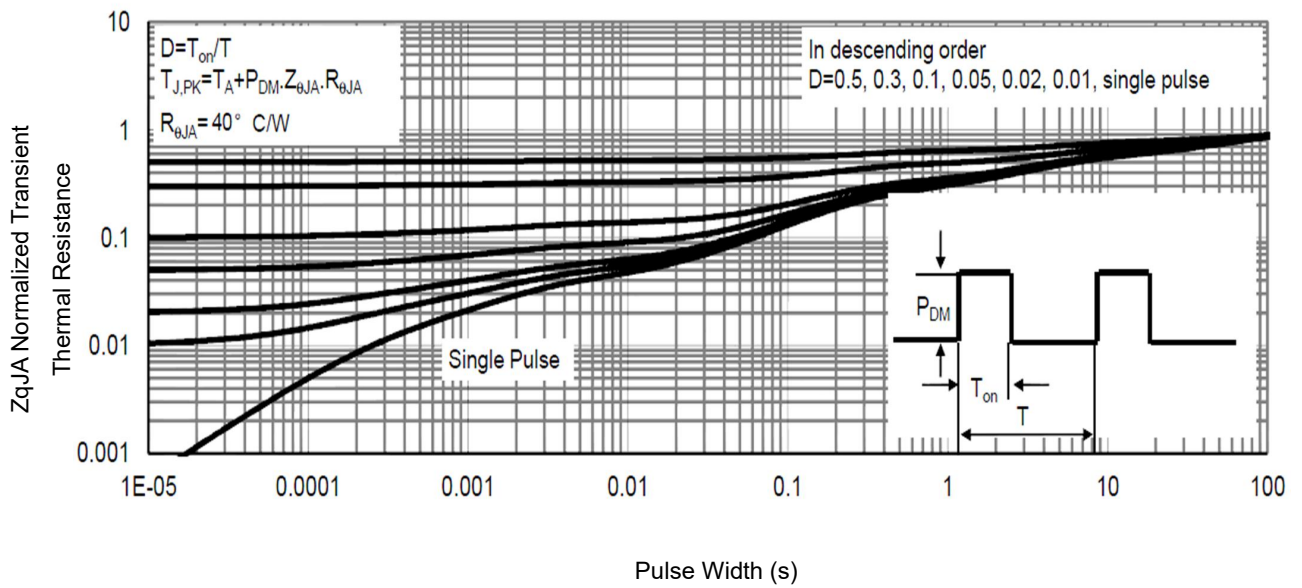


Fig9. Normalized Maximum Transient Thermal Impedance

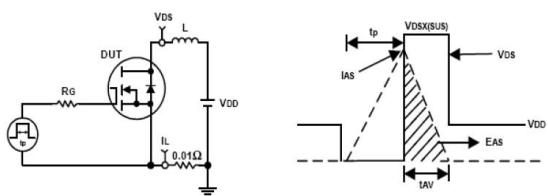


Fig10. Unclamped Inductive Test Circuit and waveforms

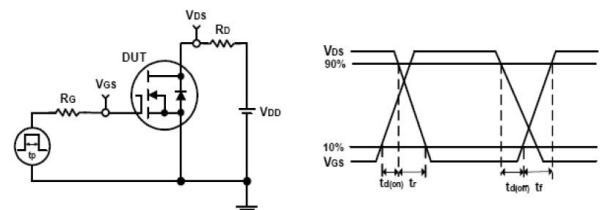
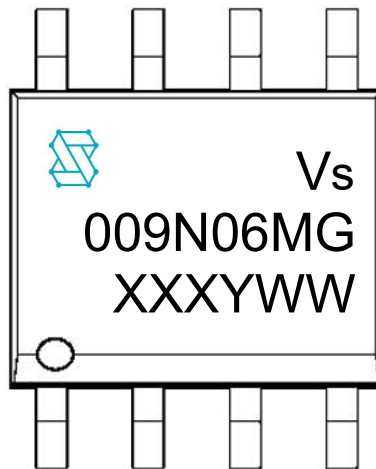


Fig11. Switching Time Test Circuit and waveforms

### Marking Information



1<sup>st</sup> line: Vanguard Code (Vs), Vanguard Logo

2<sup>nd</sup> line: Part Number (009N06MG)

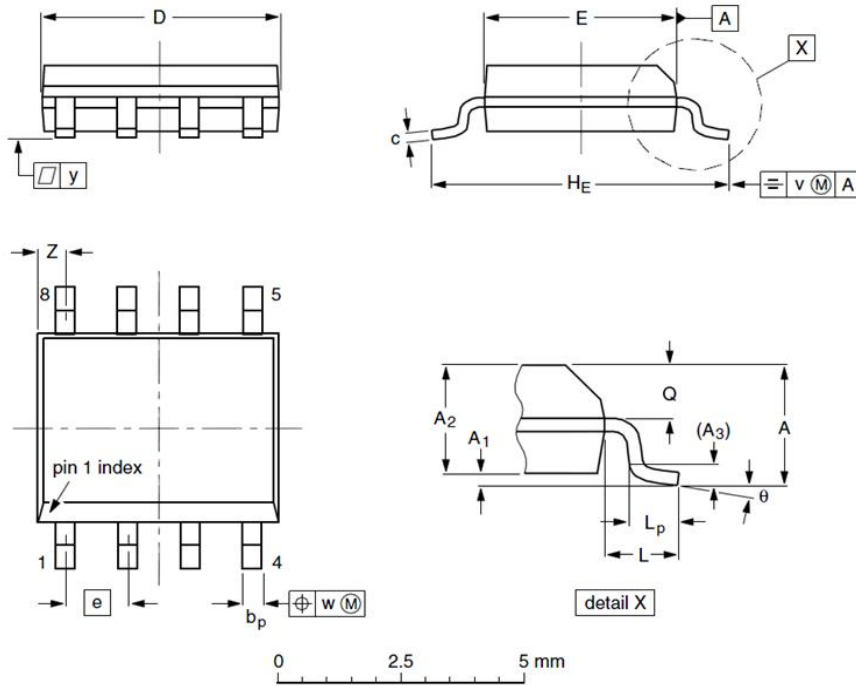
3<sup>rd</sup> line: Date code (XXXYWW)

XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code , refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

**SOP8 Package Outline Data**


Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A <sub>1</sub>	0.10	0.18	0.25
A <sub>2</sub>	1.25	1.35	1.50
A <sub>3</sub>	--	0.25	--
b <sub>p</sub>	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H <sub>E</sub>	5.80	6.00	6.20
L	--	1.05	--
L <sub>p</sub>	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

**Notes:**

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "b<sub>p</sub>" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "b<sub>p</sub>" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

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[C3M0021120D](#) [DMN6022SSD-13](#) [DMN13M9UCA6-7](#) [MCQ4828A-TP](#)