

Features

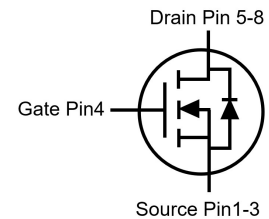
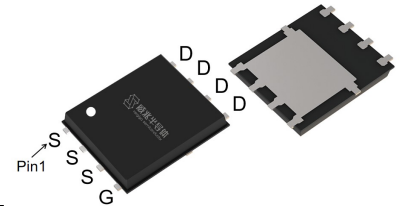
- Enhancement mode
- Very low on-resistance
- VitoMOS[®] II Technology
- Fast Switching and High efficiency
- 100% Avalanche test
- 100% 1x reflow implemented in semiconductor assembly process


Halogen-Free

Part ID	Package Type	Marking	Packing
VSP004N10MS-K	PDFN5060X	004N10MG	3000PCS/Reel

V_{DS}	100	V
$R_{DS(on),TYP@ V_{GS}=10V}$	5	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5V}$	6.9	mΩ
$I_D(\text{Silicon Limited})$	90	A
$I_D(\text{Package Limited})$	50	A

PDFN5060X



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit	
$V_{(BR)DSS}$	Drain-Source breakdown voltage	100	V	
V_{GS}	Gate-Source voltage	± 20	V	
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	90	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 25^\circ\text{C}$	90	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 100^\circ\text{C}$	57	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Package limited)	$T_C = 25^\circ\text{C}$	50	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	360	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ\text{C}$	22	A
		$T_A = 70^\circ\text{C}$	17	A
E_{AS}	Avalanche energy, single pulsed ②	36	mJ	
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	74	W
		$T_C = 100^\circ\text{C}$	29	W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	4.2	W
		$T_A = 70^\circ\text{C}$	2.7	W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 150	$^\circ\text{C}$	

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.7	2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	30	36	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _J =25°C)	V _{DS} =100V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _J =125°C)	V _{DS} =100V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.4	1.8	2.3	V
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =40A	--	5	6.5	mΩ
		(T _J =100°C)	--	6.3	--	mΩ
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =4.5V, I _D =20A	--	6.9	9	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	2325	3100	4125	pF
C _{oss}	Output Capacitance		1060	1415	1880	pF
C _{rss}	Reverse Transfer Capacitance		20	35	50	pF
R _g	Gate Resistance	f=1MHz	0.2	0.5	3	Ω
Q _{g(10V)}	Total Gate Charge	V _{DS} =50V, I _D =40A, V _{GS} =10V	--	49	65	nC
Q _{g(4.5V)}	Total Gate Charge		--	25	33	nC
Q _{gs}	Gate-Source Charge		--	9.8	13	nC
Q _{gd}	Gate-Drain Charge		--	9.5	14	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =50V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	9.8	--	ns
T _r	Turn-on Rise Time		--	30	--	ns
T _{d(off)}	Turn-Off Delay Time		--	36	--	ns
T _f	Turn-Off Fall Time		--	36	--	ns
Source- Drain Diode Characteristics@ T_J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A, V _{GS} =0V	--	0.9	1.2	V
T _{rr}	Reverse Recovery Time	I _{sd} =40A, V _{GS} =0V	--	48	96	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	44	88	nC

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 12A, V_{GS} = 10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

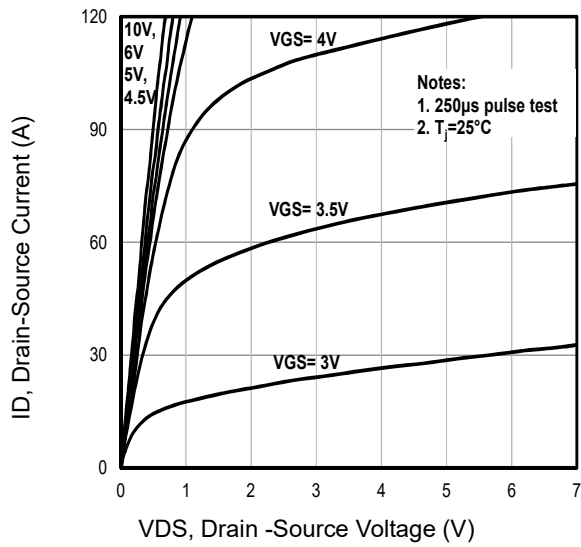


Fig1. Typical Output Characteristics

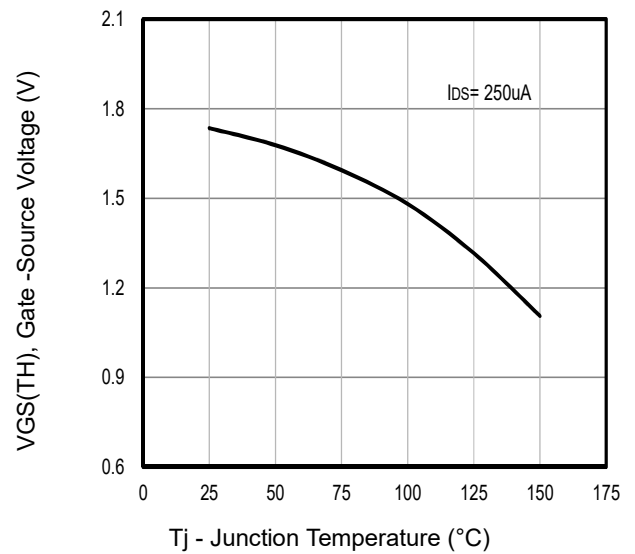


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

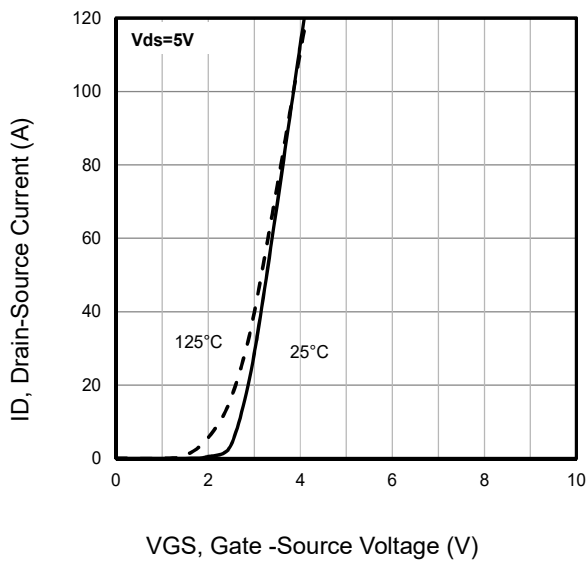


Fig3. Typical Transfer Characteristics

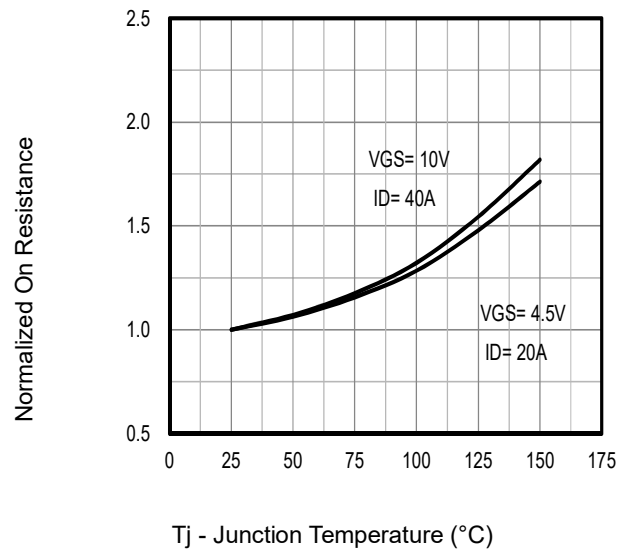


Fig4. Normalized On-Resistance Vs. T_j

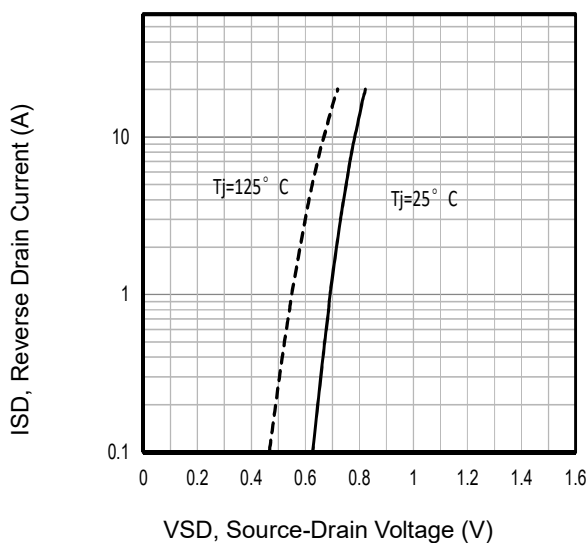


Fig5. Typical Source-Drain Diode Forward Voltage

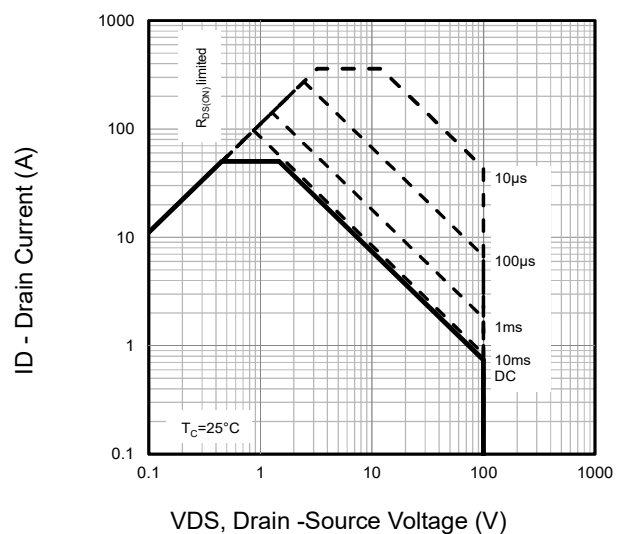


Fig6. Maximum Safe Operating Area

Typical Characteristics

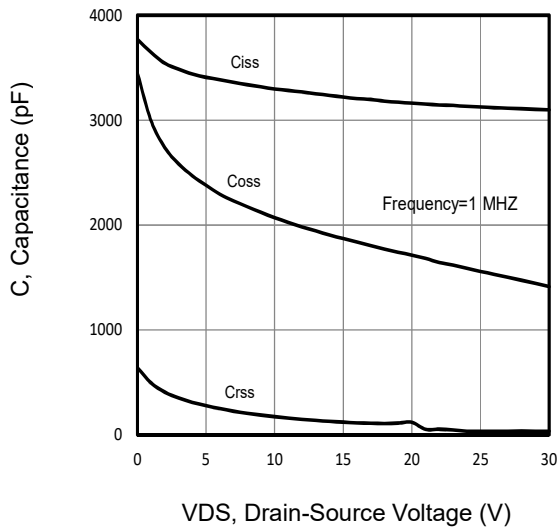


Fig7. Typical Capacitance Vs. Drain-Source Voltage

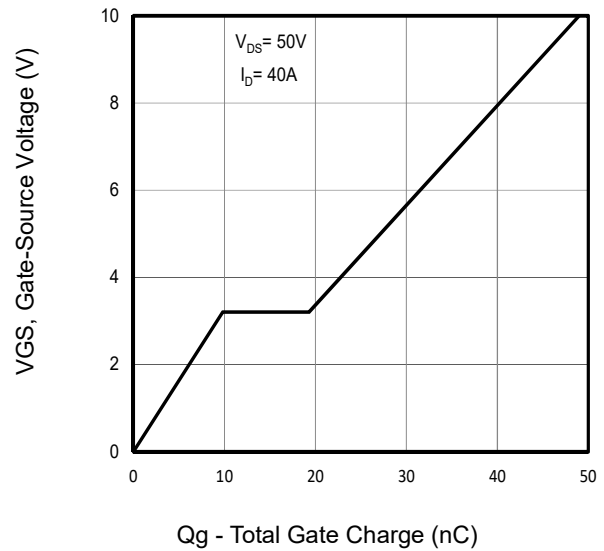


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

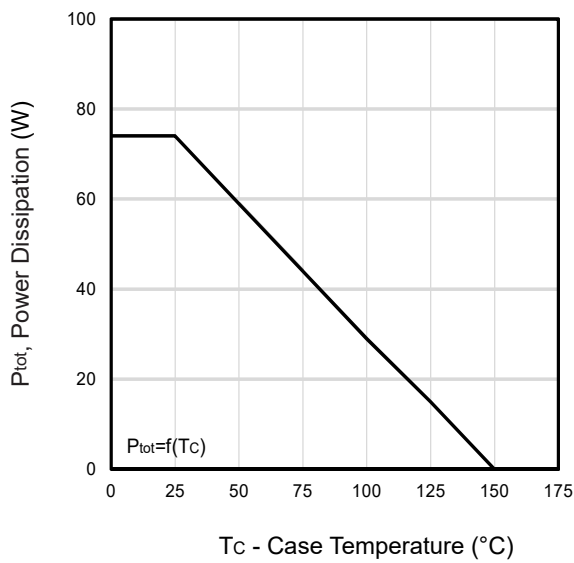


Fig9. Power Dissipation Vs. Case Temperature

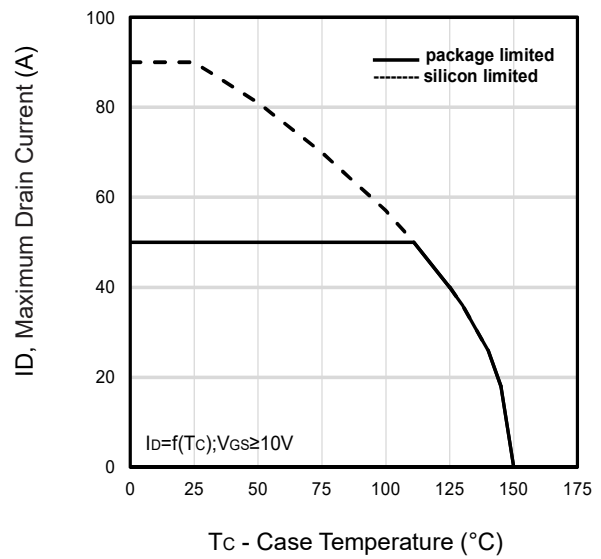


Fig10. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

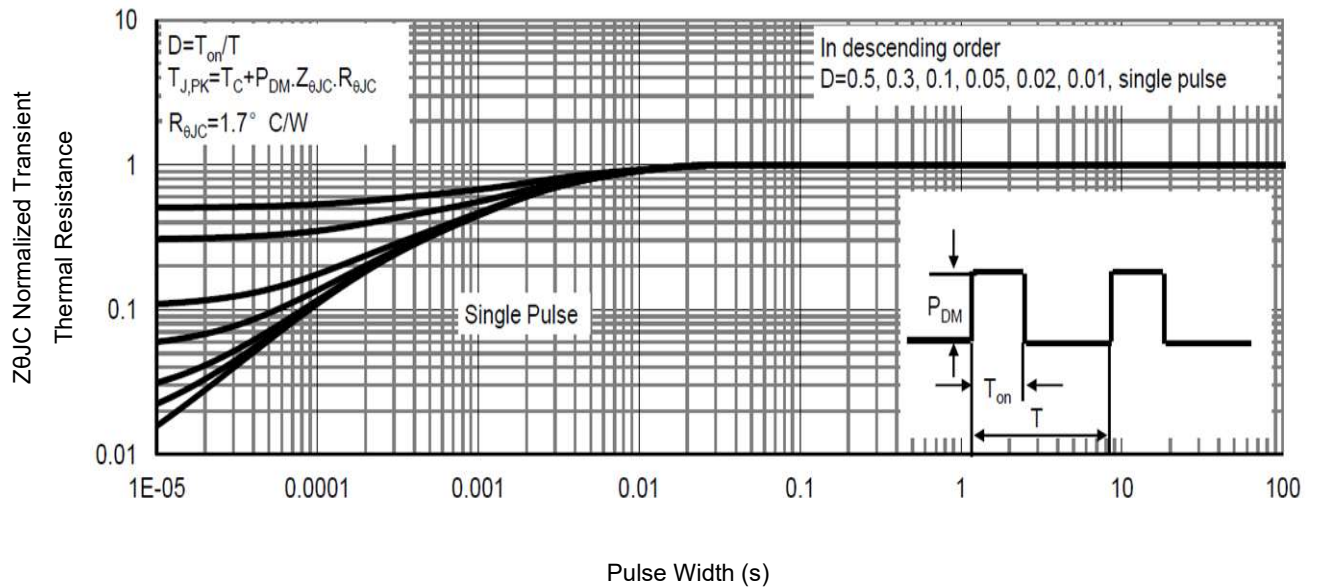


Fig11 . Normalized Maximum Transient Thermal Impedance

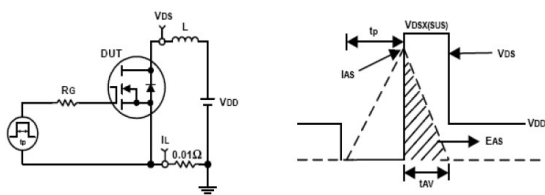


Fig12. Unclamped Inductive Test Circuit and waveforms

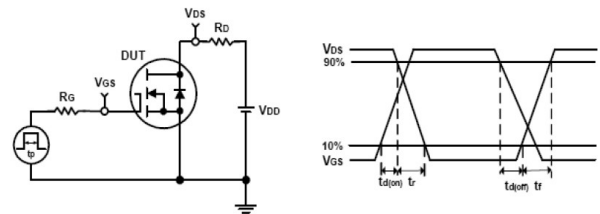
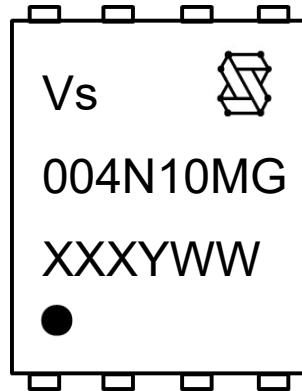


Fig13. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (004N10MG)

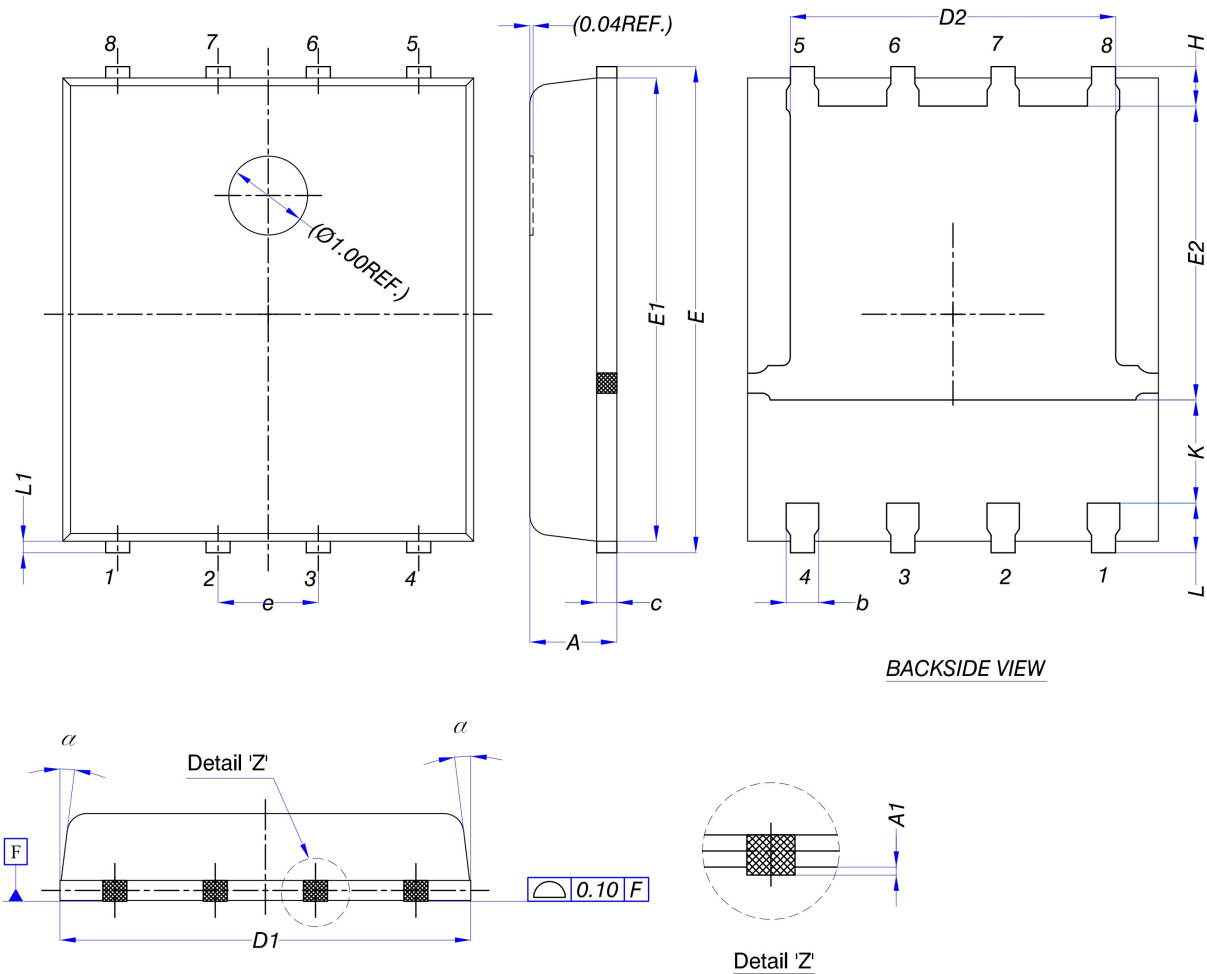
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN5060X Package Outline Data


Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	1.00	1.10	1.20
A1	0.00	--	0.05
b	0.30	0.40	0.50
c	0.20	0.25	0.30
D1	5.00	5.20	5.40
D2	3.80	4.10	4.25
E	5.95	6.15	6.35
E1	5.66	5.86	6.06
E2	3.52	3.72	3.92
e	1.27 BSC		
H	0.40	0.50	0.60
K	1.10	--	--
L	0.50	0.60	0.70
L1	0.08	0.15	0.22
α	0°	--	12°

Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service
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[TK31J60W5,S1VQ\(O](#) [2SK2614\(TE16L1,Q\)](#) [DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [FCAB21350L1](#) [P85W28HP2F-7071](#) [DMN1053UCP4-7](#)
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[IPS60R360PFD7SAKMA1](#) [IPS60R600PFD7SAKMA1](#)