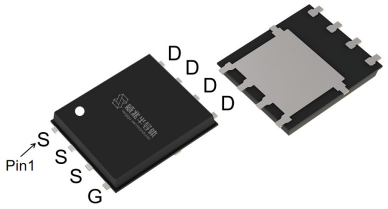
| | | |
|---|---|---|
| $V_{DS}$ | 100 | V |
| $R_{DS(on),TYP}$@ $V_{GS}$=10 V | 9.5 | mΩ |
| $R_{DS(on),TYP}$@ $V_{GS}$=4.5 V | 13 | mΩ |
| $I_D$ | 50 | A |

## Features

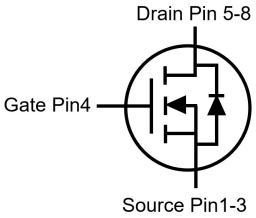
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}$=4.5 V
- VitoMOS® Ⅱ Technology
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

Pb-Free RoHS HF Halogen-Free

**PDFN5x6**




| Part ID | Package Type | Marking | Packing |
|---|---|---|---|
| VSP011N10MS-G | PDFN5x6 | 011N10MG | 3000PCS/Reel |




## Maximum ratings, at $T_A$ =25°C, unless otherwise specified

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source breakdown voltage | | 100 | V |
| VGS | Gate-Source voltage | | ±20 | V |
| $I_S$ | Diode continuous forward current | $T_C$=25°C | 50 | A |
| $I_D$ | Continuous drain current @VGS=10V | $T_C$=25°C | 50 | A |
| | | $T_C$=100°C | 32 | A |
| $I_{DM}$ | Pulse drain current tested ① | $T_C$=25°C | 200 | A |
| $I_{DSM}$ | Continuous drain current @VGS=10V | $T_A$=25°C | 15 | A |
| | | $T_A$=70°C | 12 | A |
| EAS | Avalanche energy, single pulsed ② | | 25 | mJ |
| $P_D$ | Maximum power dissipation | $T_C$=25°C | 44 | W |
| $P_{DSM}$ | Maximum power dissipation ③ | $T_A$=25°C | 4.2 | W |
| $T_{STG}$, $T_J$ | Storage and Junction Temperature Range | | -55 to 150 | °C |

## Thermal Characteristics

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 2.85 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 30 | °C/W |

## Electrical Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Electrical Characteristics @ $T_j$=25°C (unless otherwise stated)** | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=250μA | 100 | -- | -- | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=100V,$V_{GS}$=0V | -- | -- | 1 | μA |
| | Zero Gate Voltage Drain Current($T_j$=125℃) | $V_{DS}$=100V,$V_{GS}$=0V | -- | -- | 100 | μA |
| $I_{GSS}$ | Gate-Body Leakage Current | $V_{GS}$=±20V,$V_{DS}$=0V | -- | -- | ±100 | nA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 1.4 | 1.7 | 2.5 | V |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance④ | $V_{GS}$=10V, $I_D$=30A | -- | 9.5 | 13 | mΩ |
| | | $T_j$=100℃ | -- | 12 | -- | mΩ |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance④ | $V_{GS}$=4.5V, $I_D$=10A | -- | 13 | 16 | mΩ |
| **Dynamic Electrical Characteristics @ $T_j$ = 25°C (unless otherwise stated)** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=30V,$V_{GS}$=0V, f=1MHz | 1190 | 1400 | 1610 | pF |
| $C_{oss}$ | Output Capacitance | | 560 | 660 | 760 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 15 | 25 | 35 | pF |
| $R_g$ | Gate Resistance | f=1MHz | -- | 1 | -- | Ω |
| $Q_g$ (10V) | Total Gate Charge | $V_{DS}$=50V,$I_D$=30A, $V_{GS}$=10V | -- | 22 | -- | nC |
| $Q_g$ (4.5V) | Total Gate Charge | | -- | 11 | -- | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 4.5 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 4.7 | -- | nC |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}$=50V, $I_D$=30A, $R_G$=3Ω, $V_{GS}$=10V | -- | 7.4 | -- | ns |
| $t_r$ | Turn-on Rise Time | | -- | 29 | -- | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 19 | -- | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 5.4 | -- | ns |
| **Source- Drain Diode Characteristics@ $T_j$ = 25°C (unless otherwise stated)** | | | | | | |
| $V_{SD}$ | Forward on voltage | $I_{SD}$=30A,$V_{GS}$=0V | -- | 0.9 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $T_j$=25℃,$I_{sd}$=30A, $V_{GS}$=0V di/dt=100A/μs | -- | 50 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 50 | -- | nC |

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.5mH, $R_G$ = 25Ω, $I_{AS}$ = 10A, $V_{GS}$ =10V. Part not recommended for use above this value

③ The power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle≤ 2%.

## Typical Characteristics

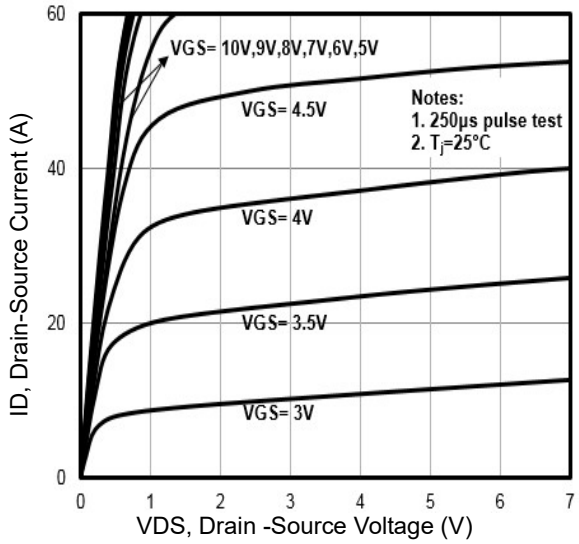



**Fig1.** Typical Output Characteristics

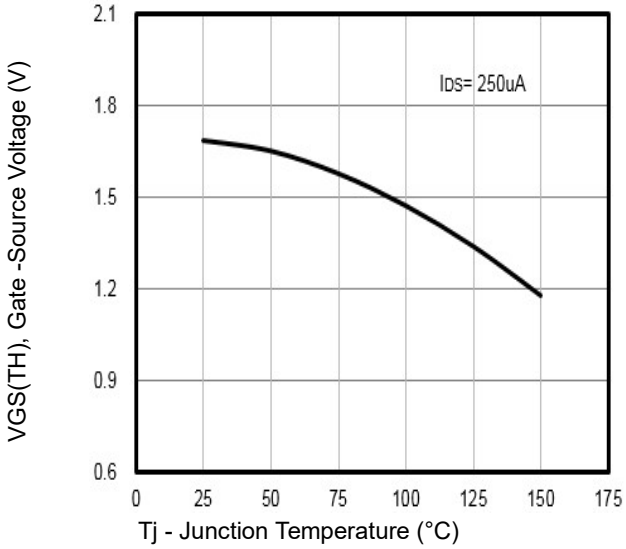



**Fig2.** $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

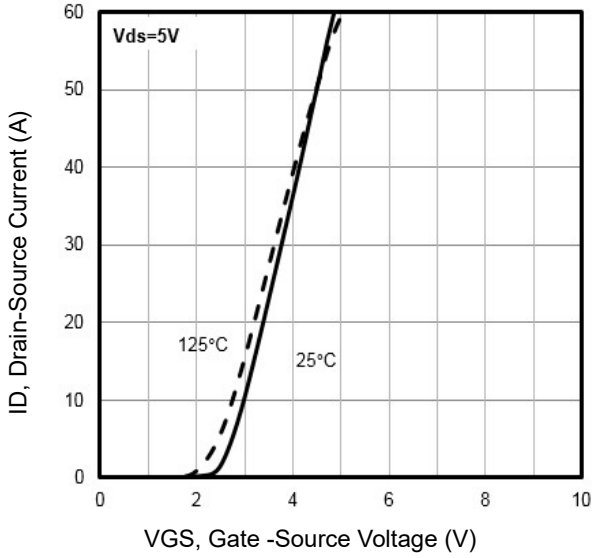



**Fig3.** Typical Transfer Characteristics

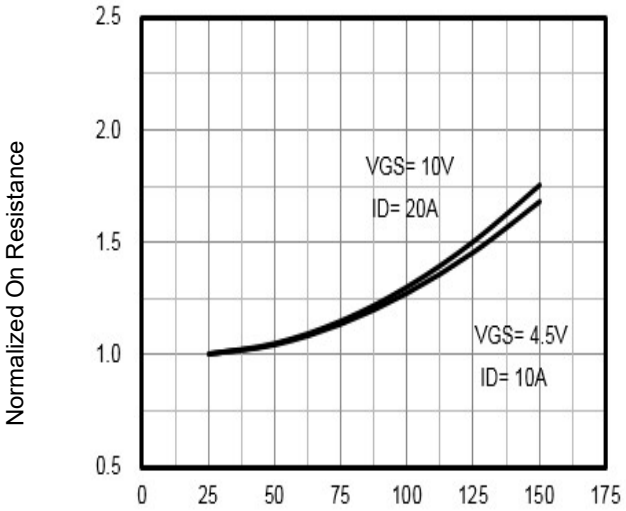



**Fig4.** Normalized On-Resistance Vs. Tj

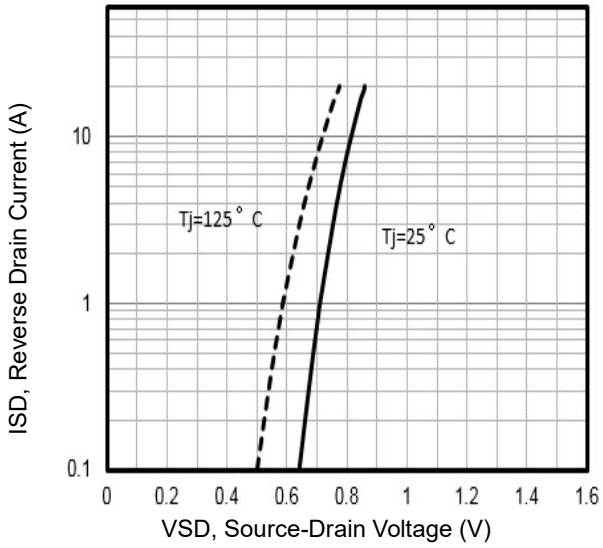



**Fig5.** Typical Source-Drain Diode Forward Voltage

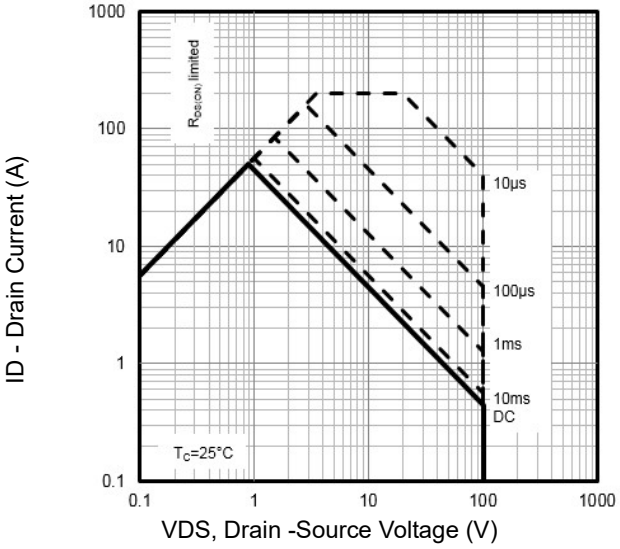



**Fig6.** Maximum Safe Operating Area

## Typical Characteristics

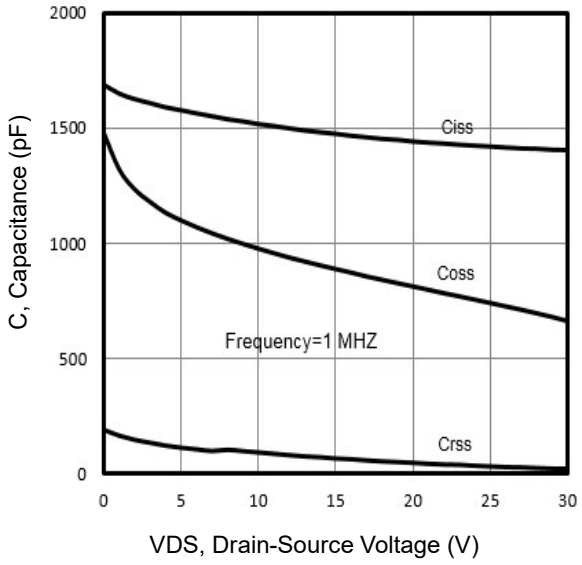



**Fig7.** Typical Capacitance Vs. Drain-Source Voltage

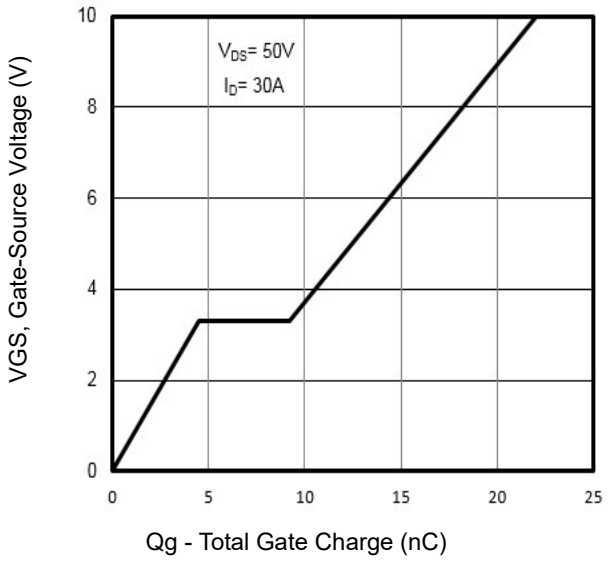



**Fig8.** Typical Gate Charge Vs. Gate-Source Voltage

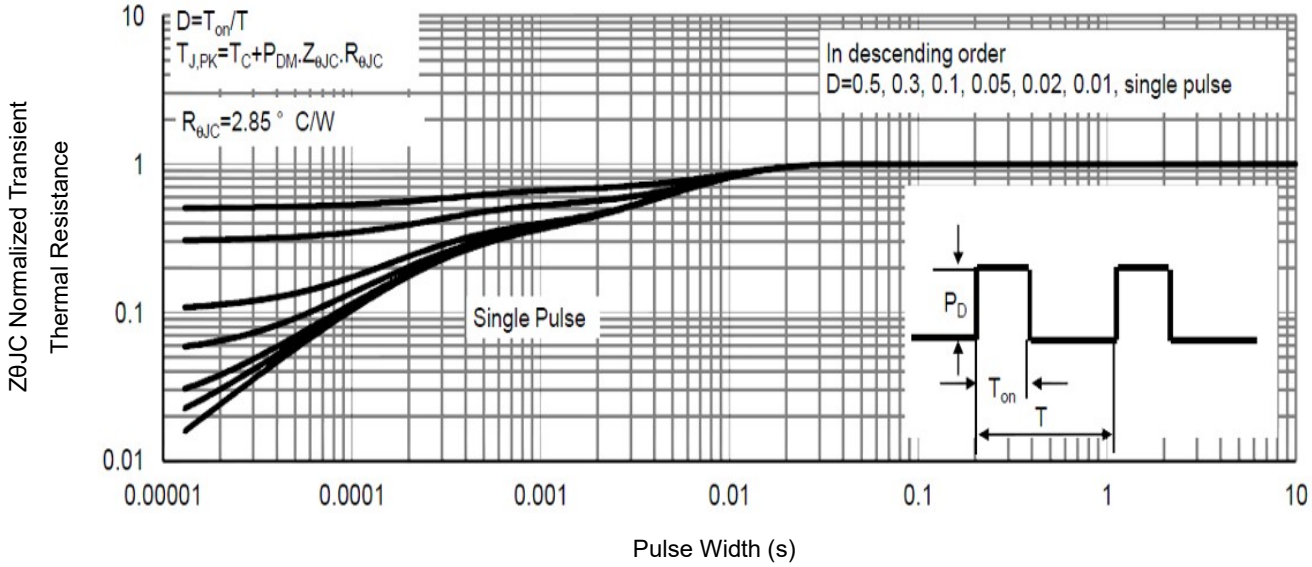



**Fig9.** Normalized Maximum Transient Thermal Impedance

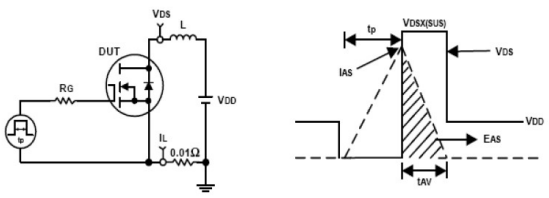



**Fig10.** Unclamped Inductive Test Circuit and waveforms

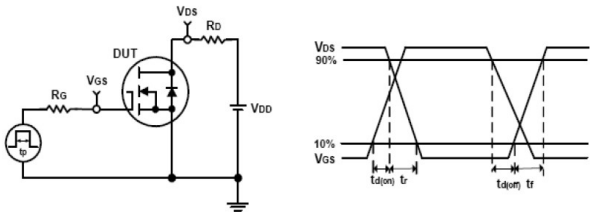
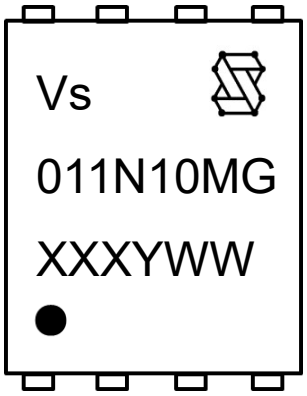



**Fig11.** Switching Time Test Circuit and waveforms

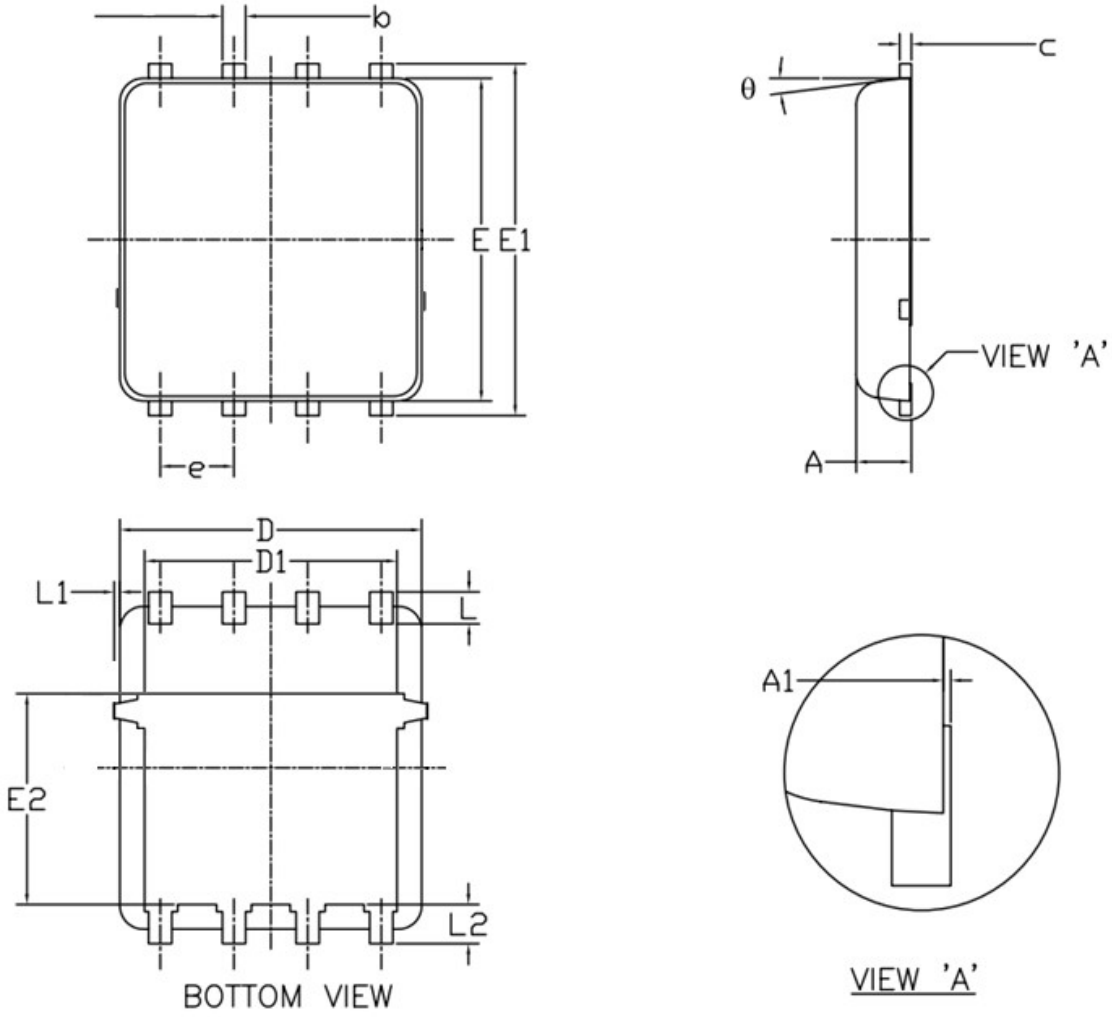
## Marking Information




1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（011N10M）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code, code changed with Lot Number
Y: Year Code，refer to table below
WW: Week Code (01 to 53)

| Code | C | D | E | F | G | H | J | K | L | M | N | P | Q | R | S | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Year | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 |

## PDFN5x6 Package Outline Data




| Symbol | DIMENSIONS ( unit : mm ) | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.90 | 1.00 | 1.20 |
| A1 | 0.00 | -- | 0.05 |
| b | 0.30 | 0.40 | 0.51 |
| c | 0.20 | 0.25 | 0.33 |
| D | 4.80 | 4.90 | 5.40 |
| D1 | 3.61 | 4.00 | 4.25 |
| E | 5.65 | 5.80 | 6.06 |
| E1 | 5.90 | 6.10 | 6.35 |
| E2 | 3.38 | 3.58 | 3.92 |
| e | 1.27 BSC | | |
| L | 0.51 | 0.61 | 0.71 |
| L1 | -- | -- | 0.15 |
| L2 | 0.41 | 0.51 | 0.61 |
| θ | 0° | -- | 12° |

Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D" and "E" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D" and "E" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

## Customer Service

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sales@vgsemi.com

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