



VL-FS-MGLS240128Z-05 REV. A
(MGLS240128Z-HT-HV-G-LED03G-IC-T6A39/40-5V VLED)

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PAGE 1 OF 13

DOCUMENT NUMBER AND REVISION
VL-FS-MGLS240128Z-05 REV. A
(MGLS240128Z-HT-HV-G-LED03G-IC-T6A39/40-5V VLED)

DOCUMENT TITLE:
SPECIFICATION
OF
LCD MODULE TYPE
MODEL NUMBER: MGLS240128Z-05

DEPARTMENT	NAME	SIGNATURE	DATE
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A	2004.12.09	<p>First Release. Based on a.) Test Specification: VL-TS-MGLS240128Z-XX REV. E, 2004.10.29.</p> <p>b.) VL-QUA-012A REV. R 2004.03.20.</p> <p>According to VL-QUA-012A, LCD size is middle because Unit Per Laminate=4 which is in the range of 2pcs/Laminate to 6pcs/Laminate.</p>	CHEN HUI JUAN	QIN SONG QING



CONTENTS

	<u>Page No.</u>
1. GENERAL DESCRIPTION	4
2. MECHANICAL SPECIFICATIONS	4
3. INTERFACE SIGNALS	6
4. ABSOLUTE MAXIMUM RATINGS	7
4.1 ELECTRICAL MAXIMUM RATINGS – FOR IC ONLY	7
4.2 ENVIRONMENTAL CONDITION	7
5. ELECTRICAL SPECIFICATIONS	8
5.1 TYPICAL ELECTRICAL CHARACTERISTICS	8
5.2 TIMING SPECIFICATIONS	9
5.3 TIMING DIAGRAM OF VCC AGAINST V0	12
6. LCD COSMETIC CONDITIONS	13
7. REMARK	13



VARITRONIX LIMITED

Specification of LCD Module Type Model No.: MGLS240128Z-05

1. General Description

- 240 x 128 dots STN Positive Yellow Transflective LCD Graphic Module.
- Driving scheme: 1/128 multiplexed drive, 1/12.4 bias.
- Viewing direction: 6 O'clock.
- 'SANYO' LC7981 (flat pack) or equivalent controller for the liquid crystal dot matrix graphic display.
- 'TOSHIBA' T6A39 (flat pack) or equivalent LCD segment drivers.
- 'TOSHIBA' T6A40 (flat pack) or equivalent LCD common drivers.
- 8 K bytes display SRAM.
- Yellow-green LED03 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	144.0(W) x 104.0(H) x 15.0 MAX.(D)	mm
Viewing area	114.0(W) x 64.0(H)	mm
Active area	107.95(W) x 57.55(H)	mm
Display format	240 (Horizontal) x 128 (Vertical)	dots
Dot size	0.40(W) x 0.40(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.45(W) x 0.45(H)	mm
Weight	Approx. 188.6	grams



3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VSS	Ground (0V).
2	VCC	Power supply for logic (+5V).
3	V0	Power supply for LCD driver.
4	RS	Register select: RS=1: Instruction register. RS=0: Data register.
5	R/W	Read/Write: “High” for MPU ← LC7981. “Low” for MPU → LC7981.
6	E	Enable: Data is written at the fall of E. Data can be read while E is 1.
7	DB0	MPU Data input/output (LSB).
8	DB1	MPU Data input/output.
9	DB2	MPU Data input/output.
10	DB3	MPU Data input/output.
11	DB4	MPU Data input/output.
12	DB5	MPU Data input/output.
13	DB6	MPU Data input/output.
14	DB7	MPU Data input/output (MSB).
15	/CS	Chip select: Selected state with /CS=0.
16	/RST	Reset. Setting RST to 0 selects display OFF, slave mode, and Hp=6.
17	LED+	Anode of LED backlight.
18	LED-	Cathode of LED backlight.



4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (Logic)	VCC - VSS	-0.3	+7.0	V
Supply voltage (LCD drive)	VLCD=VCC – V0	-0.3	+30.0	V
Input voltage	V _{in}	-0.3	VCC+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.
All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C			No condensation	
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.			3 directions	
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.			3 directions	



5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VCC = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VCC-VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VCC-V0	VCC = 5V, Note 1	19.8	20.3	20.8	V
Input signal voltage	V _{IH}	“High” level	2.2	-	VCC	V
	V _{IL}	“Low” level	0	-	0.8	V
Supply current (Logic & LCD)	ICC	Character mode, VCC = 5V. Note 1	-	9.7	14.6	mA
		Checker board mode, VCC = 5V. Note 1	-	10.6	15.9	mA
Supply Current (LCD)	I ₀	Character mode, VCC=5V, Note 1	-	5.0	7.5	mA
		Checker board mode, VCC = 5V, Note 1	-	6.0	9.0	mA
Supply voltage of Yellow-green LED03 backlight (with external current limiting resistors)	VLED03 =(VLED+) - (VLED-)	Forward current =300mA Number of LED dies =2x20=40.	4.8	5.0	5.2	V
Wavelength of yellow-green LED03G backlight	λ		-	568	-	nm
Luminance (on the backlight surface) of backlight			18	24	-	cd/m ²

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.



5.2 Timing Specifications

At Ta = -20°C TO +70°C, VCC=5V±5%, VSS=0V.

Refer to Fig. 2(a) & 2(b), the timing diagram of bus read / write operation 1 using 'SANYO' LC7981 respectively.

Table 6

Note	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
1	Address Set-up time	t _{AS}	90	-	-	ns	
2	Address Hold Time	t _{AH}	10	-	-	ns	
3	Data Delay Time (read)	t _{DDR}	-	-	140	ns	C _L =50pF
4	Data Hold Time (read)	t _{DHR}	10	-	-	ns	
5	Data Setup Time (write)	t _{DSW}	220	-	-	ns	
6	Data Hold Time (write)	t _{DHW}	20	-	-	ns	

Refer to Fig. 3(a) & 3(b), the timing diagram of bus read / write operation 2 using 'SANYO' LC7981 respectively.

Table 7

Note	Parameter	Symbol	Min.	Typ.	Max.	Unit	Instruction register value
1	Read cycle time	t _{RCY}	-	-	(Hp+2)x10 ³ /F _{OSC} +200	ns	0DH
2	Write cycle time	t _{WCY1}	-	-	(2Hp+2)x10 ³ /F _{OSC} +200	ns	0EH,0FH
2	Write cycle time	t _{WCY2}	-	-	(Hp+2)x10 ³ /F _{OSC} +200	ns	0CH
2	Write cycle time	t _{WCY3}	-	-	2000/F _{OSC} +200	ns	00H,01H,02H, 03H,04H,08H, 09H,0AH,0BH

Note:

- (1) In the character mode,
Hp is the number of horizontal dots per character in a character display.

In the graphic mode,
Hp indicates how many bits from RAM appear in a 1-byte display.
- (2) F_{OSC} is the oscillating frequency, expressed in MHz.
- (3) All measurement points are at 1.5V.



READ CYCLE

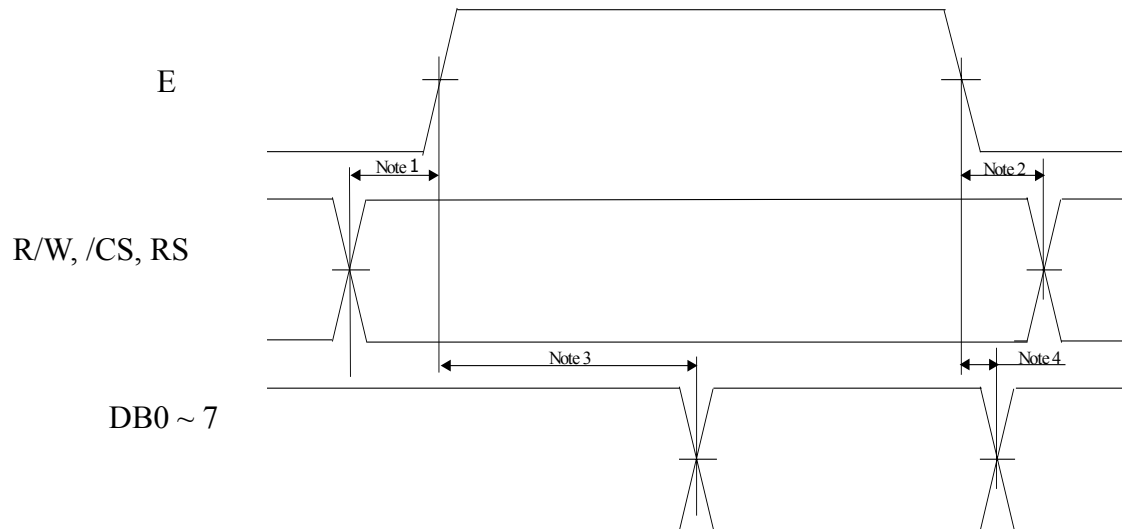


Fig. 2(a): The timing diagram of bus read operation 1 using 'SANYO' LC7981.

WRITE CYCLE

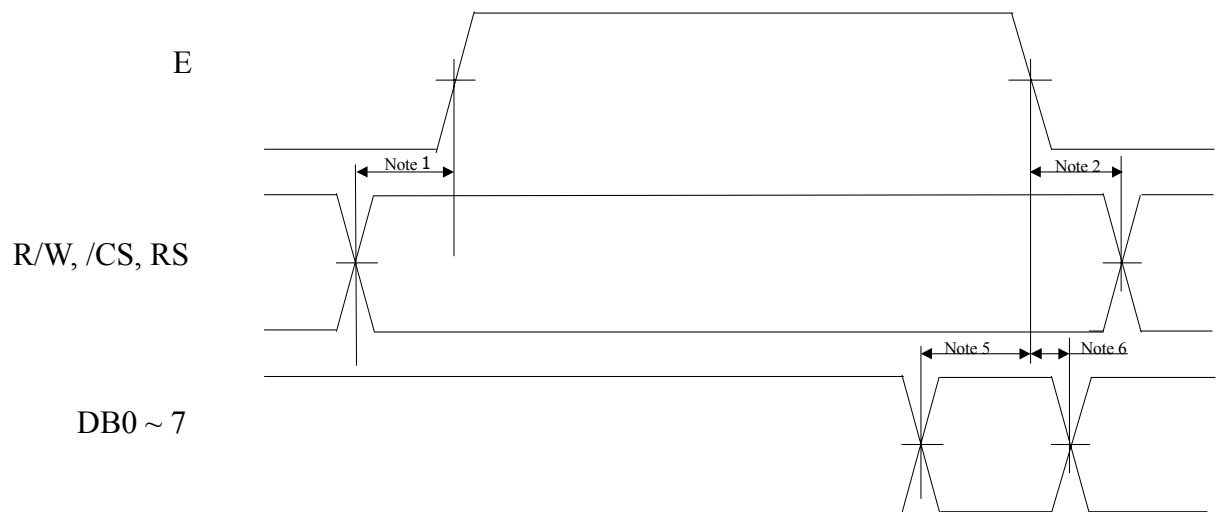


Fig. 2(b): The timing diagram of bus write operation 1 using 'SANYO' LC7981.



DATA READ CYCLE

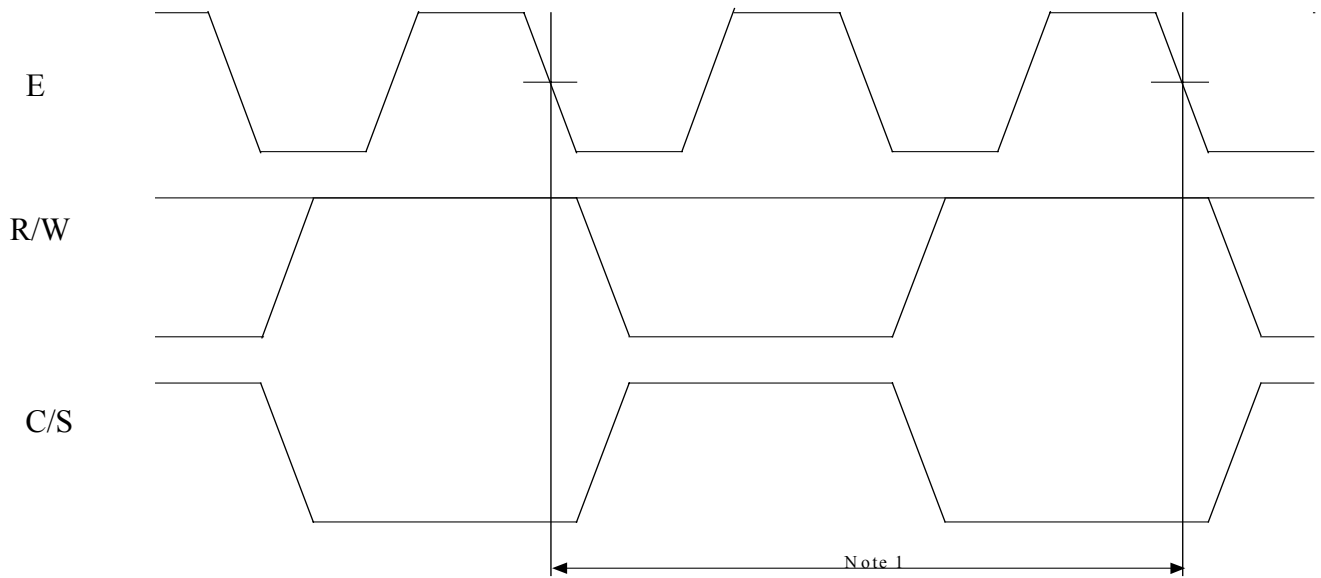


Fig. 3(a): The timing diagram of bus read operation 2 using 'SANYO' LC7981.

DATA WRITE CYCLE

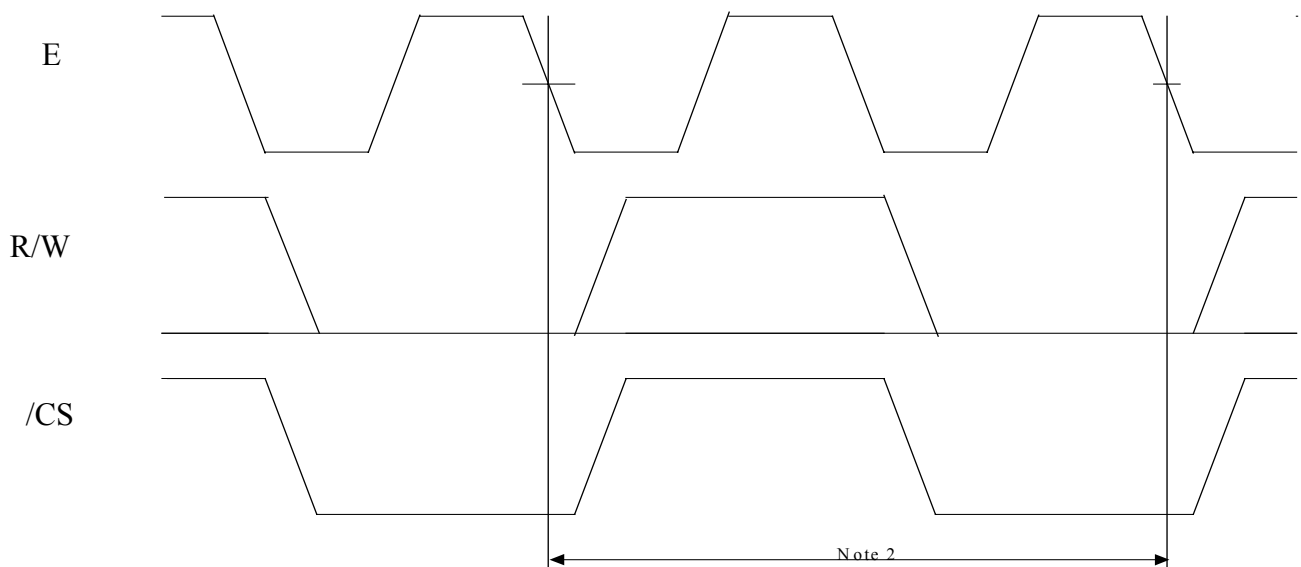


Fig. 3(b): The timing diagram of bus write operation 2 using 'SANYO' LC7981.



5.3 Timing Diagram of VCC Against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VCC against V0.

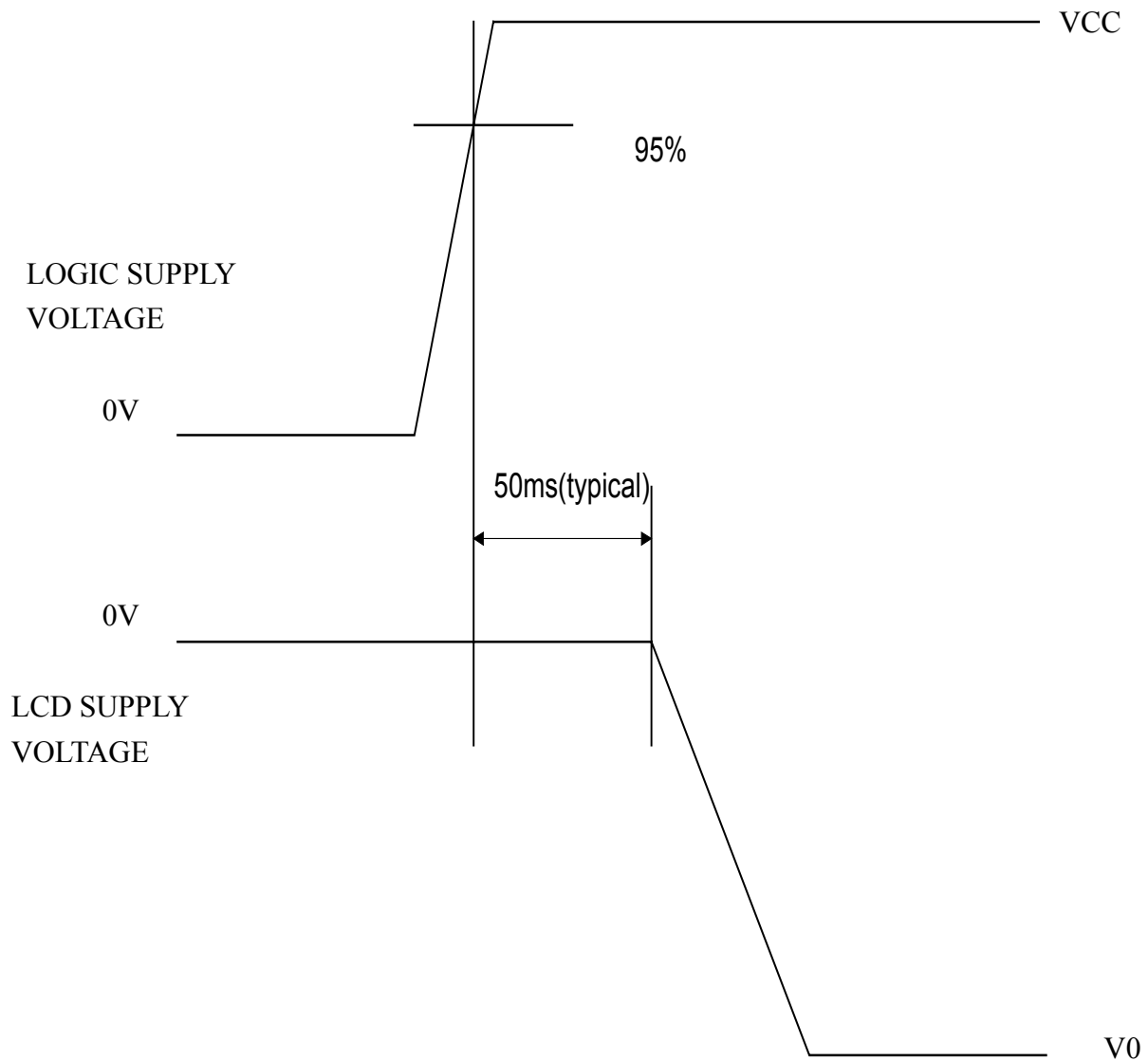


Figure 4: Timing Diagram of VCC Against V0.



6. LCD Cosmetic Conditions

- a.) Reference document follow VL-QUA-012A.
- b.) LCD size of the product is middle.

7. Remark

- a.) Identification labels will be stuck on the module without obstructing the viewing area of display.
- b.) Varitronix does not responsible for any polarizer defect after the protective film has been removed from the display.

“Varitronix Limited reserves the right to change this specification.”

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- END -

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