

P-Channel 60 V (D-S) MOSFET

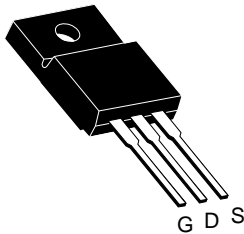
PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
- 60	0.050 at V _{GS} = - 10 V	- 30	67
	0.060 at V _{GS} = - 4.5 V	- 24	

FEATURES

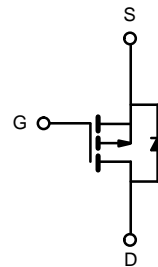
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



TO-220 FULLPAK



Top View



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 60	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 30	A
		T _C = 70 °C	- 29	
Pulsed Drain Current (t = 300 μs)	I _{DM}	- 100		
Avalanche Current	I _{AS}	- 32		
Single Avalanche Energy ^a	L = 0.1 mH	E _{AS}	51	mJ
Maximum Power Dissipation ^a	T _C = 25 °C	P _D	41.7 ^b	W
	T _A = 25 °C ^c		2.1	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	60	°C/W
Junction-to-Case (Drain)	R _{thJC}	3	

Notes:

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

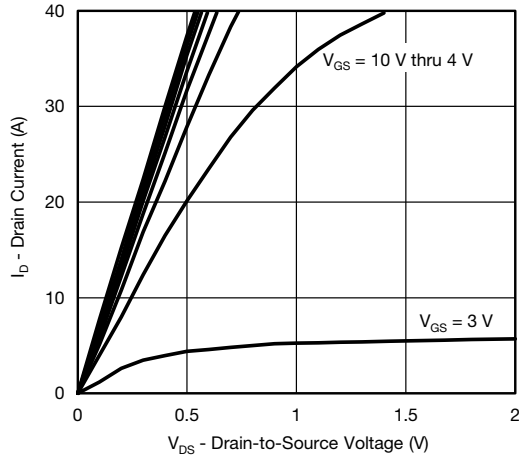
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1		-2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			-50	
		$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$			-250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -10\text{ V}, V_{GS} = -10\text{ V}$	-30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -14\text{ A}$		0.050		Ω
		$V_{GS} = -4.5\text{ V}, I_D = -12\text{ A}$		0.060		
Forward Transconductance ^a	g_{fs}	$V_{DS} = -20\text{ V}, I_D = -14\text{ A}$		40		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -20\text{ V}, f = 1\text{ MHz}$		1765		μF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			180		
Total Gate Charge ^c	Q_g	$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -14\text{ A}$		67		nC
Gate-Source Charge ^c	Q_{gs}			13.5		
Gate-Drain Charge ^c	Q_{gd}			14		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.5	2.5	5	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		10	20	ns
Rise Time ^c	t_r			11	20	
Turn-Off Delay Time ^c	$t_{d(off)}$			42	63	
Fall Time ^c	t_f			12	20	
Drain-Source Body Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}^b$						
Continuous Current	I_S				-36	A
Pulsed Current	I_{SM}				-100	
Forward Voltage ^a	V_{SD}	$I_F = -10\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.5	V
Reverse Recovery Time	t_{rr}	$I_F = -10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		38	57	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			2.3	3.5	A
Reverse Recovery Charge	Q_{rr}			40	60	nC

Notes:

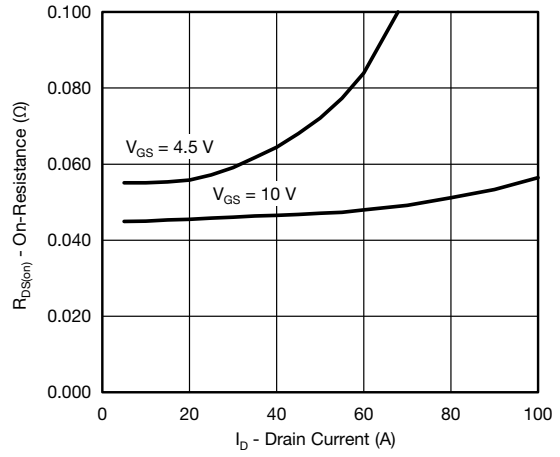
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

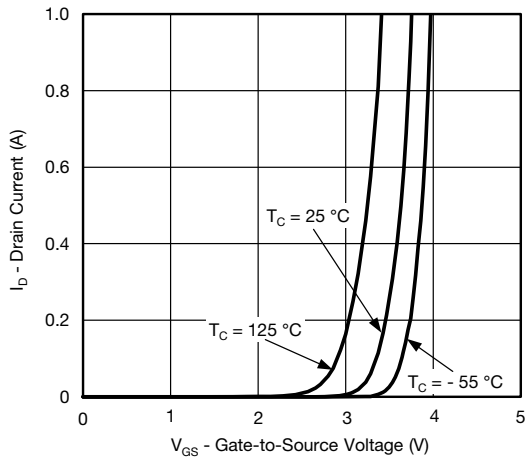
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



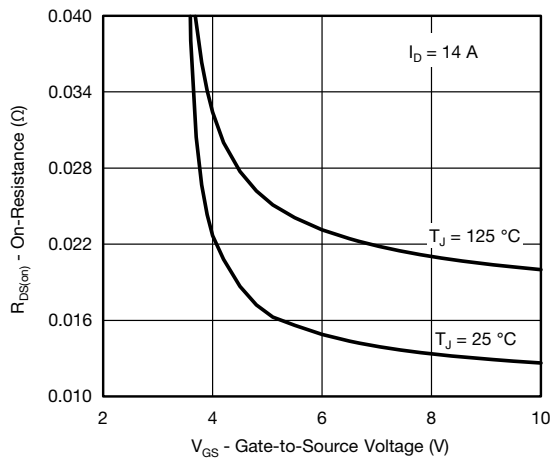
Output Characteristics



On-Resistance vs. Drain Current



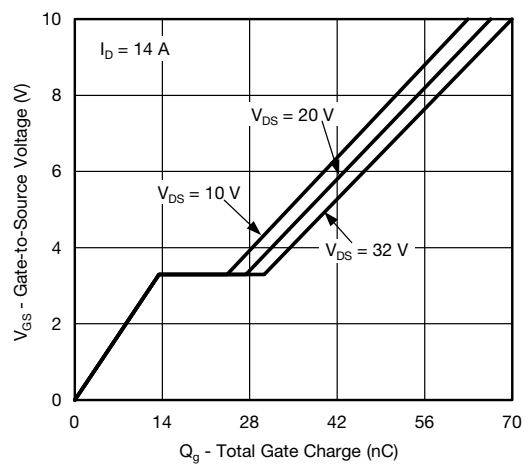
Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage



Transconductance



Gate Charge

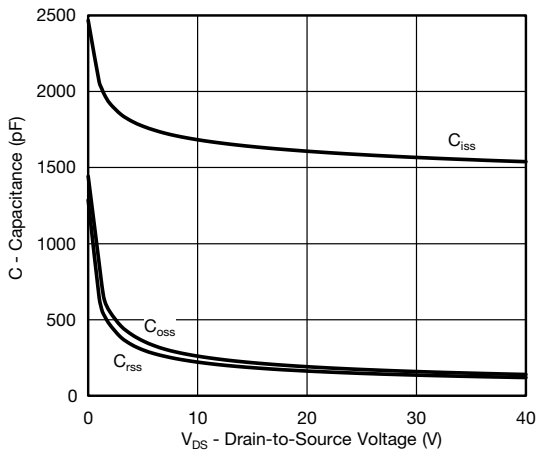
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



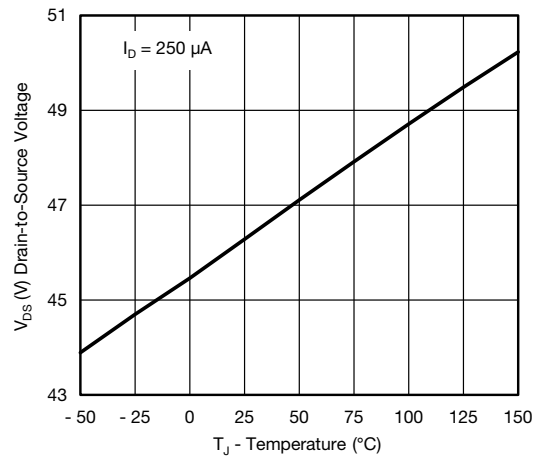
Source-Drain Diode Forward Voltage



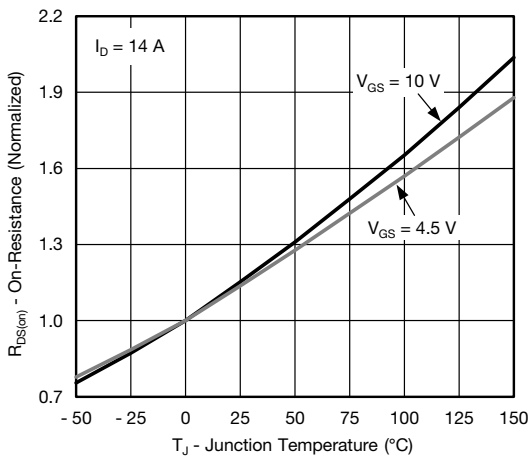
Threshold Voltage



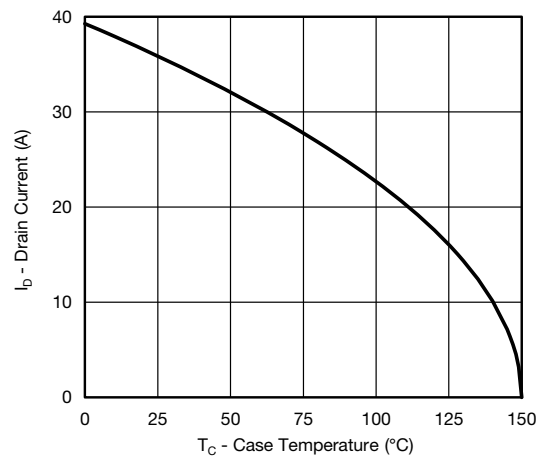
Capacitance



Drain Source Breakdown vs. Junction Temperature

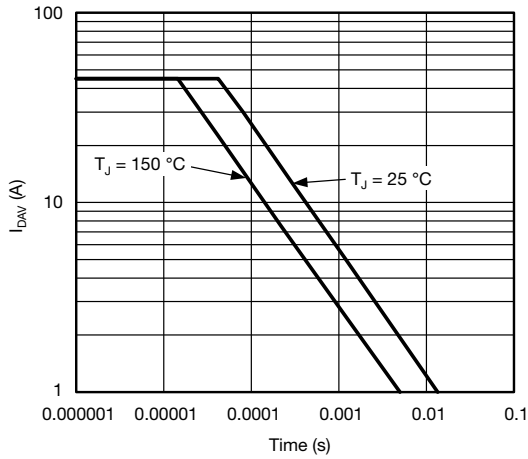


On-Resistance vs. Junction Temperature

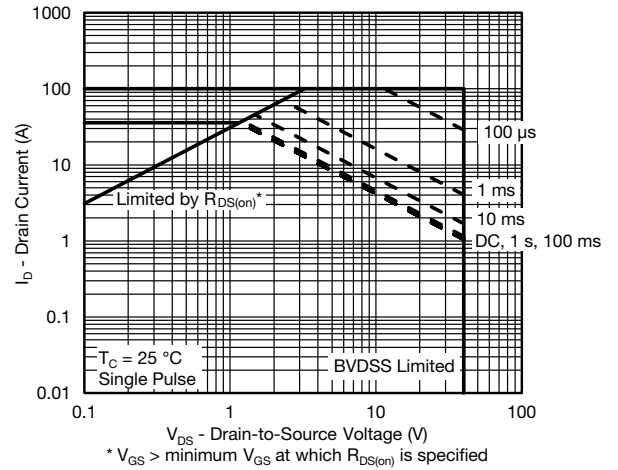


Current Derating

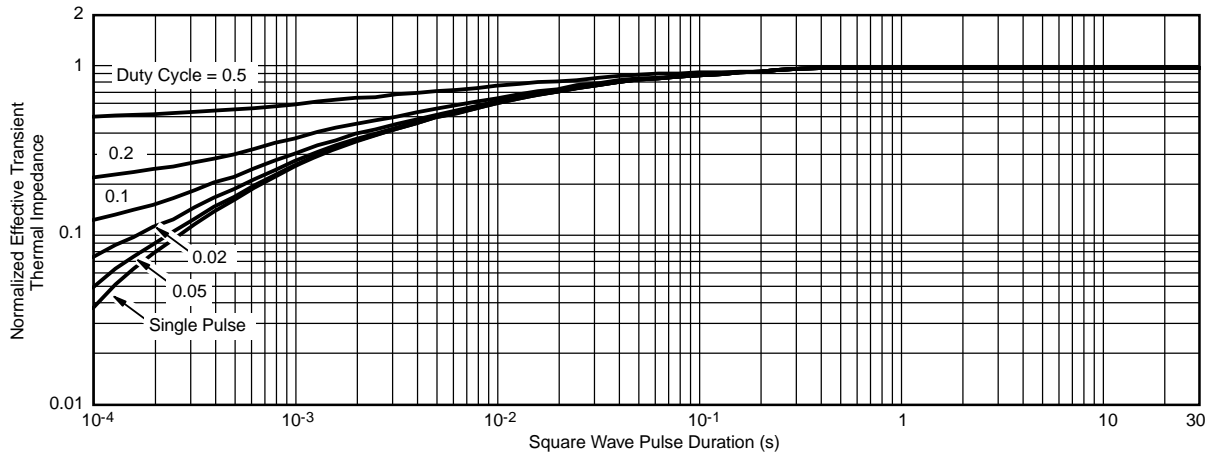
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Single Pulse Avalanche Current Capability vs. Time



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

TO-220 FULLPAK (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09
DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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