

N-Channel 60 V (D-S) MOSFET

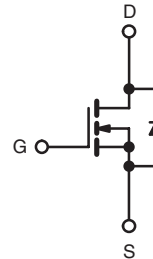
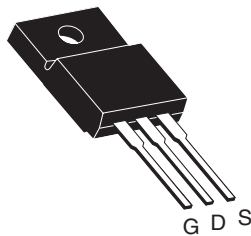
| PRODUCT SUMMARY | | |
|---------------------------|-----------------|-------|
| V_{DS} (V) | 60 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10$ V | 0.027 |
| Q_g (Max.) (nC) | 95 | |
| Q_{gs} (nC) | 27 | |
| Q_{gd} (nC) | 46 | |
| Configuration | Single | |

FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- 175 °C Operating Temperature
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available



TO-220 FULLPAK



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted | | | | |
|--|------------------|-----------------------------------|-------|----------|
| PARAMETER | SYMBOL | LIMIT | UNIT | |
| Drain-Source Voltage | V_{DS} | 60 | V | |
| Gate-Source Voltage | V_{GS} | ± 20 | | |
| Continuous Drain Current | I_D | V_{GS} at 10 V $T_C = 25$ °C | 45 | A |
| | | $T_C = 100$ °C | 30 | |
| Pulsed Drain Current ^a | I_{DM} | 220 | | |
| Linear Derating Factor | | 0.32 | W/°C | |
| Single Pulse Avalanche Energy ^b | E_{AS} | 100 | mJ | |
| Maximum Power Dissipation | P_D | 52 | W | |
| Peak Diode Recovery dV/dt ^c | dV/dt | 4.5 | V/ns | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to + 175 | °C | |
| Soldering Recommendations (Peak Temperature) | for 10 s | 300 ^d | | |
| Mounting Torque | 6-32 or M3 screw | 10 | | lbf · in |
| | | 1.1 | N · m | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$ V, starting $T_J = 25$ °C, L = 129 μ H, $R_G = 25$ Ω , $I_{AS} = 30$ A (see fig. 12).
- $I_{SD} \leq 52$ A, $dI/dt \leq 250$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
- 1.6 mm from case.

| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | 65 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 3.1 | |

| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | | |
|--|---------------------|---|--|------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 60 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | | - | 0.060 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 1.0 | - | 3.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 25 | μA |
| | | $V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$ | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 18\text{ A}^b$ | - | 0.027 | - | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 25\text{ V}, I_D = 18\text{ A}^b$ | | 15 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5 | | - | 1500 | - | pF |
| Output Capacitance | C_{oss} | | | - | 720 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 100 | - | |
| Drain to Sink Capacitance | C | $f = 1.0\text{ MHz}$ | | - | 12 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 52\text{ A}, V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^b | - | - | 95 | nC |
| Gate-Source Charge | Q_{GS} | | | - | - | 27 | |
| Gate-Drain Charge | Q_{GD} | | | - | - | 46 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 30\text{ V}, I_D = 52\text{ A}, R_G = 9.1\text{ }\Omega, R_D = 0.54\text{ }\Omega$, see fig. 10 ^b | | - | 19 | - | ns |
| Rise Time | t_r | | | - | 120 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 55 | - | |
| Fall Time | t_f | | | - | 86 | - | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact | | - | 4.5 | - | nH |
| Internal Source Inductance | L_S | | | - | 7.5 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode | | - | - | 45 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | | - | - | 120 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 30\text{ A}, V_{GS} = 0\text{ V}^b$ | | - | - | 2.5 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 52\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$ | | - | 140 | 300 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | - | 1.2 | 2.8 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

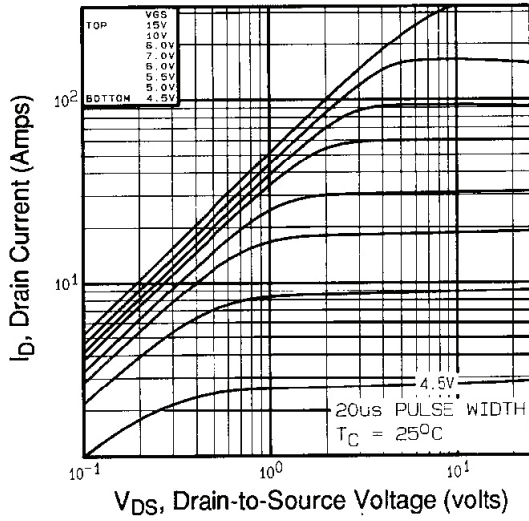


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

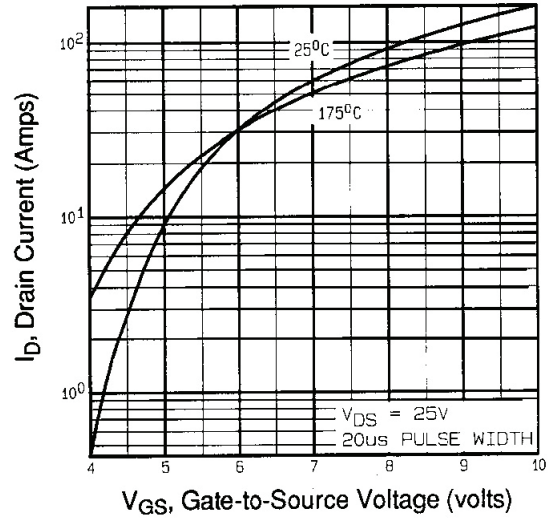


Fig. 3 - Typical Transfer Characteristics

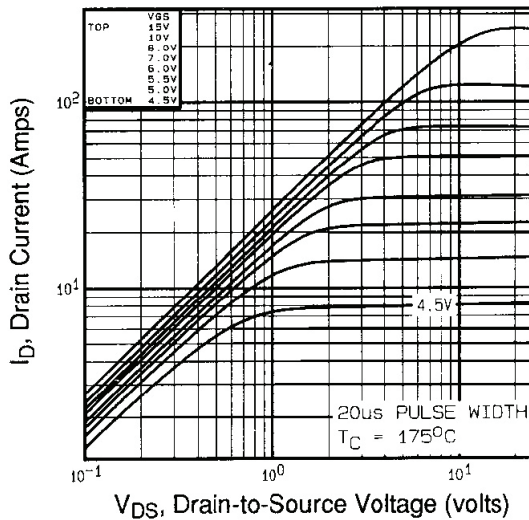


Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^\circ\text{C}$

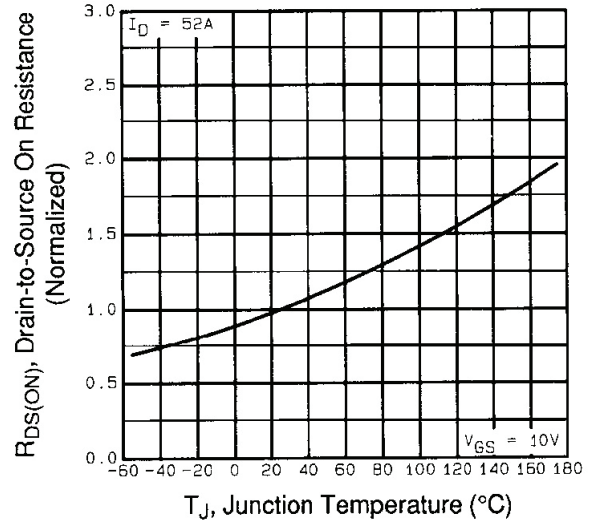


Fig. 4 - Normalized On-Resistance vs. Temperature



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

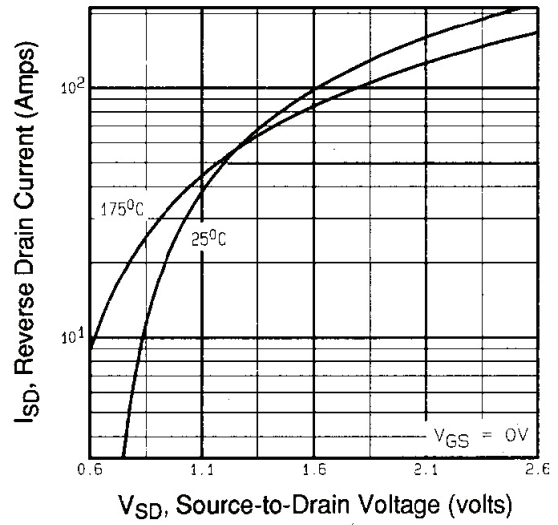


Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

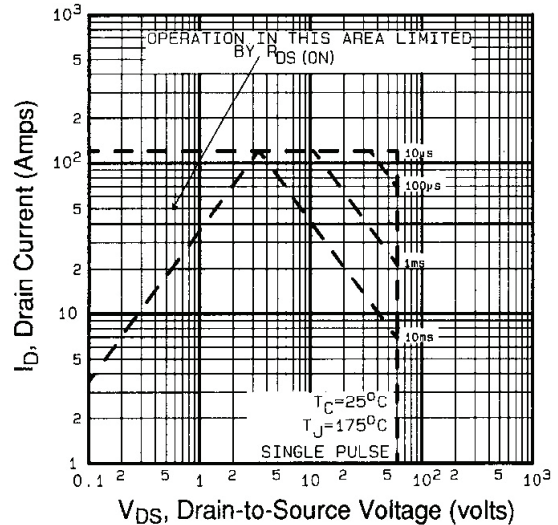


Fig. 8 - Maximum Safe Operating Area

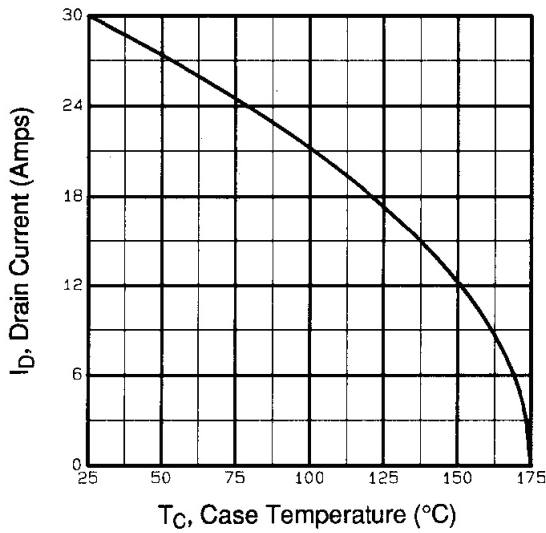


Fig. 9 - Maximum Drain Current vs. Case Temperature

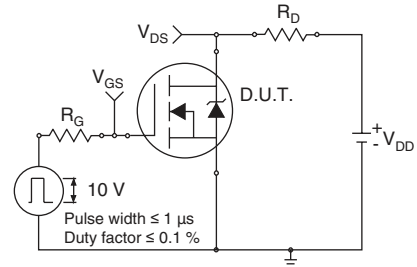


Fig. 10a - Switching Time Test Circuit

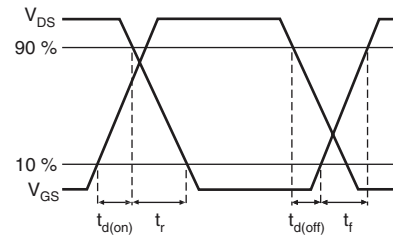


Fig. 10b - Switching Time Waveforms

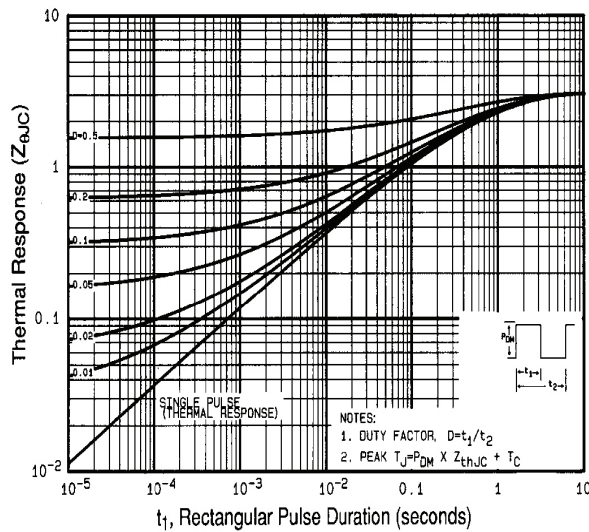


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

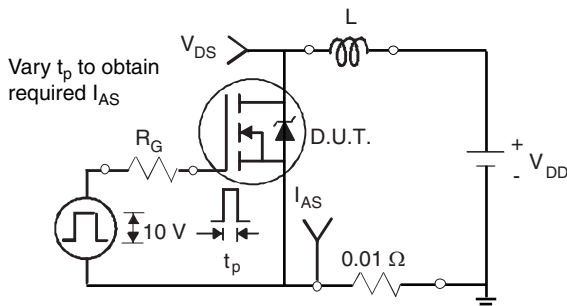


Fig. 12a - Unclamped Inductive Test Circuit

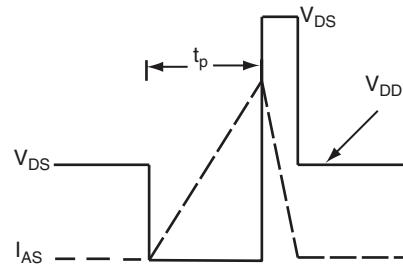


Fig. 12b - Unclamped Inductive Waveforms



Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 13a - Basic Gate Charge Waveform

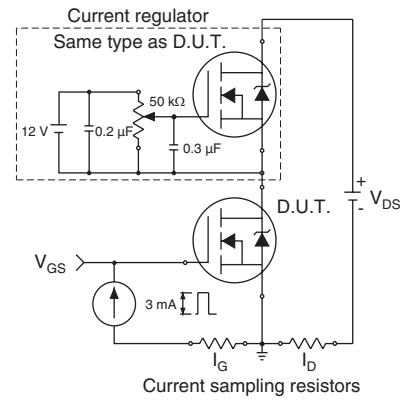
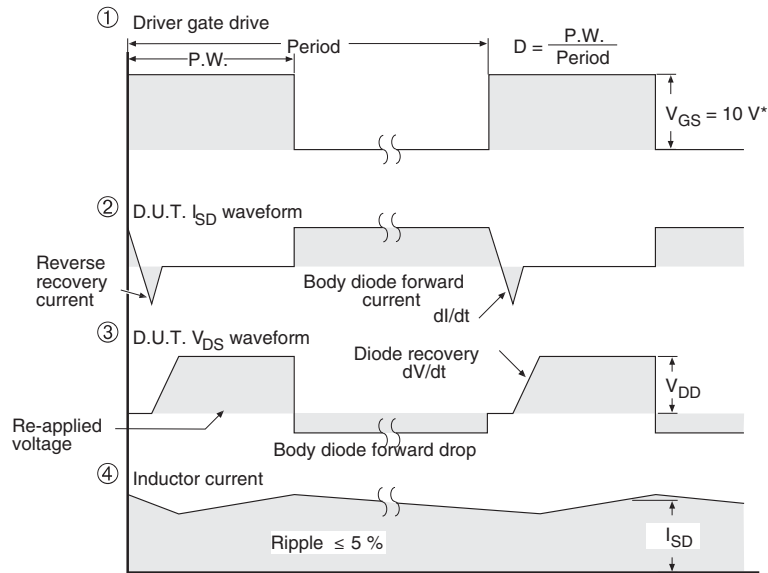


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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