

Power MOSFET

| PRODUCT SUMMARY | | |
|---------------------------|------------------------|-------|
| V_{DS} (V) | 100 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10\text{ V}$ | 0.020 |
| Q_g (Max.) (nC) | 70 | |
| Q_{gs} (nC) | 13 | |
| Q_{gd} (nC) | 39 | |
| Configuration | Single | |

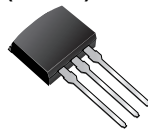
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Low-Profile Through-Hole
- Available in Tape and Reel
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC

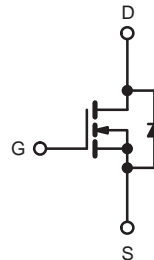


RoHS*
 COMPLIANT
 HALOGEN
FREE
 Available

**I²PAK
(TO-262)**



**D²PAK
(TO-263)**



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | |
|---|----------------------------------|-----------------------------------|----------------|------------------|------|
| PARAMETER | | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | | V_{DS} | 100 | V |
| Gate-Source Voltage | | | V_{GS} | ± 20 | |
| Continuous Drain Current | V_{GS} at 10 V | $T_C = 25\text{ }^\circ\text{C}$ | I_D | 70 | A |
| | | $T_C = 100\text{ }^\circ\text{C}$ | | 56 | |
| Pulsed Drain Current ^{a, e} | | | I_{DM} | 250 | |
| Linear Derating Factor | | | | 1.0 | W/°C |
| Single Pulse Avalanche Energy ^{b, e} | | | E_{AS} | 580 | mJ |
| Avalanche Current ^a | | | I_{AR} | 20 | A |
| Repetitive Avalanche Energy ^a | | | E_{AR} | 13 | mJ |
| Maximum Power Dissipation | $T_C = 25\text{ }^\circ\text{C}$ | | P_D | 3.1 | W |
| | $T_A = 25\text{ }^\circ\text{C}$ | | | 130 | |
| Peak Diode Recovery dV/dt ^{c, e} | | | dV/dt | 5.0 | V/ns |
| Operating Junction and Storage Temperature Range | | | T_J, T_{stg} | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300 ^d | |

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 2.7\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 18\text{ A}$ (see fig. 12).
- $I_{SD} \leq 20\text{ A}$, $dI/dt \leq 150\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | |
|--|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient (PCB Mounted, Steady-State) ^a | R_{thJA} | - | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 1.0 | |

Note

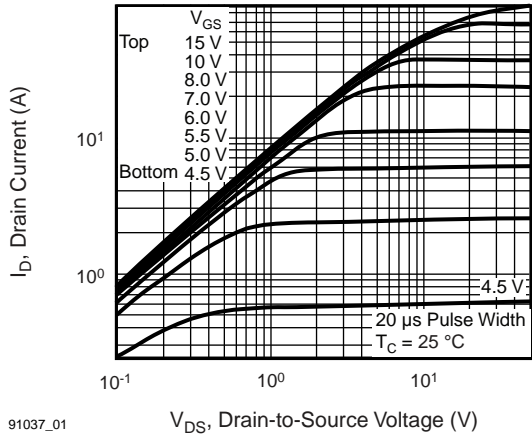
a. When mounted on 1" square PCB (FR-4 or G-10 material).

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------------|--|--|------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 100 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^c$ | | - | 0.29 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 25 | μA |
| | | $V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 11\text{ A}^b$ | - | 0.020 | - | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}, I_D = 11\text{ A}^d$ | | 6.7 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5 ^d | | - | 1300 | - | pF |
| Output Capacitance | C_{oss} | | | - | 430 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 130 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 20\text{ A}, V_{DS} = 160\text{ V}$, see fig. 6 and 13 ^{b, c} | - | - | 70 | nC |
| Gate-Source Charge | Q_{gs} | | | - | - | 13 | |
| Gate-Drain Charge | Q_{gd} | | | - | - | 39 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 50\text{ V}, I_D = 20\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 5.4\text{ }\Omega$, see fig. 10 ^{b, c} | | - | 14 | - | ns |
| Rise Time | t_r | | | - | 51 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 45 | - | |
| Fall Time | t_f | | | - | 36 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 20 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | | - | - | 72 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 20\text{ A}, V_{GS} = 0\text{ V}^b$ | | - | - | 2.0 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b, c$ | | - | 300 | 610 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | - | 3.4 | 7.1 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

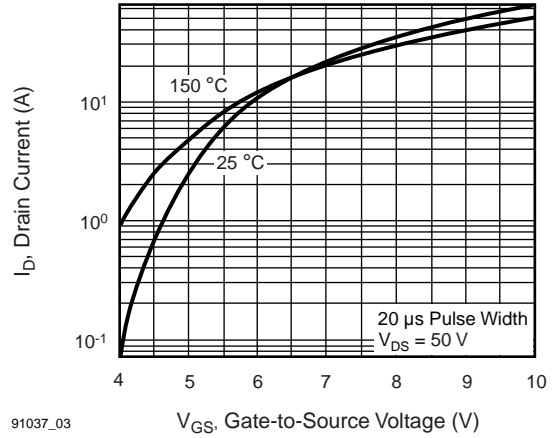
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- Uses IRF640/SiHF640 data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



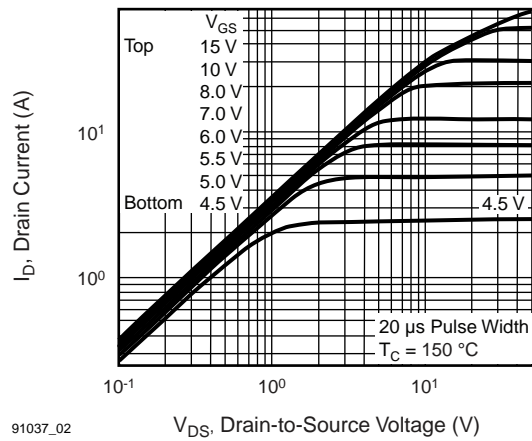
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Fig. 1 - Typical Output Characteristics, $T_J = 25\text{ °C}$



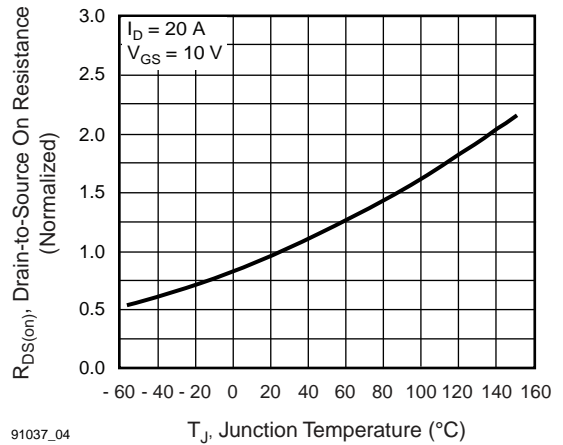
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Fig. 3 - Typical Transfer Characteristics



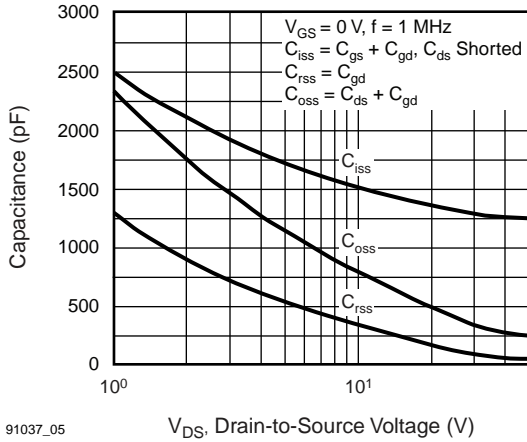
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Fig. 2 - Typical Output Characteristics, $T_J = 175\text{ °C}$



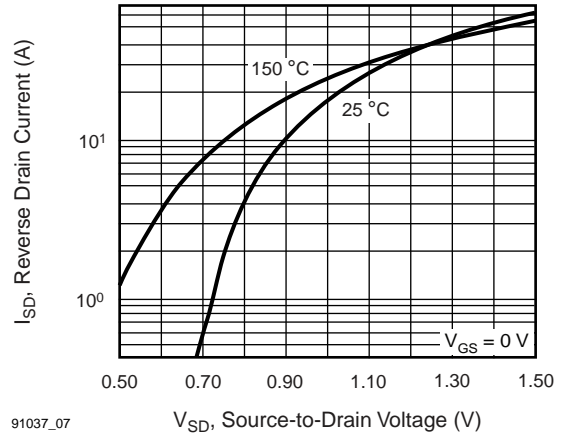
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Fig. 4 - Normalized On-Resistance vs. Temperature



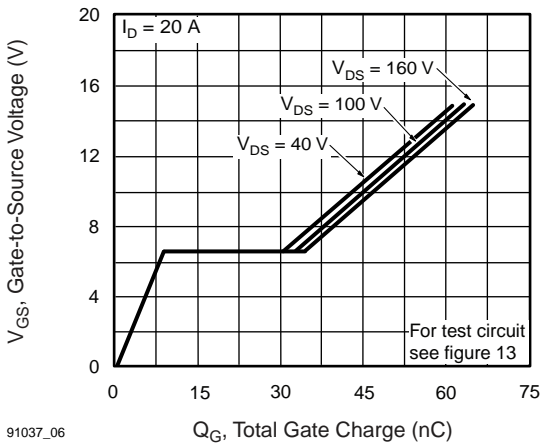
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



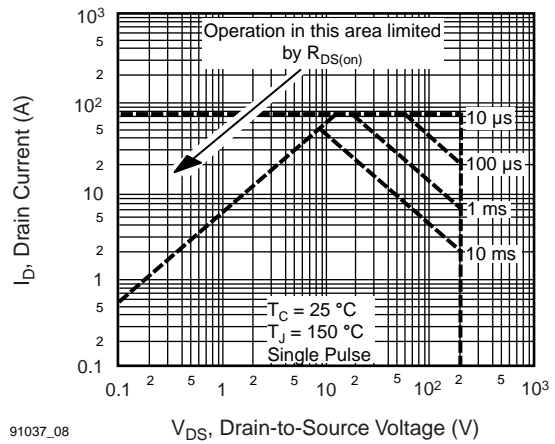
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



91037_08

Fig. 8 - Maximum Safe Operating Area

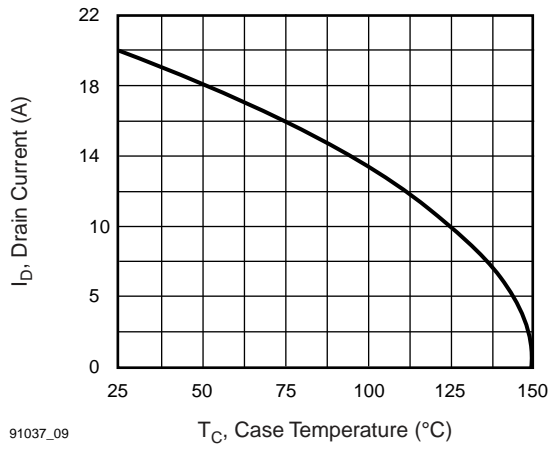


Fig. 9 - Maximum Drain Current vs. Case Temperature

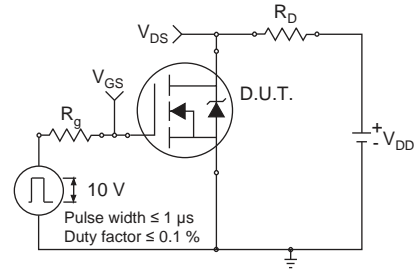


Fig. 10a - Switching Time Test Circuit

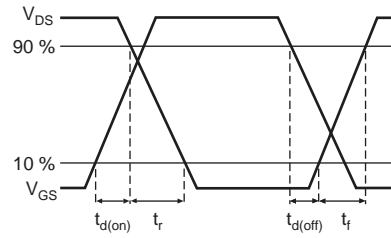


Fig. 10b - Switching Time Waveforms

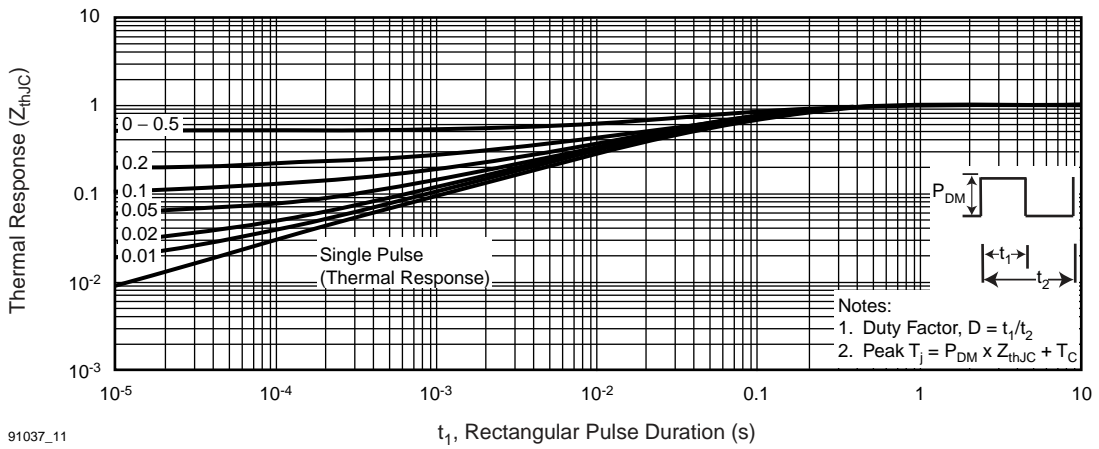


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms

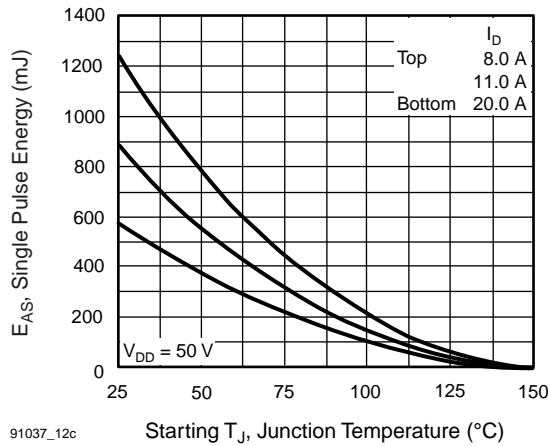


Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 13a - Basic Gate Charge Waveform

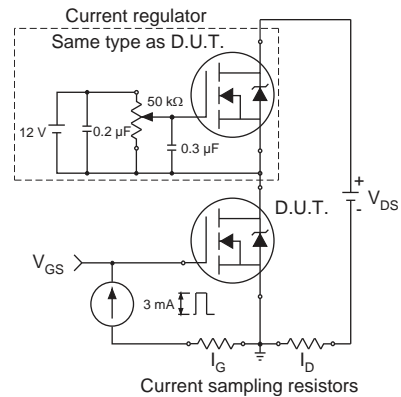
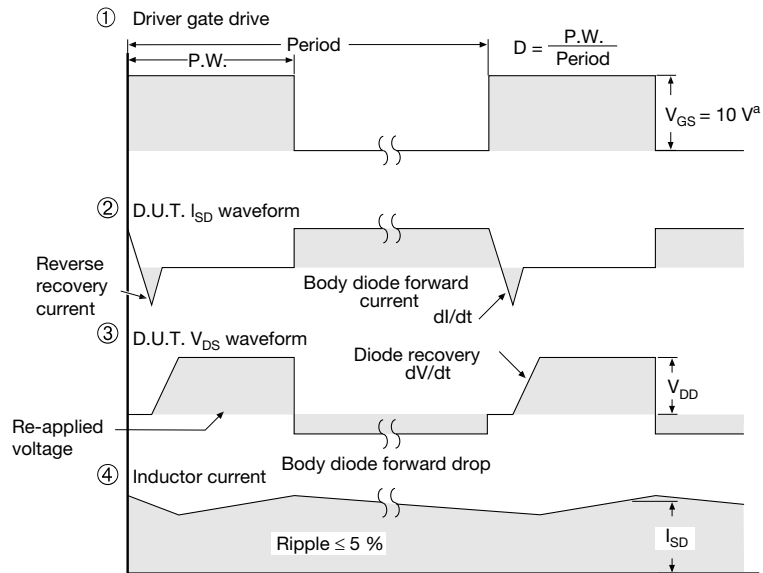


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

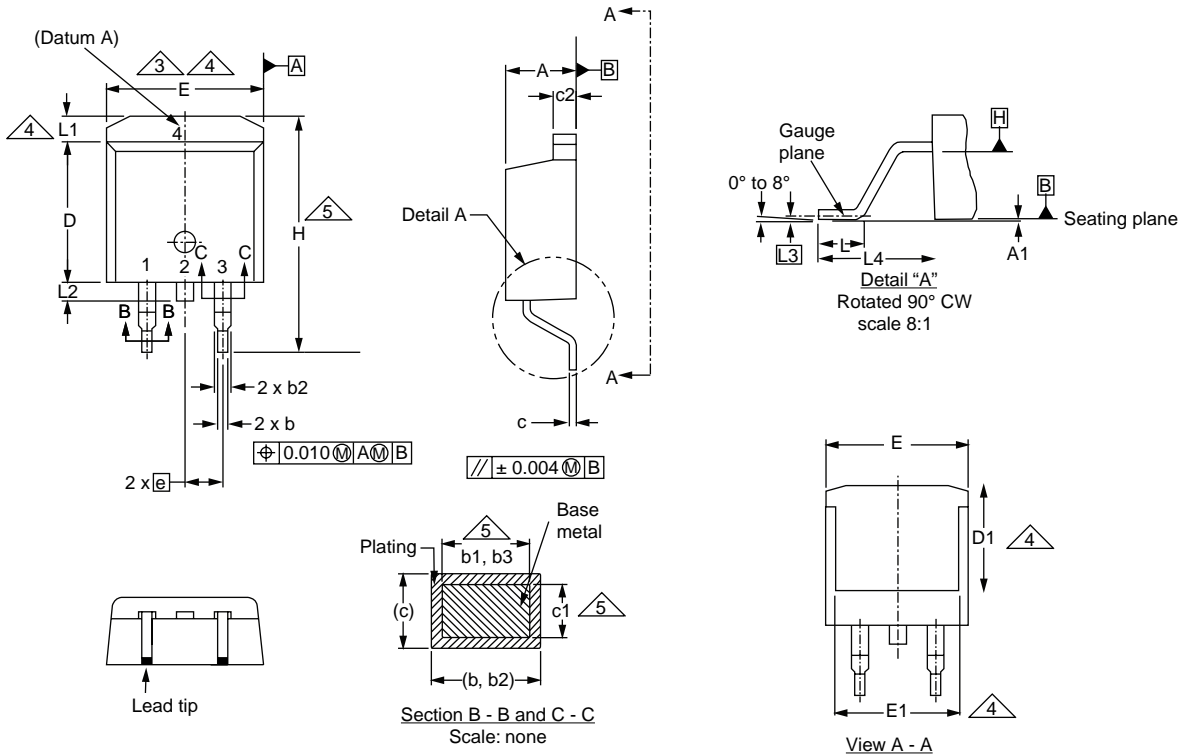


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

TO-263AB (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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