N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)	Q_g (Typ.)
80	0.0055 at V_{GS} = 10 V	75[a]	17.1 nC
	0.0088 at V_{GS} = 6.0 V	65[a]	
	0.0115 at V_{GS} = 5.0 V	54	

FEATURES

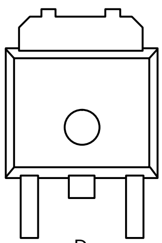
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested

RoHS COMPLIANT
HALOGEN FREE

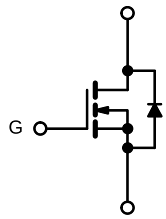
APPLICATIONS

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting

TO-252



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	75[a]	A
	T_C = 70 °C		62.7	
	T_A = 25 °C		28.6[b, c]	
	T_A = 70 °C		24.9[b, c]	
Pulsed Drain Current (t = 100 μs)		I_{DM}	150	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	75a	
	T_A = 25 °C		4.5[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	30	
Single Pulse Avalanche Energy		E_{AS}	45	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	62.5	W
	T_C = 70 °C		40	
	T_A = 25 °C		5[b, c]	
	T_A = 70 °C		3.2[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b, f]	t ≤ 10 s	R_{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.5	2.0	

Notes

a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. The TO-220 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 70 °C/W.

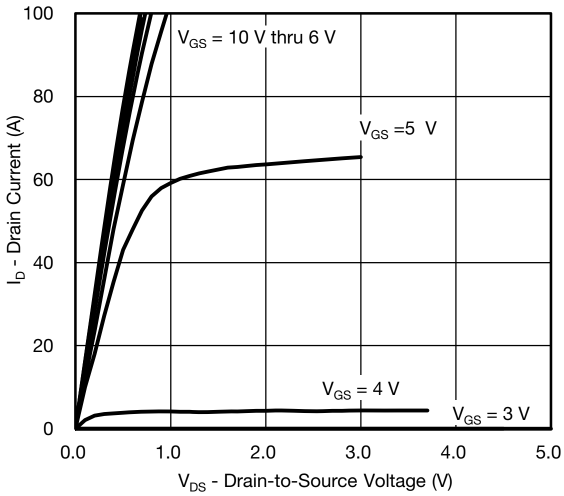
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	80			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA		37		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	2.5		4.0	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.0050		Ω
		V_{GS} = 6 V, I_D = 15 A		0.0070		
		V_{GS} = 5.0 V, I_D = 10 A		0.0087		
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 20 A		60		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		1855		pF
Output Capacitance	C_{oss}			950		
Reverse Transfer Capacitance	C_{rss}			76		
Total Gate Charge	Q_g	V_{DS} = 40 V,V_{GS} = 10 V, I_D = 10 A		35.5	54	nC
		V_{DS} = 40 V, V_{GS} = 6 V, I_D = 10 A		22	33	
		V_{DS} = 40 V,V_{GS} = 4.5 V, I_D = 10 A		17.1	26	
Gate-Source Charge	Q_{gs}			5.3		
Gate-Drain Charge	Q_{gd}			7.3		
Output Charge	Q_{oss}	V_{DS} = 40 V, V_{GS} = 0 V		57	86	
Gate Resistance	R_g	f = 1 MHz	0.5	1.3	2	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 40 V, R_L = 4 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		12	24	ns
Rise Time	t_r			8	16	
Turn-Off DelayTime	$t_{d(off)}$			32	64	
Fall Time	t_f			7	14	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 40 V, R_L = 4 Ω $I_D \cong$ 10 A, V_{GEN} = 6.0 V, R_g = 1 Ω		14	28	
Rise Time	t_r			11	22	
Turn-Off DelayTime	$t_{d(off)}$			30	60	
Fall Time	t_f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			75	A
Pulse Diode Forward Current (t = 100 μs)	I_{SM}				150	
Body Diode Voltage	V_{SD}	I_S = 5 A		0.76	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 10 A, dI/dt = 100 A/μs, T_J = 25 °C		38	75	ns
Body Diode Reverse Recovery Charge	Q_{rr}			36	70	nC
Reverse Recovery Fall Time	t_a			19		ns
Reverse Recovery Rise Time	t_b			19		

Notes

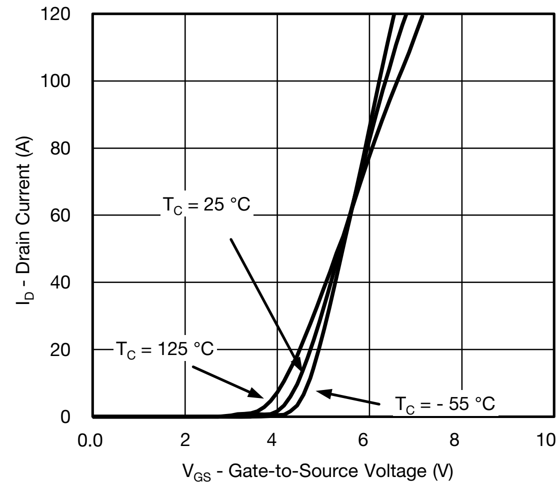
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

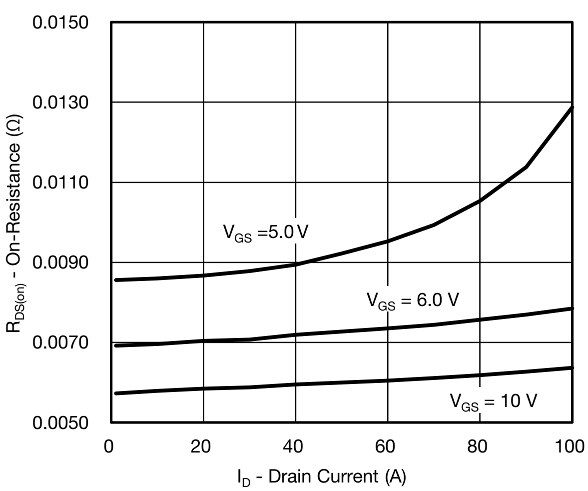
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



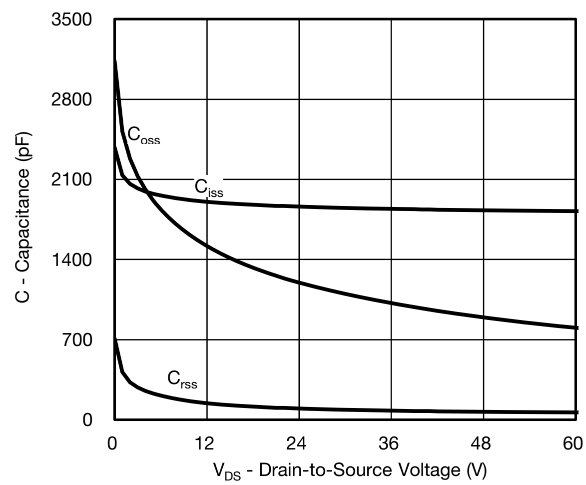
Output Characteristics



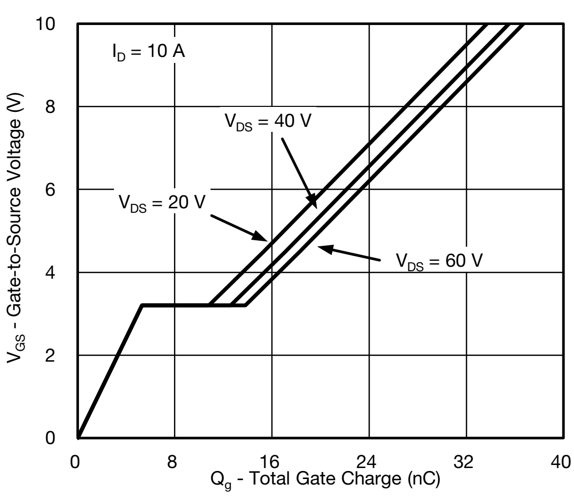
Transfer Characteristics



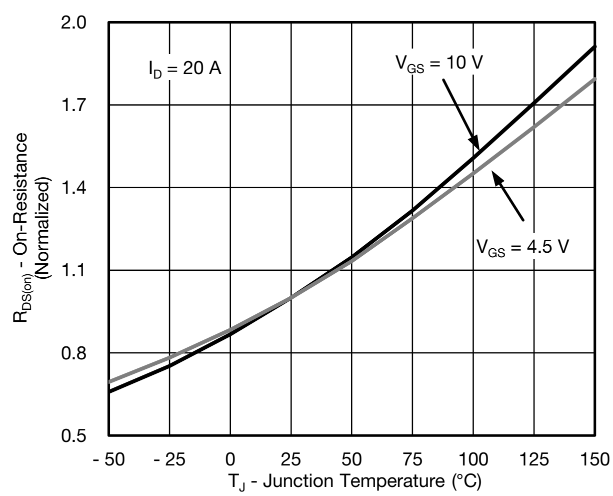
On-Resistance vs. Drain Current



Capacitance

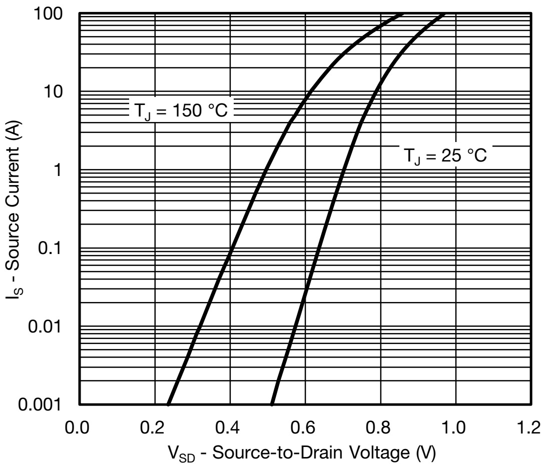


Gate Charge

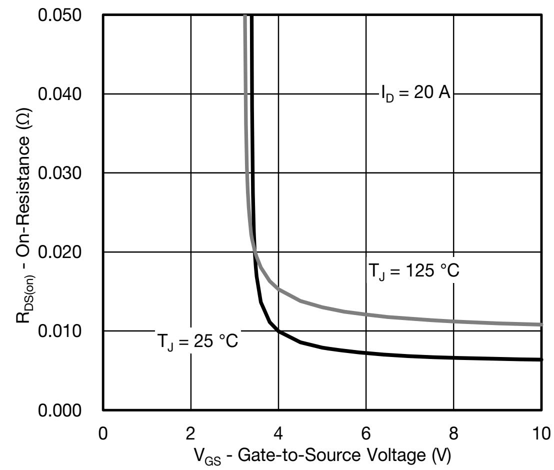


On-Resistance vs. Junction Temperature

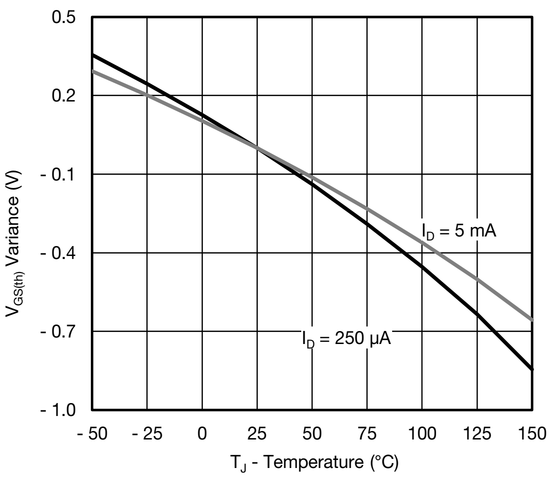
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



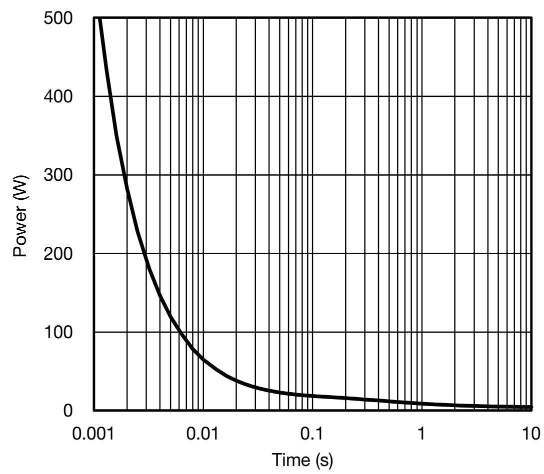
Source-Drain Diode Forward Voltage



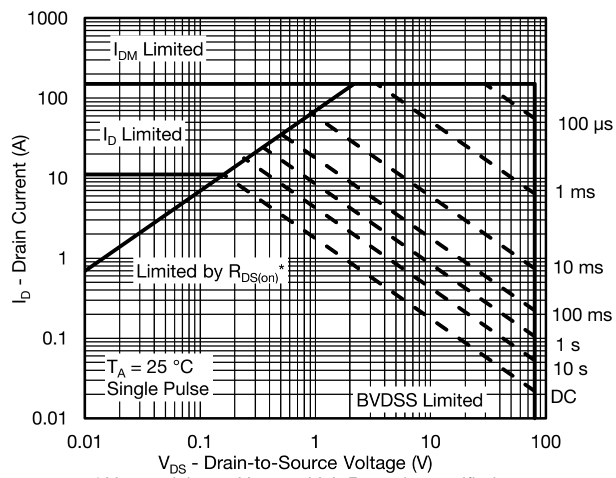
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



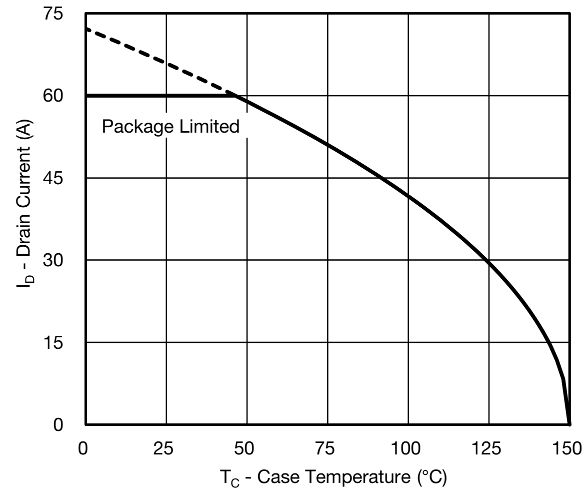
Single Pulse Power, Junction-to-Ambient



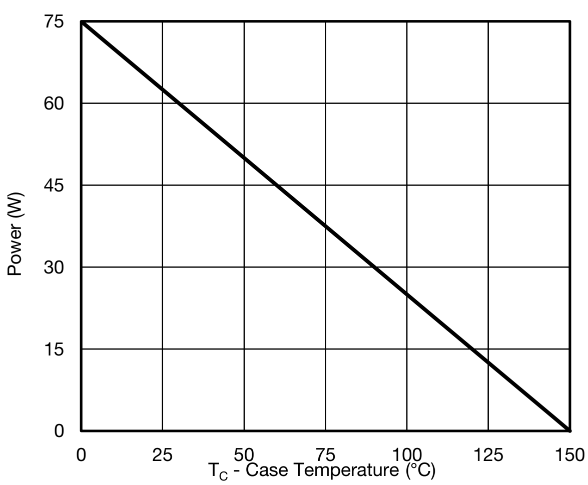
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

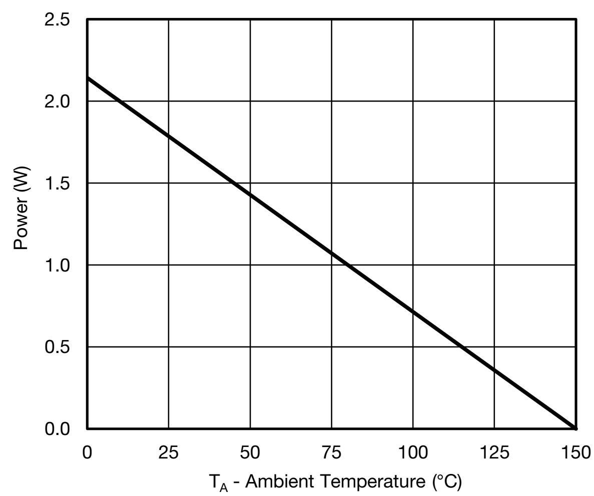
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



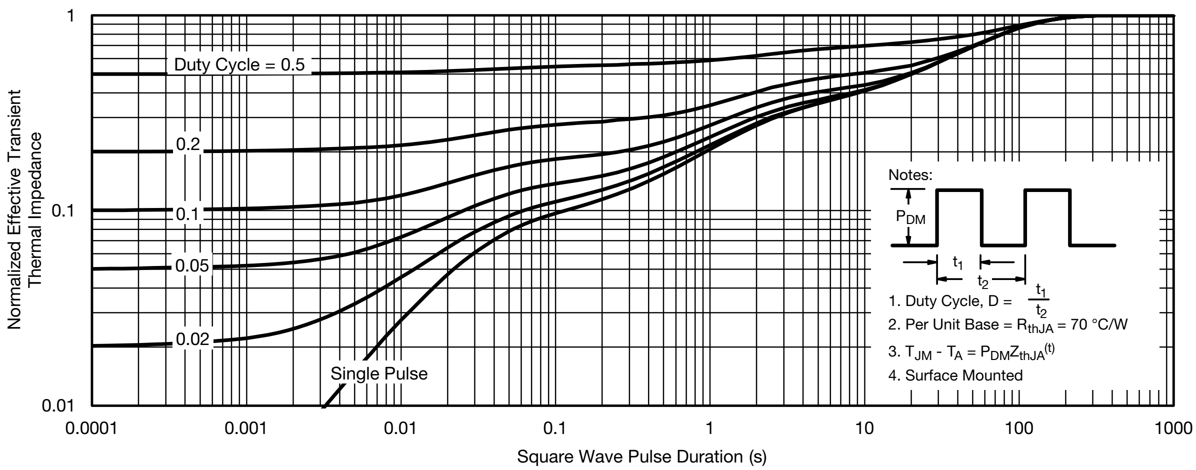
Power, Junction-to-Case



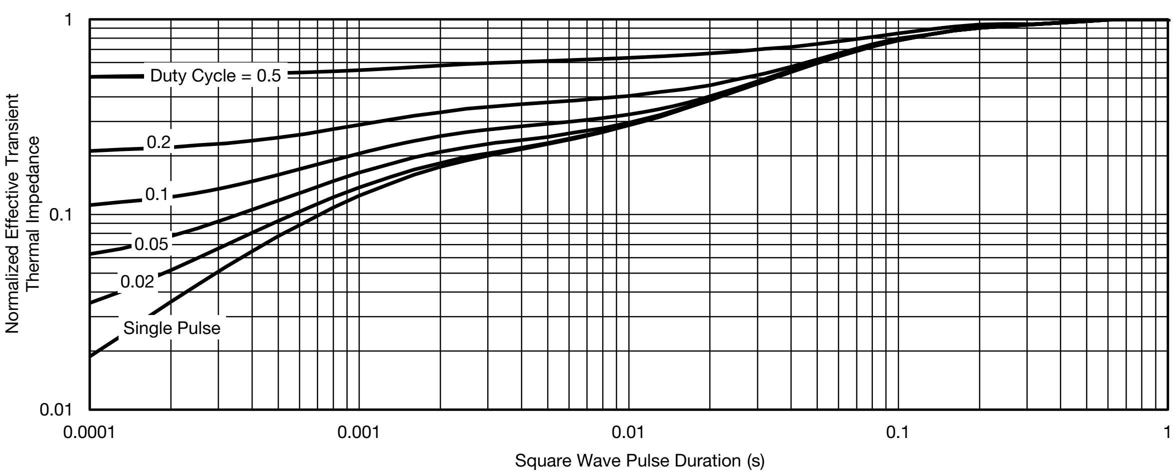
Power, Junction-to-Ambient

** The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.*

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

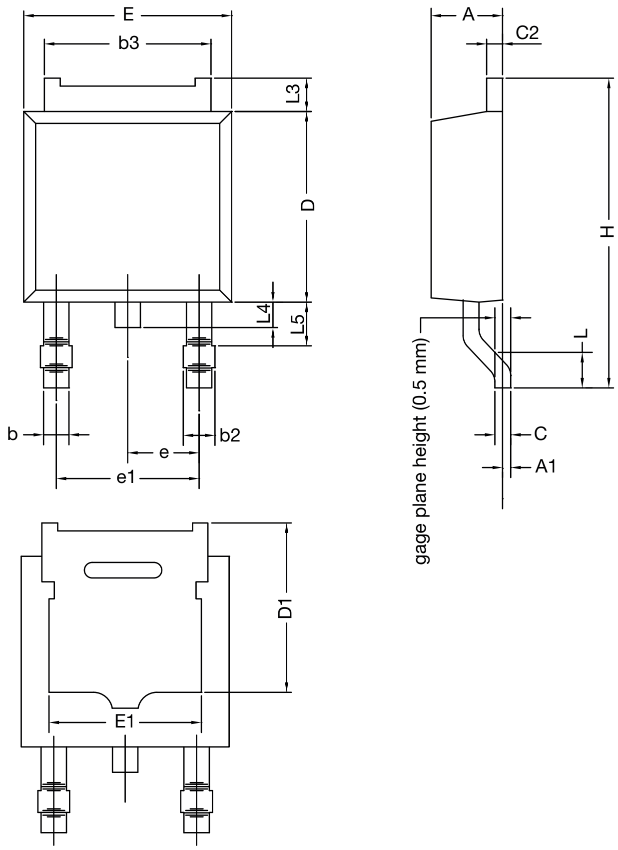


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

TO-252AA CASE OUTLINE

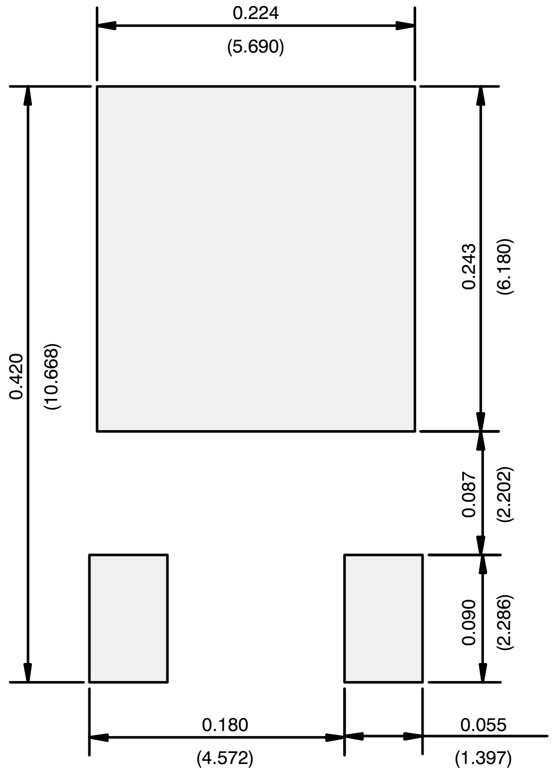


	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347				

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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