

## FCP850N80Z-VB Datasheet

### N-Channel 800V (D-S) Super Junction Power MOSFET

| PRODUCT SUMMARY                            |                        |       |
|--|------------------------|-------|
| V <sub>DS</sub> (V) at T <sub>J</sub> max. | 800                    |       |
| R <sub>DS(on)</sub> at 25 °C (Ω)           | V <sub>GS</sub> = 10 V | 0.800 |

#### FEATURES

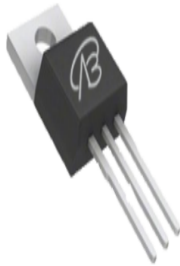
- Low figure-of-merit (FOM) R<sub>on</sub> x Q<sub>g</sub>
- Low input capacitance (C<sub>iss</sub>)
- Reduced switching and conduction losses
- Ultra low gate charge (Q<sub>g</sub>)
- Avalanche energy rated (UIS)



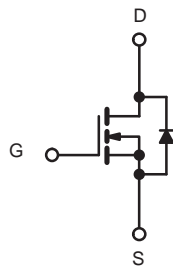
#### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial

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Top View



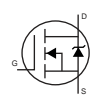
N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted) |                                   |                         |      |      |
|---|-----------------------------------|-------------------------|------|------|
| PARAMETER   | SYMBOL                            | LIMIT                   | UNIT |      |
| Drain-Source Voltage  | V <sub>DS</sub>                   | 800                     | V    |      |
| Gate-Source Voltage   | V <sub>GS</sub>                   | ± 30                    |      |      |
| Continuous Drain Current (T <sub>J</sub> = 150 °C)                        | V <sub>GS</sub> at 10 V           | T <sub>C</sub> = 25 °C  | 6    | A    |
|   |                                   | T <sub>C</sub> = 100 °C | 3.5  |      |
| Pulsed Drain Current <sup>a</sup>   | I <sub>DM</sub>                   | 18                      |      |      |
| Linear Derating Factor  |                                   | 1.67                    | W/°C |      |
| Single Pulse Avalanche Energy <sup>b</sup>                                | E <sub>AS</sub>                   | 650                     | mJ   |      |
| Maximum Power Dissipation   | P <sub>D</sub>                    | 140                     | W    |      |
| Operating Junction and Storage Temperature Range                          | T <sub>J</sub> , T <sub>stg</sub> | -55 to +150             | °C   |      |
| Drain-Source Voltage Slope  | dV/dt                             | T <sub>J</sub> = 125 °C | 50   | V/ns |
| Reverse Diode dV/dt <sup>d</sup>  |                                   | 15                      |      |      |
| Soldering Recommendations (Peak Temperature) <sup>c</sup>                 | for 10 s                          | 260                     | °C   |      |

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- V<sub>DD</sub> = 100 V, starting T<sub>J</sub> = 25 °C, L = 28.2 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 3A.
- 1.6 mm from case.
- I<sub>SD</sub> ≤ I<sub>D</sub>, dI/dt = 100 A/μs, starting T<sub>J</sub> = 25 °C.

| THERMAL RESISTANCE RATINGS       |            |      |      |      |
|----------------------------------|------------|------|------|------|
| PARAMETER                        | SYMBOL     | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient      | $R_{thJA}$ | -    | 62   | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | -    | 0.7  |      |

| SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted) |                     |   |   |  |       |           |               |
|---|---------------------|---|---|--|-------|-----------|---------------|
| PARAMETER   | SYMBOL              | TEST CONDITIONS   |   | MIN.                                   | TYP.  | MAX.      | UNIT          |
| <b>Static</b>   |                     |   |   |  |       |           |               |
| Drain-Source Breakdown Voltage  | $V_{DS}$            | $V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$  |   | 800                                    | -     | -         | V             |
| $V_{DS}$ Temperature Coefficient  | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$   |   | -                                      | 0.70  | -         | V/°C          |
| Gate-Source Threshold Voltage (N)   | $V_{GS(th)}$        | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$   |   | 2.5                                    | -     | 4.5       | V             |
| Gate-Source Leakage   | $I_{GSS}$           | $V_{GS} = \pm 20\text{ V}$  |   | -                                      | -     | $\pm 100$ | nA            |
|   |                     | $V_{GS} = \pm 30\text{ V}$  |   | -                                      | -     | $\pm 1$   | $\mu\text{A}$ |
| Zero Gate Voltage Drain Current   | $I_{DSS}$           | $V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$  |   | -                                      | -     | 1         | $\mu\text{A}$ |
|   |                     | $V_{DS} = 640\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$   |   | -                                      | -     | 100       |               |
| Drain-Source On-State Resistance  | $R_{DS(on)}$        | $V_{GS} = 10\text{ V}$  | $I_D = 2\text{ A}$                        | -                                      | 0.800 | -         | $\Omega$      |
| Forward Transconductance  | $g_{fs}$            | $V_{DS} = 30\text{ V}, I_D = 2\text{ A}$  |   | -                                      | 5.6   | -         | S             |
| <b>Dynamic</b>  |                     |   |   |  |       |           |               |
| Input Capacitance   | $C_{iss}$           | $V_{GS} = 0\text{ V},$<br>$V_{DS} = 100\text{ V},$<br>$f = 1\text{ MHz}$  |   | -                                      | 1300  | -         | pF            |
| Output Capacitance  | $C_{oss}$           |   |   | -                                      | 80    | -         |               |
| Reverse Transfer Capacitance  | $C_{rss}$           |   |   | -                                      | 4     | -         |               |
| Effective Output Capacitance, Energy Related <sup>a</sup>                   | $C_{o(er)}$         | $V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$   |   | -                                      | 62    | -         |               |
| Effective Output Capacitance, Time Related <sup>b</sup>                     | $C_{o(tr)}$         |   |   | -                                      | 213   | -         |               |
| Total Gate Charge   | $Q_g$               | $V_{GS} = 10\text{ V}$  | $I_D = 8\text{ A}, V_{DS} = 520\text{ V}$ | -                                      | 9.6   | -         | nC            |
| Gate-Source Charge  | $Q_{gs}$            |   |   | -                                      | 15    | -         |               |
| Gate-Drain Charge   | $Q_{gd}$            |   |   | -                                      | 1.9   | -         |               |
| Turn-On Delay Time  | $t_{d(on)}$         | $V_{DD} = 520\text{ V}, I_D = 8\text{ A},$<br>$V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$   |   | -                                      | 18    | 25        | ns            |
| Rise Time   | $t_r$               |   |   | -                                      | 24    | 55        |               |
| Turn-Off Delay Time   | $t_{d(off)}$        |   |   | -                                      | 8.0   | -         |               |
| Fall Time   | $t_f$               |   |   | -                                      | 1.2   | -         |               |
| Gate Input Resistance   | $R_g$               |   |   | $f = 1\text{ MHz}, \text{ open drain}$ |       | -         |               |
| <b>Drain-Source Body Diode Characteristics</b>                              |                     |   |   |  |       |           |               |
| Continuous Source-Drain Diode Current                                       | $I_S$               | MOSFET symbol showing the integral reverse p-n junction diode  |   | -                                      | -     | 6         | A             |
| Pulsed Diode Forward Current  | $I_{SM}$            |   |   | -                                      | -     | 18        |               |
| Diode Forward Voltage   | $V_{SD}$            | $T_J = 25\text{ }^\circ\text{C}, I_S = 8\text{ A}, V_{GS} = 0\text{ V}$   |   | -                                      | -     | 1.5       | V             |
| Reverse Recovery Time   | $t_{rr}$            | $T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 8\text{ A},$<br>$di/dt = 100\text{ A}/\mu\text{s}, V_R = 400\text{ V}$                                 |   | -                                      | 475   | -         | ns            |
| Reverse Recovery Charge   | $Q_{rr}$            |   |   | -                                      | 5.8   | -         | $\mu\text{C}$ |
| Reverse Recovery Current  | $I_{RRM}$           |   |   | -                                      | 35    | -         | A             |

**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .
- b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Fig. 1 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**



**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**

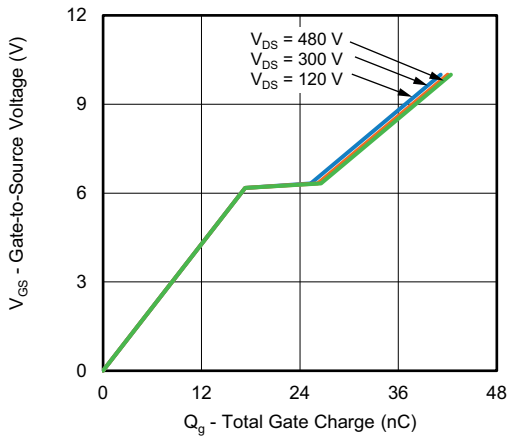


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 10 - Maximum Drain Current vs. Case Temperature



Fig. 8 - Typical Source-Drain Diode Forward Voltage

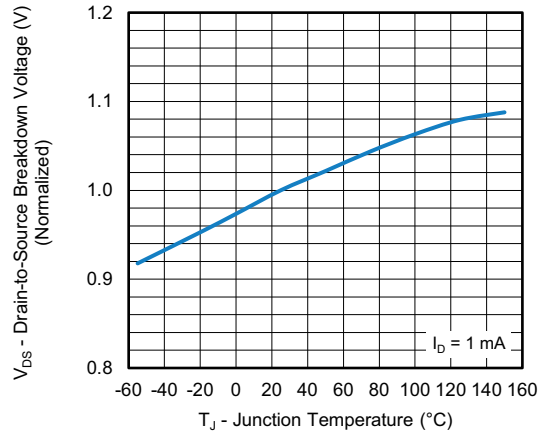


Fig. 11 - Temperature vs. Drain-to-Source Voltage



Fig. 9 - Maximum Safe Operating Area

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case



Fig. 13 - Switching Time Test Circuit



Fig. 16 - Unclamped Inductive Waveforms



Fig. 14 - Switching Time Waveforms



Fig. 17 - Basic Gate Charge Waveform

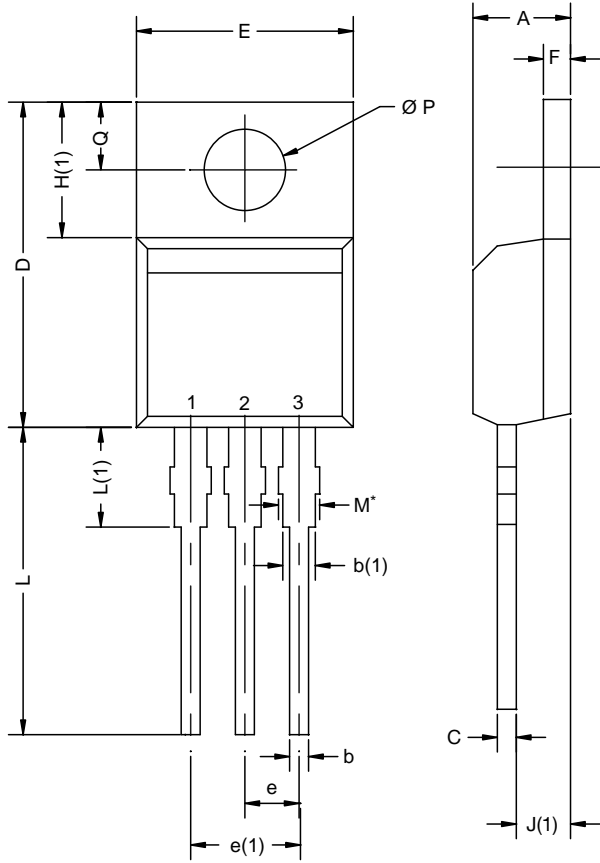


Fig. 15 - Unclamped Inductive Test Circuit



Fig. 18 - Gate Charge Test Circuit

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| DIM.            | MILLIMETERS |       | INCHES |       |
|-----------------|-------------|-------|--------|-------|
|                 | MIN.        | MAX.  | MIN.   | MAX.  |
| A               | 4.25        | 4.65  | 0.167  | 0.183 |
| b               | 0.69        | 1.01  | 0.027  | 0.040 |
| b(1)            | 1.20        | 1.73  | 0.047  | 0.068 |
| c               | 0.36        | 0.61  | 0.014  | 0.024 |
| D               | 14.85       | 15.49 | 0.585  | 0.610 |
| E               | 10.04       | 10.51 | 0.395  | 0.414 |
| e               | 2.41        | 2.67  | 0.095  | 0.105 |
| e(1)            | 4.88        | 5.28  | 0.192  | 0.208 |
| F               | 1.14        | 1.40  | 0.045  | 0.055 |
| H(1)            | 6.09        | 6.48  | 0.240  | 0.255 |
| J(1)            | 2.41        | 2.92  | 0.095  | 0.115 |
| L               | 13.35       | 14.02 | 0.526  | 0.552 |
| L(1)            | 3.32        | 3.82  | 0.131  | 0.150 |
| $\varnothing P$ | 3.54        | 3.94  | 0.139  | 0.155 |
| Q               | 2.60        | 3.00  | 0.102  | 0.118 |

ECN: X12-0208-Rev. N, 08-Oct-12  
DWG: 5471

Notes

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM

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