

FDP8441-VB Datasheet

N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS}	40	V
$R_{DS(on)}$ $V_{GS} = 10\text{ V}$	6	m Ω
I_D	110	A
Configuration	Single	

FEATURES

- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested



RoHS
COMPLIANT

APPLICATIONS

- Synchronous Rectification
- Power Supplies

TO-220AB



G D S
Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	40	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 175\text{ }^\circ\text{C}$)	I_D	$T_C = 25\text{ }^\circ\text{C}$	110 ^{a, c}	
		$T_C = 70\text{ }^\circ\text{C}$	90 ^c	
		$T_A = 25\text{ }^\circ\text{C}$	31 ^b	
		$T_A = 70\text{ }^\circ\text{C}$	25 ^b	
Pulsed Drain Current	I_{DM}	270	A	
Avalanche Current Pulse	I_{AS}	85		
Single Pulse Avalanche Energy	E_{AS}	320		
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	110 ^{a, c}	
		$T_A = 25\text{ }^\circ\text{C}$	2.6 ^b	
Maximum Power Dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	312 ^a	
		$T_C = 70\text{ }^\circ\text{C}$	200	
		$T_A = 25\text{ }^\circ\text{C}$	3.13 ^b	
		$T_A = 70\text{ }^\circ\text{C}$	2.0 ^b	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^b	R_{thJA}	32	40	°C/W	
Maximum Junction-to-Case	R_{thJC}	0.33	0.4		

Notes:

a. Based on $T_C = 25\text{ }^\circ\text{C}$.

b. Surface Mounted on 1" x 1" FR4 board.

c. Calculated based on maximum junction temperature. Package limitation current is 110 A.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		41		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.2		2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	120			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		6		m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		7		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		180		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2900		pF
Output Capacitance	C_{oss}			750		
Reverse Transfer Capacitance	C_{rss}			310		
Total Gate Charge	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		130		nC
Gate-Source Charge	Q_{gs}			20		
Gate-Drain Charge	Q_{gd}			32		
Gate Resistance	R_g	$f = 1\text{ MHz}$		0.85	1.3	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 1.0\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		20	30	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			77	115	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 1.0\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		102	155	
Rise Time	t_r			62	95	
Turn-Off Delay Time	$t_{d(off)}$			180	270	
Fall Time	t_f			60	90	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			110	A
Pulse Diode Forward Current ^a	I_{SM}				200	
Body Diode Voltage	V_{SD}	$I_S = 20\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		50	75	ns
Body Diode Reverse Recovery Charge	Q_{rr}			70	105	nC
Reverse Recovery Fall Time	t_a			30		ns
Reverse Recovery Rise Time	t_b			20		

Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Output Characteristics



Transfer Characteristics



Transconductance



On-Resistance vs. Drain Current



Capacitance



Gate Charge

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



On-Resistance vs. Junction Temperature



Forward Diode Voltage vs. Temperature



On-Resistance vs. Gate-to-Source Voltage



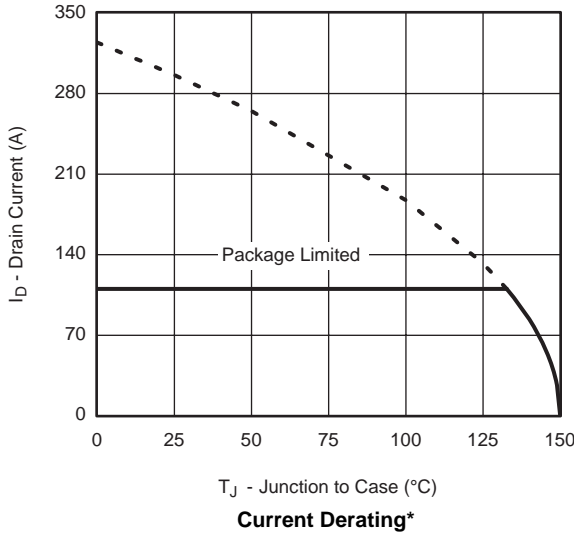
Threshold Voltage



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12
DWG: 5471

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

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