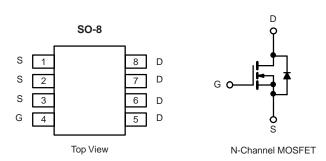


N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^d	Q _g (Typ.)		
60	0.025 at V _{GS} = 10 V	7.6	10.5 nC		
	0.030 at V _{GS} = 4.5 V	6.5	10.5110		



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Optimized for "Low Side" Synchronous Rectifier Operation
- 100 % R_g and UIS Tested



ROHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

CCFL Inverter

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage		V_{GS}	± 20	v
	T _C = 25 °C		7.6 ^a	
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C		6.8	
Continuous Diam Current (1) = 150 °C)	T _A = 25 °C	l _D	6.1 ^{b, c}	
	T _A = 70 °C		4.8 ^{b, c}	
Pulsed Drain Current	I _{DM}	25	A	
	T _C = 25 °C		4.2	
Continuous Source-Drain Diode Current	T _A = 25 °C	ls —	2.1 ^{b, c}	
Avalanche Current	1 0411	I _{AS}	15	
Single-Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	11.2	mJ
	T _C = 25 °C		5	
Maniana Banas Biodestina	T _C = 70 °C		3.2	
Maximum Power Dissipation	T _A = 25 °C	P _D	2.5 ^{b, c}	W
	T _A = 70 °C		1.6 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	38	50	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	20	25	-C/VV	

Notes:

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 85 °C/W.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			,	•			
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V	
V _{DS} Temperature Coefficient	AVpe/Tu			55		m\//9C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 6.3		mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.2		2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zara Cata Valtaga Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1 1		
Zero Gate Voltage Drain Current		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			10	μA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	25			Α	
Davis Ossans Os Otata Basista sa	D	V _{GS} = 10 V, I _D = 4.6 A		0.025	0.030		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 4.2 \text{ A}$		0.035	0.040	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 4.6 A		20		S	
Dynamic ^b			•	•			
Input Capacitance	C _{iss}			1100		pF	
Output Capacitance	C _{oss}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		90			
Reverse Transfer Capacitance	C _{rss}			55			
Total Cata Chausa		$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4.6 \text{ A}$		21	32		
Total Gate Charge				10.5	16		
Gate-Source Charge	Q_{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 4.6 \text{ A}$		3.5		nC	
Gate-Drain Charge	Q_{gd}			4.2		1	
Gate Resistance	R _g	f = 1 MHz		3.3	5	Ω	
Turn-On Delay Time	t _{d(on)}			20	30		
Rise Time	t _r	$V_{DD} = 30 \text{ V, R}_{L} = 5.4 \Omega$		150	225		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong 5.6 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		20	30		
Fall Time	t _f	_		60	90		
Turn-On Delay Time	t _{d(on)}			10	15	ns	
Rise Time	t _r	$V_{DD} = 30 \text{ V, R}_{L} = 5.4 \Omega$		15	25	1	
Turn-Off DelayTime	t _{d(off)}	$I_{D} \cong 5.6 \text{ A}, V_{GEN} = 10 \text{ V}, R_{g} = 1 \Omega$		25	40		
Fall Time	t _f	_		10	15		
Drain-Source Body Diode Characterist	ics		,	•			
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			4.2	۸	
Pulse Diode Forward Current ^a	I _{SM}				25	Α	
Body Diode Voltage	V _{SD}	I _S = 2 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	-		25	50	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			25	50	nC	
Reverse Recovery Fall Time	t _a	$I_F = 5.5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 °\text{C}$		19			
Reverse Recovery Rise Time	t _b			6		ns	

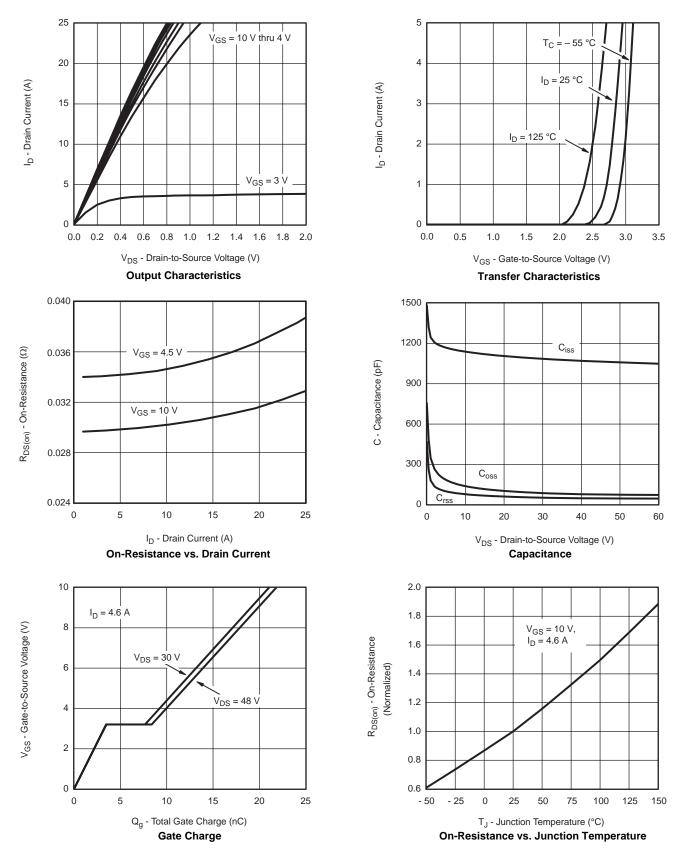
Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

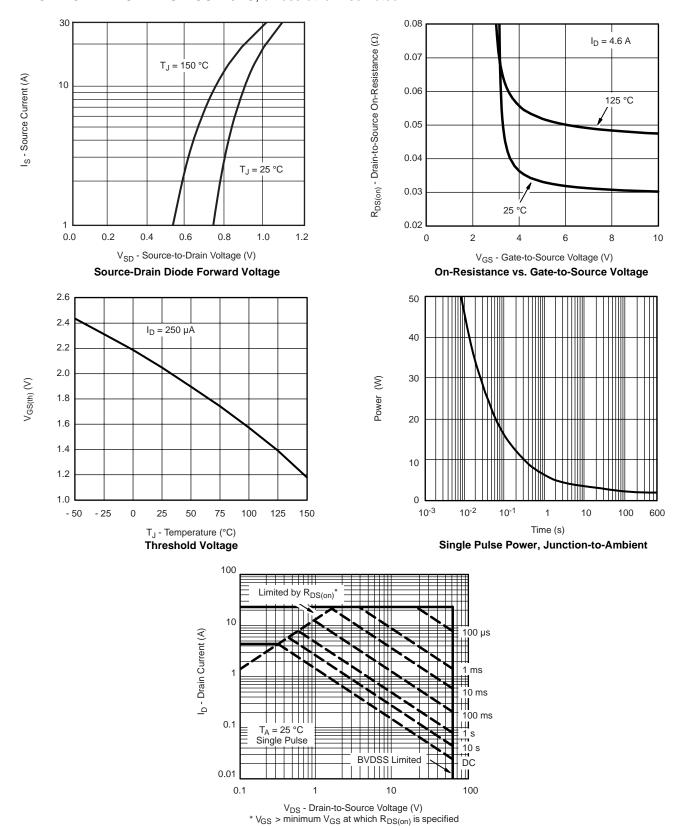
a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$

b. Guaranteed by design, not subject to production testing.



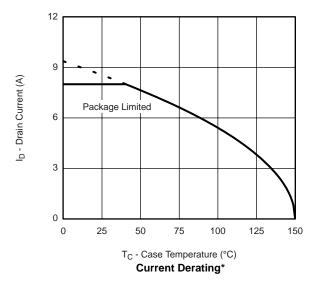


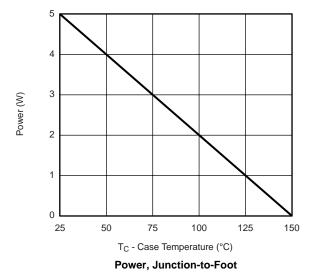




Safe Operating Area

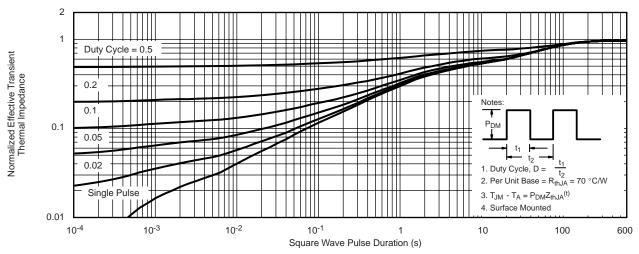




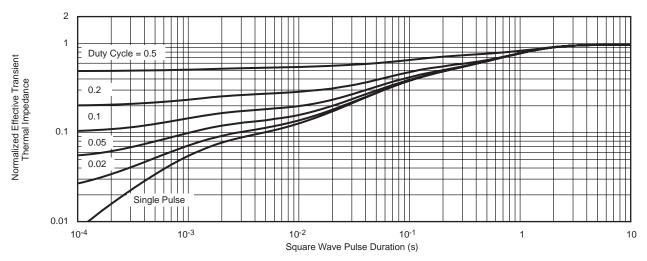


^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package





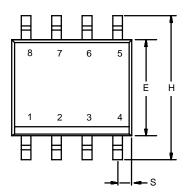
Normalized Thermal Transient Impedance, Junction-to-Ambient



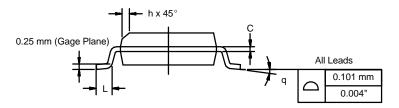
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEADJEDEC Part Number: MS-012







	MILLIMETERS		INC	HES		
DIM	Min	Max	Min	Max		
А	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
FCN: C-06527-Rev 11-Sen-06						

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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