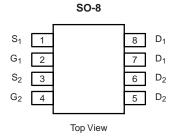


## **Dual P-Channel 30-V (D-S) MOSFET**

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>d, e</sup>	Q <sub>g</sub> (Typ.)			
- 30	0.021 at V <sub>GS</sub> = - 10 V	- 9.5	15 nC			
	0.028 at V <sub>GS</sub> = - 4.5 V	- 8.0	13110			



#### **FEATURES**

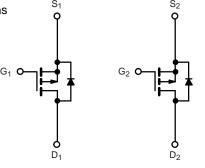
- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % UIS Tested

# Pb-free

RoHS

#### **APPLICATIONS**

- · Load Switches
  - Notebook PCs
  - Desktop PCs
  - Game Stations



P-Channel MOSFET

P-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> T <sub>A</sub> = 25 °C, unless otherwise noted					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	- 30	V		
Gate-Source Voltage	$V_{GS}$	± 20	V		
	T <sub>C</sub> = 25 °C		- 9.5 <sup>e</sup>		
Continuous Drain Current (T <sub>.I</sub> = 150 °C)	T <sub>C</sub> = 70 °C	] [	- 8.0 <sup>e</sup>		
Continuous Diain Current (1) = 130 C)	T <sub>A</sub> = 25 °C	l lD	- 8.3 <sup>a, b</sup>		
	T <sub>A</sub> = 70 °C		- 7.9 <sup>a, b</sup>	Α	
Pulsed Drain Current	I <sub>DM</sub>	- 32 <sup>e</sup>			
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	I-	- 4.1		
Continuous Source-Dialii Diode Current	T <sub>A</sub> = 25 °C	- I <sub>S</sub>	- 2.0 <sup>a, b</sup>		
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	- 20		
Single-Pulse Avalanche Energy	L = U.1 IIIII	E <sub>AS</sub>	20	mJ	
	T <sub>C</sub> = 25 °C		5.0		
Maximum Dawar Dissipation	T <sub>C</sub> = 70 °C	$P_{D}$	3.2	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	] <sup>[D</sup> [	2.5 <sup>a, b</sup>	VV	
	T <sub>A</sub> = 70 °C	1	1.6 <sup>a, b</sup>		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a, c</sup>	t ≤ 10 s	R <sub>thJA</sub>	38	50	°C/W	
Maximum Junction-to-Foot	Steady State	$R_{thJF}$	20	25	C/VV	

#### Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. Maximum under Steady State conditions is 85 °C/W.
- d. Based on  $T_C = 25$  °C.
- e. Limited by package.



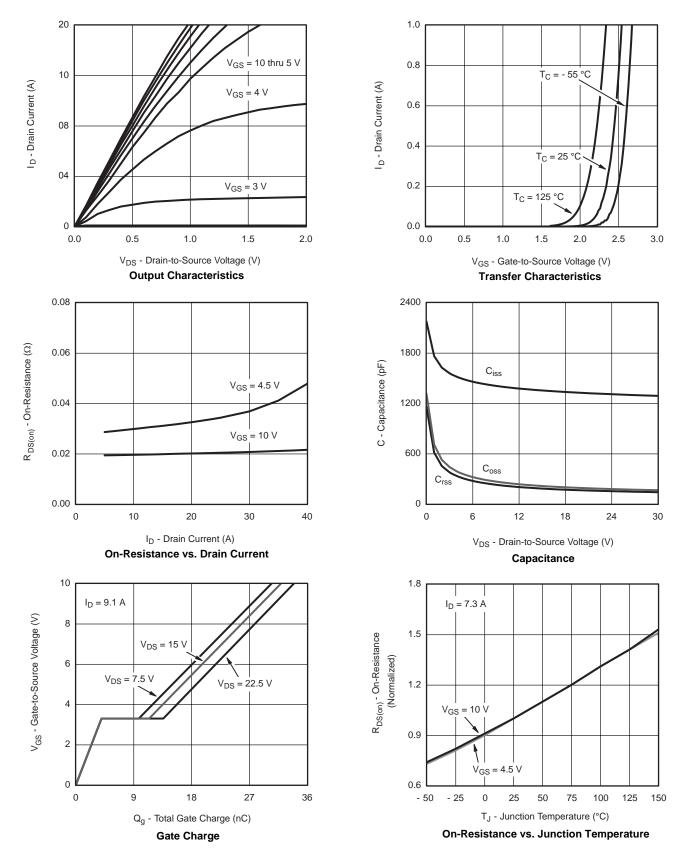
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = - 250 μA		- 31		m\//9C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	Ι <sub>D</sub> = - 250 μΑ		4.5		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	- 1.0		- 3.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Oata Waltana Basis Osamast	I <sub>DSS</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V			- 1		
Zero Gate Voltage Drain Current		V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 5	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge -10 \text{ V}, V_{GS} = -10 \text{ V}$	- 30			Α	
Davis Ossans Os Otata Basista and	D	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 7.3 A		0.021			
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 6.2 A		0.028		Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 9.1 A		23		S	
Dynamic <sup>b</sup>					•		
Input Capacitance	C <sub>iss</sub>			1350		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		215			
Reverse Transfer Capacitance	C <sub>rss</sub>			185			
Tatal Cata Charra		$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -9.1 \text{ A}$		32 50	50	nC	
Total Gate Charge				15	25		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -9.1 \text{ A}$		4			
Gate-Drain Charge	$Q_{gd}$			7.5			
Gate Resistance	R <sub>g</sub>	f = 1 MHz		5.8		Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			10	15		
Rise Time	t <sub>r</sub>	$V_{DD} = -15 \text{ V}, R_{L} = 15 \Omega$		8	15		
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong$ - 1 A, $V_{GEN}$ = - 10 V, $R_g$ = 1 $\Omega$		45	70		
Fall Time	t <sub>f</sub>	_		12	25		
Turn-On Delay Time	t <sub>d(on)</sub>			42	70	ns	
Rise Time	t <sub>r</sub>	$V_{DD} = -15 \text{ V}, R_{L} = 15 \Omega$		35	60	<u></u>	
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong$ - 1 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 1 $\Omega$		40	70		
Fall Time	ì,	<u> </u>		16	30		
<b>Drain-Source Body Diode Characterist</b>	ics						
Continous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 4.1	٨	
Pulse Diode Forward Current	I <sub>SM</sub>	-			- 32	Α	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = -2 A, V <sub>GS</sub> = 0 V		- 0.75	- 1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	, GS -		34	60	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1 2 A dl/dt 100 A/va T 25 °C		22	40	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = -2 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	4/μs, 1 <sub>J</sub> = 25 °C	11			
Reverse Recovery Rise Time	t <sub>b</sub>			23		ns	

#### Notes:

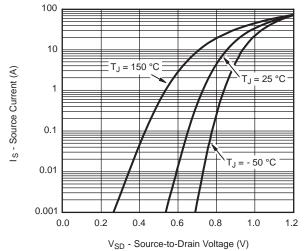
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

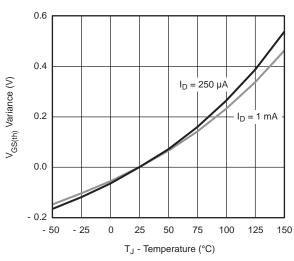




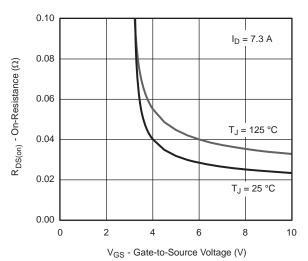




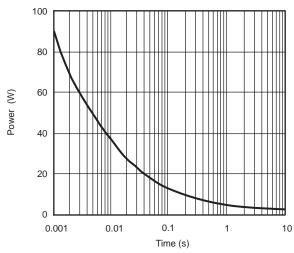
Source-Drain Diode Forward Voltage



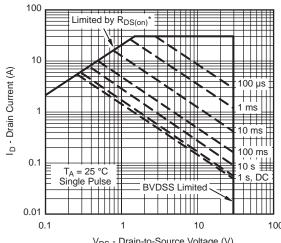
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

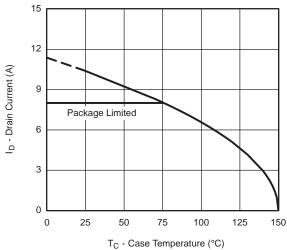


V<sub>DS</sub> - Drain-to-Source Voltage (V)

Safe Operating Area

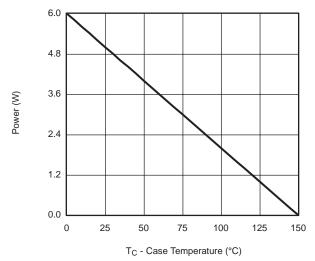
<sup>\*</sup>  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



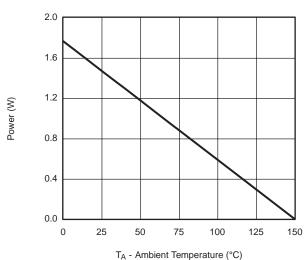




#### **Current Derating\***



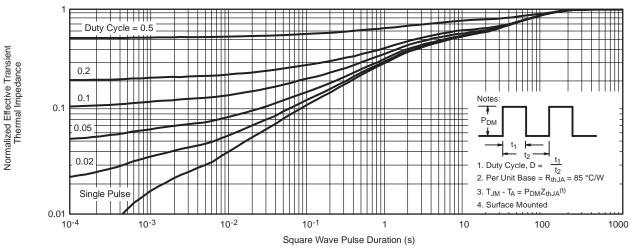




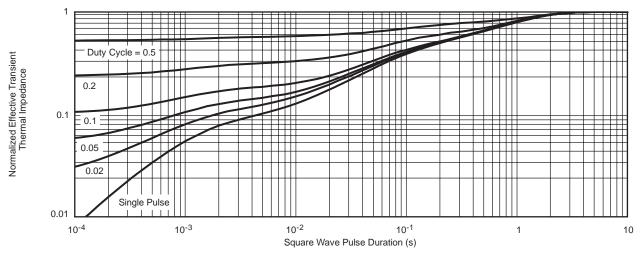
Power Derating, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



**SOIC (NARROW): 8-LEAD**JEDEC Part Number: MS-012







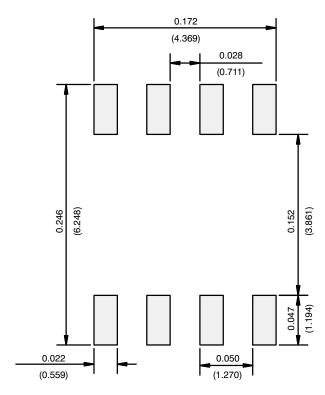
	MILLIMETERS		INC	HES	
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
FCN: C-06527-Rev   11-Sen-06					

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



#### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)



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