

# N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)		
40	0.0045 at V <sub>GS</sub> = 10 V	18	8 nC		
40	$0.0065 \text{ at V}_{GS} = 4.5 \text{ V}$	14.5	OIIC		

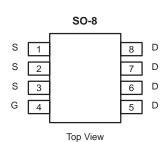
#### **FEATURES**

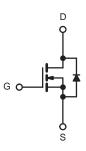
- Halogen-free According to IEC 61249-2-21
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested

# COMPLIANT HALOGEN FREE

#### **APPLICATIONS**

- Notebook CPU Core
  - High-Side Switch





N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	40	V	
Gate-Source Voltage		$V_{GS}$	± 20	v	
	T <sub>C</sub> = 25 °C		18		
Continuous Drain Current (T <sub>.I</sub> = 150 °C)	T <sub>C</sub> = 70 °C	T	13.5		
Continuous Brain Current (1) = 130 C)	T <sub>A</sub> = 25 °C	l <sub>D</sub>	12 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C	1	9.6 <sup>b, c</sup>	^	
Pulsed Drain Current		I <sub>DM</sub>	50	A	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	1-	4.5		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2.2 <sup>b, c</sup>		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	20		
Avalanche Energy	L = 0.1 IIII	E <sub>AS</sub>	20	mJ	
	T <sub>C</sub> = 25 °C		5		
Maximum Dawar Dissipation	T <sub>C</sub> = 70 °C	P <sub>D</sub>	3.2	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C		2.5 <sup>b, c</sup>	VV	
	T <sub>A</sub> = 70 °C		1.6 <sup>b, c</sup>		
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	$R_{thJA}$	38	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	20	25	C/ V V		

- a. Based on T<sub>C</sub> = 25 °C.
  b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 85 °C/W.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	2/T <sub>1</sub>		34		\//00	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	- I <sub>D</sub> = 250 μA		- 4.7		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1.0		3.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Cata Valtana Brain Comment	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μA	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10 P		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
	В	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.0038			
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$		0.0057		Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		30		S	
Dynamic <sup>b</sup>			•	•			
Input Capacitance	C <sub>iss</sub>			985		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		205			
Reverse Transfer Capacitance	C <sub>rss</sub>	1		76			
Total Cata Channa	0	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$		18	27		
Total Gate Charge	Q <sub>g</sub>		8	12			
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$		2.4		nC	
Gate-Drain Charge	$Q_{gd}$			2.3			
Gate Resistance	$R_g$	f = 1 MHz	0.3	1.3	2.6	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			14	25		
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega$		12	24		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		19	35		
Fall Time	t <sub>f</sub>			9	18	ne	
Turn-On Delay Time	t <sub>d(on)</sub>			8	16	ns -	
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega$		10	20		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		16	30		
Fall Time	t <sub>f</sub>			9	18		
Drain-Source Body Diode Characterist	cs						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			4.5	Λ	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				50	Α	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 3 A		0.76	1.1	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			14	28	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1 = 10 A dl/dt = 100 A/us T = 25 °C		5	10	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$		8			
Reverse Recovery Rise Time t <sub>b</sub>		1		6		ns	

#### Notes:

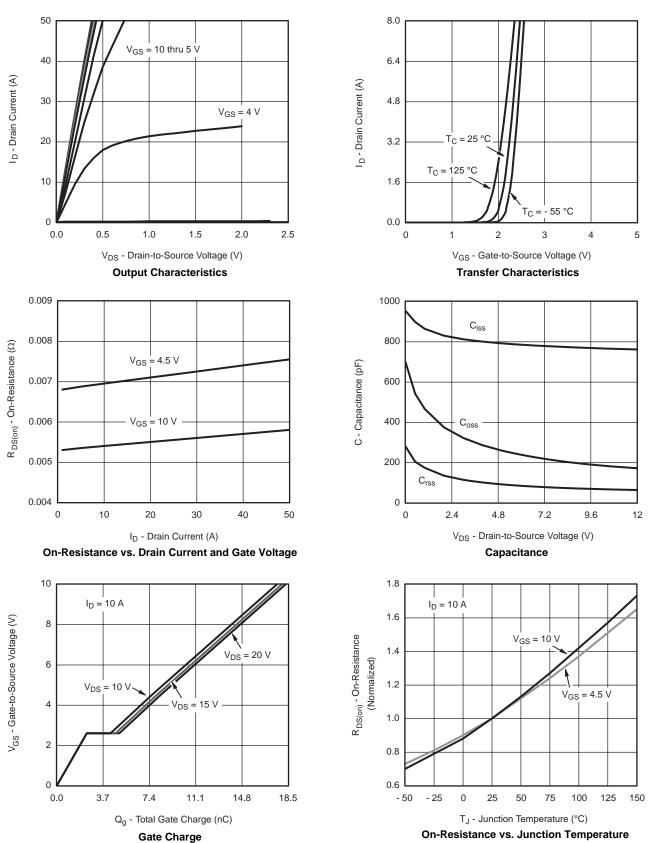
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$ 

b. Guaranteed by design, not subject to production testing.

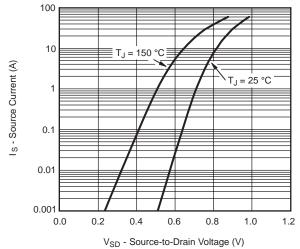


### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

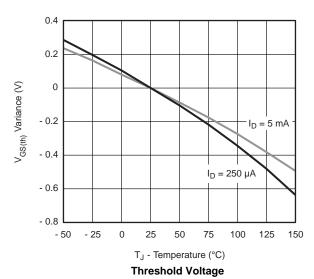




#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

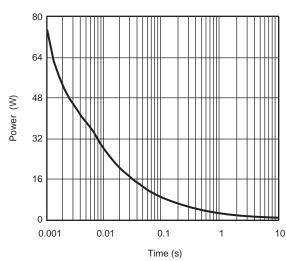


Source-Drain Diode Forward Voltage

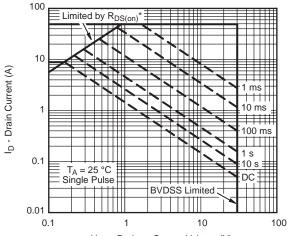


0.012  $I_D = 10 \text{ Å}$ 0.010  $R_{DS(on)}$  - On-Resistance  $(\Omega)$ 0.008 0.006  $T_J = 125$  °C 0.004 T<sub>J</sub> = 25 °C 0.002 0 2 3 4 5 8 9 10 V<sub>GS</sub> - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



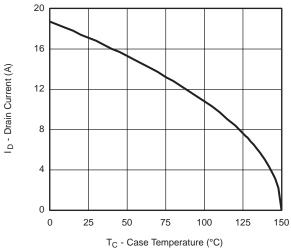
V<sub>DS</sub> - Drain-to-Source Voltage (V)

\*  $V_{GS} > \mbox{minimum } V_{GS}$  at which  $R_{DS(on)}$  is specified

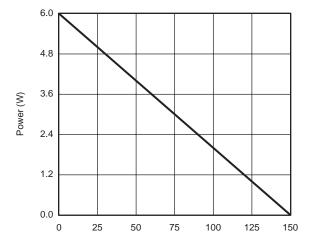
Safe Operating Area, Junction-to-Ambient



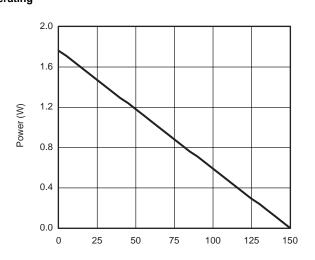
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



### Current Derating\*







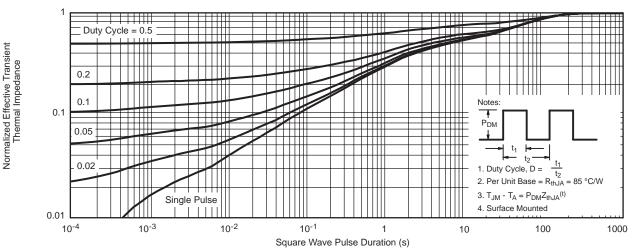
T<sub>A</sub> - Ambient Temperature (°C) **Power Derating, Junction-to-Foot** 

5

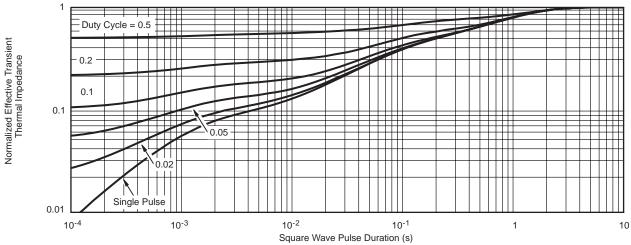
<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



#### TYPICAL CHARACTERISTICS 25 C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

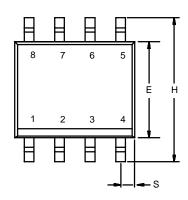


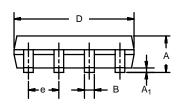
Normalized Thermal Transient Impedance, Junction-to-Foot

服务热线:400-655-8788 6



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	INCHES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
FCN: C-06527-Rev I 11-Sen-06						

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)



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DMN2080UCB4-7 DMN61D9UWQ-13 US6M2GTR DMN31D5UDJ-7 DMP22D4UFO-7B DMN1006UCA6-7 DMN16M9UCA6-7
STF5N65M6 IRF40H233XTMA1 STU5N65M6 DMN6022SSD-13 DMN13M9UCA6-7 DMTH10H4M6SPS-13 DMN2990UFB-7B
IPB80P04P405ATMA2 2N7002W-G MCAC30N06Y-TP MCQ7328-TP BXP7N65D BXP4N65F AOL1454G WMJ80N60C4 BXP2N20L
BXP2N65D BXT1150N10J BXT1700P06M TSM60NB380CP ROG RQ7L055BGTCR DMNH15H110SK3-13 SLF10N65ABV2
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