

N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY					
V_{DS}	100	V			
$R_{DS(on)} V_{GS} = 10 V$	32	mΩ			
I _D	9	Α			
Configuration	Single				

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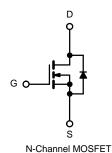
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q_{gd} for Switching Losses
- 100 % R_g Tested
- 100 % Avalanche Tested
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

· Primary Side Switch



ΔBS	OLU	ITE	МΔ	XII	иUN	l F
		То	p Viev	N		
G	4				5	D
S	3				6	D
S	2				7	D
S	1				8	D

SO-8

Parameter Drain-Source Voltage		Symbol	Limit	Unit
		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
	T _C = 25 °C		9	
Continuous Drain Current (T _{.1} = 150 °C)	$T_C = 70 ^{\circ}C$	I_	6	
Continuous Drain Current (1) = 150 C)	T _A = 25 °C	I _D	6 ^{b, c}	
	T _A = 70 °C		5 ^{b, c}	A
Pulsed Drain Current		I _{DM}	40	
Continuous Source-Drain Diode Current	T _C = 25 °C		7	
Continuous Source-Diam Diode Current	T _A = 25 °C	I _S	3.8 ^{b, c}	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	30	
Single Pulse Avalanche Energy		E _{AS}	112	mJ
Maximum Power Dissipation	T _C = 25 °C		14	
	T _C = 70 °C	P _D	5	w
	$T_A = 25 ^{\circ}\text{C}$] ^{[D}]	4 ^{b, c}	VV
	T _A = 70 °C]	2 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stq}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	33	40	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	17	21	C/VV		

Notes

- a. Based on T_C = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under steady state conditions is 80 °C/W.



2

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V, } I_{D} = 250 \mu\text{A}$	100			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		172		>//06
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_{J}$	I _D = 230 μA		- 10		mV/°0
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	1.0		3.0	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zana Cata Valtana Brain Commant		V _{DS} = 100 V, V _{GS} = 0 V			1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	30			Α
Davis Course On Otata Basista and	()	$V_{GS} = 10 \text{ V, } I_D = 5 \text{ A}$	0.032			
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$		0.033	m	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 5 A		20		S
Dynamic ^b		-				
Input Capacitance	C _{iss}			1900		pF
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		150		
Reverse Transfer Capacitance	C _{rss}			50		
Fatal Oata Ohanna	Q_g $V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 5 \text{ A}$	28.5	28.5	43	
Total Gate Charge			23	35]	
Gate-Source Charge	Q _{gs}	$V_{DS} = 75 \text{ V}, V_{GS} = 8 \text{ V}, I_{D} = 5 \text{ A}$		8		- nC
Gate-Drain Charge	Q _{gd}			6.5		
Gate Resistance	R_{g}	f = 1 MHz		0.80	1.3	Ω
Turn-on Delay Time	t _{d(on)}			14	21	
Rise Time	t _r	V_{DD} = 50 V, R_L = 10 Ω		12	18	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 5 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		22	33	
Fall Time	t _f			6	10	no
Turn-On Delay Time	t _{d(on)}			16	24	ns
Rise Time	t _r	V_{DD} = 50 V, R_L = 10 Ω		12	18	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 5$ A, $V_{GEN} = 8$ V, $R_g = 1$ Ω		20	30	
Fall Time	t _f			7	12	
Drain-Source Body Diode Characteristi	cs					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			7.7	А
Pulse Diode Forward Current ^a	I _{SM}				50	^
Body Diode Voltage	V _{SD}	I _S = 2.6 A		0.77	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			63	95	ns
Body Diode Reverse Recovery Charge	Q _{rr}	L = 5 A dl/dt = 100 A/up T = 25 °C		110	165	nC
Reverse Recovery Fall Time	t _a	$I_F = 5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		49		na
Reverse Recovery Rise Time	t _b			14		ns

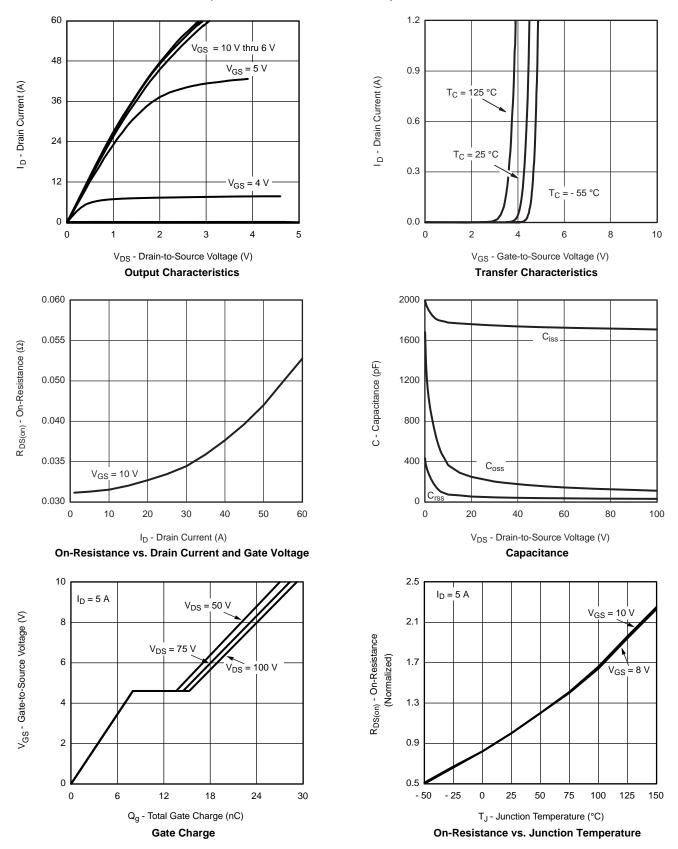
Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

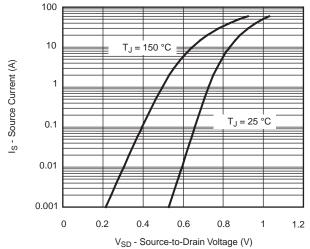
a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$

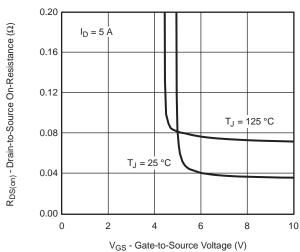
a. Guaranteed by design, not subject to production testing.





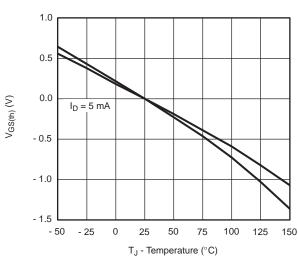


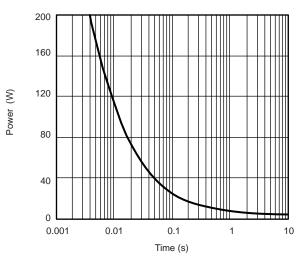




Source-Drain Diode Forward Voltage

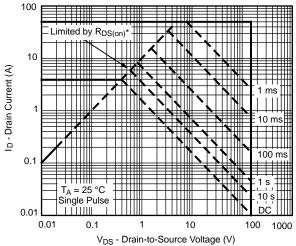






Threshold Voltage

Single Pulse Power, Junction-to-Ambient

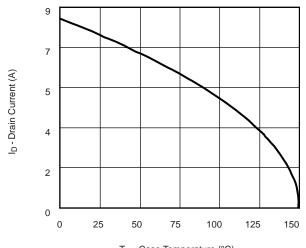


V_{DS} - Drain-to-Source Voltage (V)

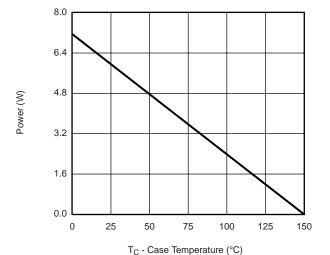
* V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

Safe Operating Area, Junction-to-Ambient

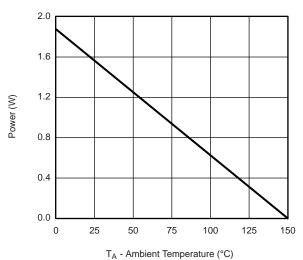




T_C - Case Temperature (°C) **Current Derating***



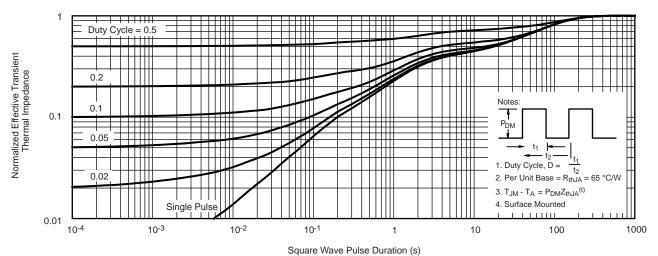
Power, Junction-to-Case



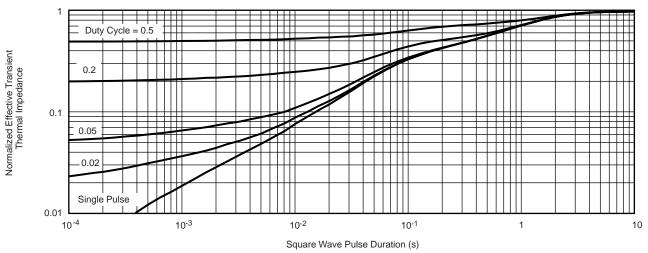
Power, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





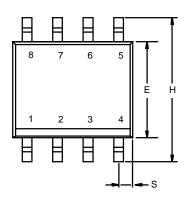
Normalized Thermal Transient Impedance, Junction-to-Ambient

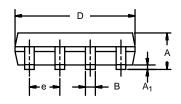


Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







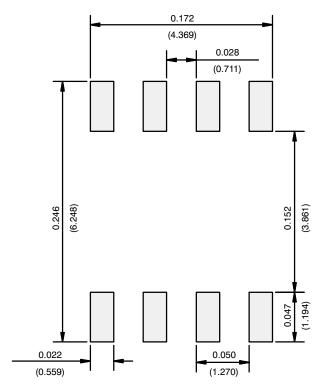
	MILLIMETERS		INC	HES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
FCN: C-06527-Rev I 11-Sen-06						

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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