

N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a			
60	0.024 at V _{GS} = 10 V	50			
	0.028 at V _{GS} = 4.5 V	40			

FEATURES

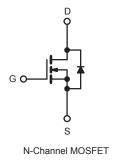
- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Logic-Level Gate Drive
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



Ο GDS

Top View

TO-220AB



ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	60	v	
Gate-Source Voltage			V _{GS}	± 20	l v	
Continuous Drain Current ^f	V_{GS} at 10 V $T_C = 25 \degree C$		L_	50		
Continuous Drain Current	VGS AL TO V	T _C = 100 °C	I _D	36	А	
Pulsed Drain Current ^a			I _{DM}	200		
Linear Derating Factor				1.0	W/°C	
Linear Derating Factor (PCB Mount) ^e				0.025	VV/ C	
Single Pulse Avalanche Energy ^b			E _{AS}	400	mJ	
Maximum Power Dissipation	T _C = 25 °C		р	150	W	
Maximum Power Dissipation (PCB Mount) ^e	T _A = 25 °C		P _D	3.7	vv	
Peak Diode Recovery dV/dt ^c			dV/dt	4.5	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg} - 55 to + 175		°C	
Soldering Recommendations (Peak Temperature) ^d	for 10 s			300 ^d		

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. $V_{DD} = 25 \text{ V}$, starting $T_J = 25 \text{ °C}$, $L = 179 \text{ }\mu\text{H}$, $R_g = 25 \Omega$, $I_{AS} = 51 \text{ A}$ (see fig. 12). c. $I_{SD} \le 51 \text{ A}$, dl/dt $\le 250 \text{ A/}\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_J \le 175 \text{ °C}$.

e. When mounted on 1" square PCB (FR-4 or G-10 material).

f. Current limited by the package, (die current = 51 A).

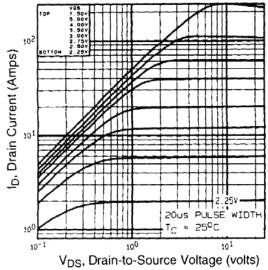
d. 1.6 mm from case.



THERMAL RESISTANCE RATI	NGS								
PARAMETER	SYMBOL	TYP		MAX.		UNIT			
Maximum Junction-to-Ambient	R _{thJA}	-	62						
Maximum Junction-to-Ambient (PCB Mount) ^a	R _{thJA}	-		40		°C/W			
Maximum Junction-to-Case (Drain)	R _{thJC}	- 1.0]			
lote When mounted on 1" square PCB (FR-4									
SPECIFICATIONS ($T_J = 25 \ ^{\circ}C$, u								1	
PARAMETER	SYMBOL	TES	T CONDIT	IONS	MIN.	TYP.	MAX.	UNIT	
Static		1			T	1			
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	= 0, I _D = 25	50 µA	60	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C,	$I_D = 1 \text{ mA}$	-	0.070	-	V/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$		1.0	-	2.5			
Gate-Source Leakage	I _{GSS}	N	V _{GS} = ± 10	V	-	-	± 100	nA	
Zero Gate Voltage Drain Current		V _{DS} =	= 60 V, V _{GS}	= 0 V	-	-	25		
	I _{DSS}	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 150 \text{ °C}$			-	-	250	μA	
	_	V _{GS} = 10 V	۱ _D	= 21 A ^b	-	0.024	-		
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 4.5 V			-	0.028	-	Ω	
Forward Transconductance	g _{fs}	V _{DS} = 25 V, I _D = 21A ^b		23	-	-	S		
Dynamic	0.0							I	
Input Capacitance	C _{iss}				_	190			
Output Capacitance	C _{oss}		$V_{GS} = 0 V,$ $V_{DS} = 25 V$		_	920	_	pF	
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz, see fig. 5		_	170	-	P		
Total Gate Charge	Qg	$V_{GS} = 5.0 \text{ V}$ $I_D = 51 \text{ A}, V_{DS} = 48 \text{ V},$		-	-	66	nC		
Gate-Source Charge	Q _{gs}				-	12			
Gate-Drain Charge	Q _{gs} Q _{gd}	VGS - 0.0 V	see fig	g. 6 and 13 ^b	_	_	43		
0					_	17	-		
Turn-On Delay Time	t _{d(on)}	-			-			4	
Rise Time	t _r	$V_{DD} = 30 \text{ V, } I_D = 51 \text{ A,}$ R _g = 4.6 Ω, R _D = 0.56 Ω, see fig. 10 ^b			230	-	ns		
Turn-Off Delay Time	t _{d(off)}			-	2	-			
Fall Time	t _f			-	110	-			
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH		
Internal Source Inductance	L _S			-	7.5	-			
Drain-Source Body Diode Characteristi	cs								
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	50 ^c	A		
Pulsed Diode Forward Current ^a	I _{SM}			-	-	200			
Body Diode Voltage	V _{SD}	$T_J = 25 \text{ °C}, I_S = 51 \text{ A}, V_{GS} = 0 \text{ V}^{b}$		-	-	2.5	V		
Body Diode Reverse Recovery Time	t _{rr}	$T_{J} = 25 \text{ °C}, I_{F} = 51 \text{ A}, dl/dt = 100 \text{ A}/\mu\text{s}^{b}$ Intrinsic turn-on time is negligible (turn		-	130	180	ns		
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.84	1.3	μC		
,	-11						<u> </u>		

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.
c. Current limited by the package, (Die Current = 51 A).





TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



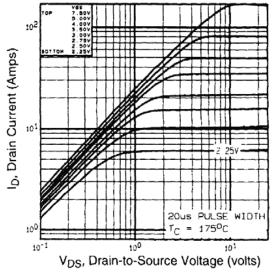
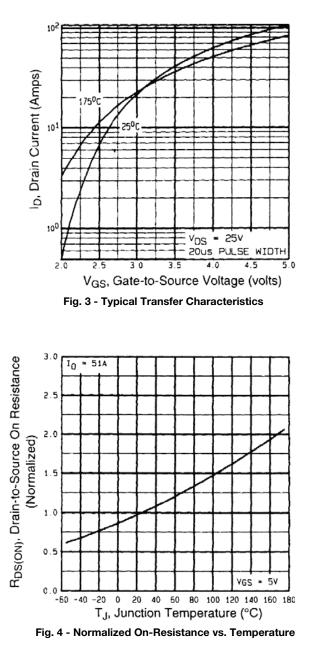


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C





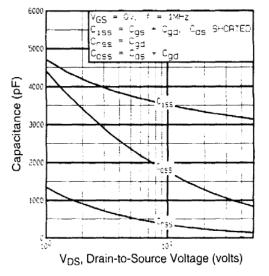


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

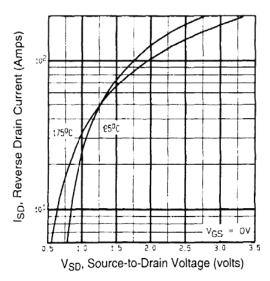


Fig. 7 - Typical Source-Drain Diode Forward Voltage

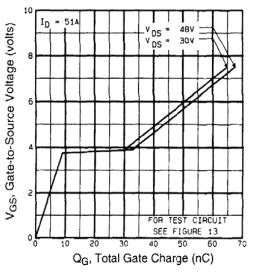
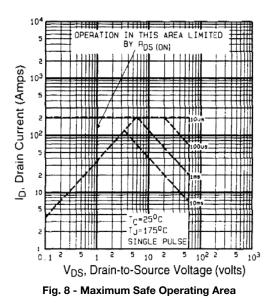


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage





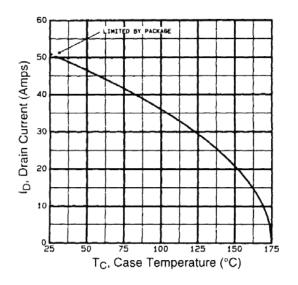


Fig. 9 - Maximum Drain Current vs. Case Temperature

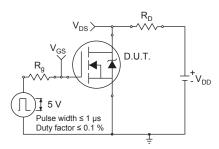


Fig. 10a - Switching Time Test Circuit

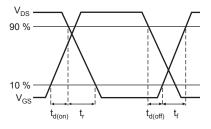
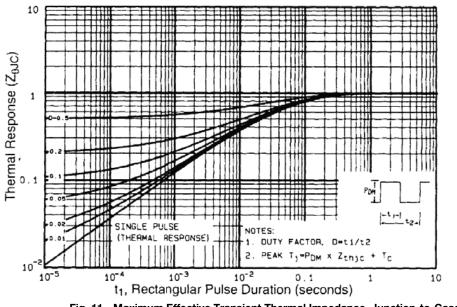


Fig. 10b - Switching Time Waveforms







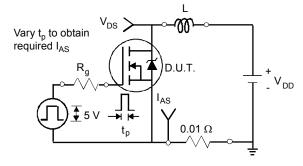


Fig. 12a - Unclamped Inductive Test Circuit

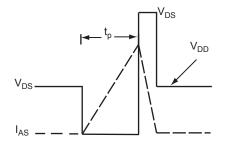


Fig. 12b - Unclamped Inductive Waveforms

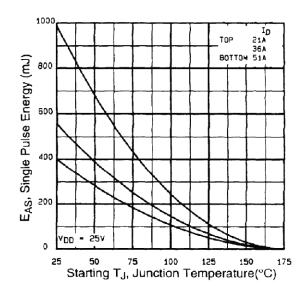


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

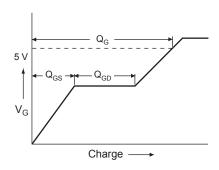


Fig. 13a - Basic Gate Charge Waveform

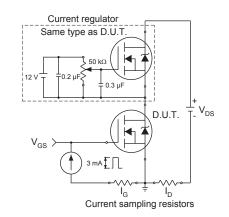
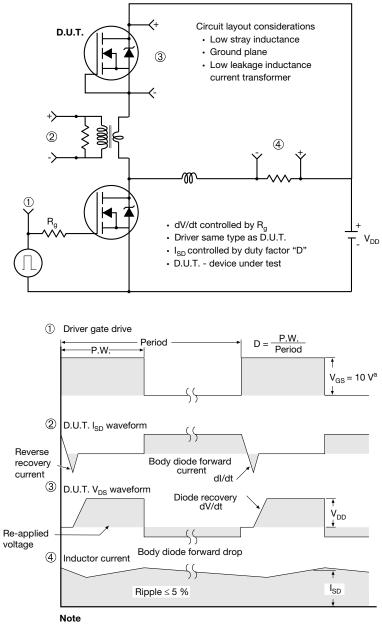


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit

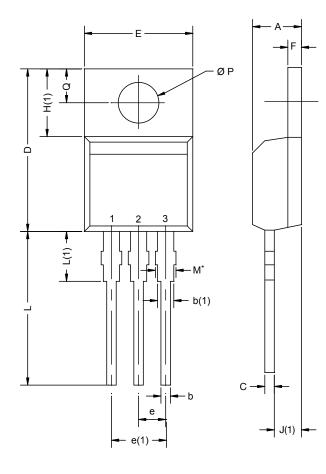


a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel



TO-220AB



	MILLIN	IETERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
А	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØΡ	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
ECN: X12- DWG: 547	0208-Rev. N, 1	08-Oct-12			

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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