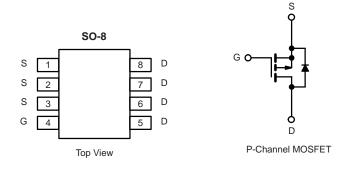


P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)		
- 40	0.010 at V_{GS} = - 10 V	- 16.1	33 nC		
- 40	0.014 at V _{GS} = - 4.5 V	- 13.3	33 110		



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Load Switch
- POL

ABSOLUTE MAXIMUM RATIN	I GS T _A = 25 °C,	unless othe	rwise noted	
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	- 40	V
Gate-Source Voltage		V _{GS}	± 20	V
	T _C = 25 °C	-	- 16.1	
Continuous Drain Current (T ₁ = 150 °C)	T _C = 70 °C		- 12.9	
Continuous Drain Current $(T_j = 150 \text{ C})$	T _A = 25 °C	I _D	- 10.2 ^{b, c}	
	T _A = 70 °C		- 8.2 ^{b, c}	Α
Pulsed Drain Current		I _{DM}	- 50	A
Continous Source-Drain Diode Current	T _C = 25 °C	– I _S	- 5.3	
	T _A = 25 °C		- 2.1 ^{b, c}	
Single Pulse Avalanche Current L = 0.1 ml		I _{AS}	- 28	
Single Pulse Avalanche Energy		E _{AS}	39	mJ
	T _C = 25 °C		6.3	
Maximum Power Dissipation	T _C = 70 °C	D_	4	W
	T _A = 25 °C	– P _D	2.5 ^{b, c}	VV
	T _A = 70 °C	1	1.6 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS							
	Symbol	Typical	Maximum	Unit			
$t \le 10 s$	R _{thJA}	37	50	°C/W			
Steady State	R _{thJF}	16	20	0/10			
	t ≤ 10 s	$\begin{tabular}{ c c c c } \hline Symbol \\ \hline t \le 10 \ s & R_{thJA} \end{tabular}$	SymbolTypical $t \le 10$ s R_{thJA} 37	SymbolTypicalMaximum $t \le 10$ s R_{thJA} 3750			

Notes:

a. Based on $T_C = 25 \text{ °C}$. b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under steady state conditions is 85 °C/W.



ME4925

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	•					•	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_D = -250 \mu A$	- 40			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = - 250 μA		- 36		m\//0C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	i _D = - 250 μA		5		mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \ \mu A$	- 1.2		- 2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zana Oata Maltana Duain Ourmant	1	V _{DS} = - 40 V, V _{GS} = 0 V			- 1	μA	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			- 5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le$ - 5 V, V_{GS} = - 10 V	- 25			Α	
Drain Courses On Otata Desistenced	Р	V _{GS} = - 10 V, I _D = - 10.2 A		0.010		Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 8.4 A		0.014			
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 10.2 A		37		S	
Dynamic ^b	•	· · · · · · · · · · · · · · · · · · ·					
Input Capacitance	C _{iss}			3007		pF	
Output Capacitance	C _{oss}	V _{DS} = - 20 V, V _{GS} = 0 V, f = 1 MHz		335			
Reverse Transfer Capacitance	C _{rss}			291			
Total Gate Charge		V_{DS} = - 20 V, V_{GS} = - 10 V, I_{D} = - 10.2 A		64	95	-	
	Q _g			33	50		
Gate-Source Charge	Q _{gs}	V_{DS} = - 20 V, V_{GS} = - 4.5 V, I_{D} = - 10.2 A		9.8			
Gate-Drain Charge	Q _{gd}			15.7			
Gate Resistance	Rg	f = 1 MHz	0.4	2	4	Ω	
Turn-On Delay Time	t _{d(on)}			57	86	-	
Rise Time	t _r	V_{DD} = - 20 V, R_L = 2.4 Ω		50	75		
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong$ - 8.2 A, V_GEN = - 4.5 V, R_g = 1 Ω		40	60		
Fall Time	t _f			17	26		
Turn-On Delay Time	t _{d(on)}			13	20	ns	
Rise Time	t _r	V_{DD} = - 20 V, R_L = 2.4 Ω		11	20		
Turn-Off Delay Time	t _{d(off)}	$I_{D}\cong$ - 8.2 A, V_{GEN} = - 10 V, R_{g} = 1 Ω		45	68		
Fall Time	t _f			9	18		
Drain-Source Body Diode Characteristi	cs	· · · · · · · · · · · · · · · · · · ·					
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			- 5.3	A	
Pulse Diode Forward Current	I _{SM}				- 50		
Body Diode Voltage	V _{SD}	I _S = - 8.2 A, V _{GS} = 0 V		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 8.2 A, dl/dt = 100 A/μs, T _J = 25 °C		36	54	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			41	62	nC	
Reverse Recovery Fall Time	t _a			20			
Reverse Recovery Rise Time	t _b			16		ns	

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

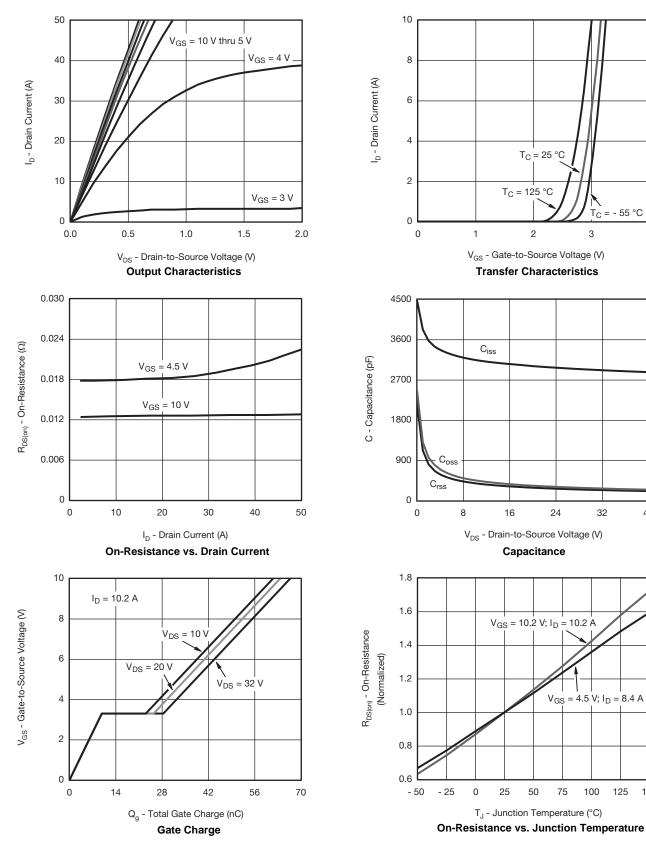




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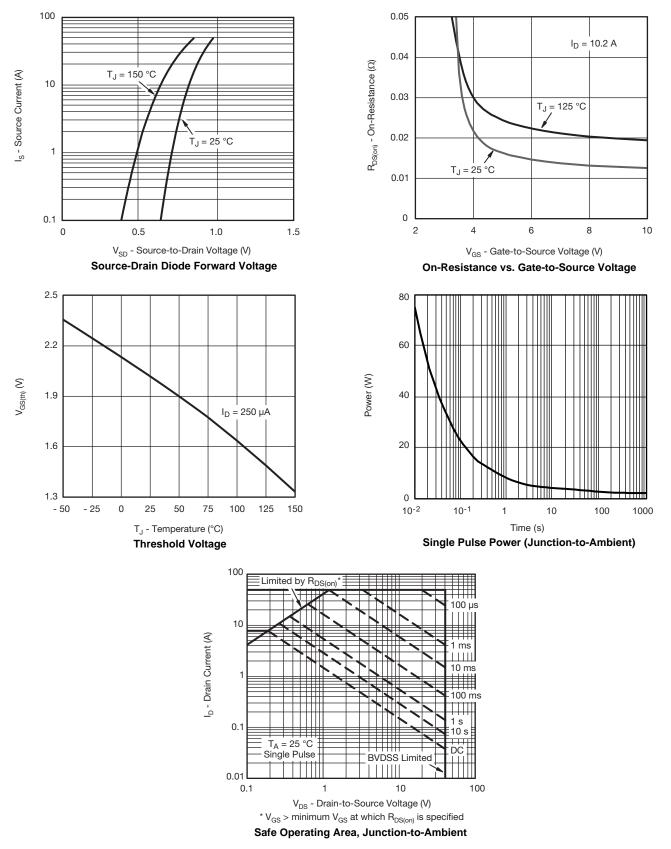
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



150

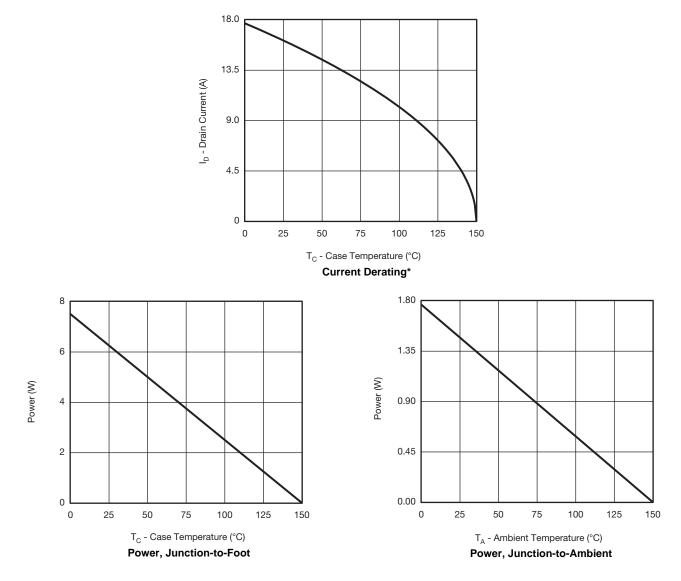








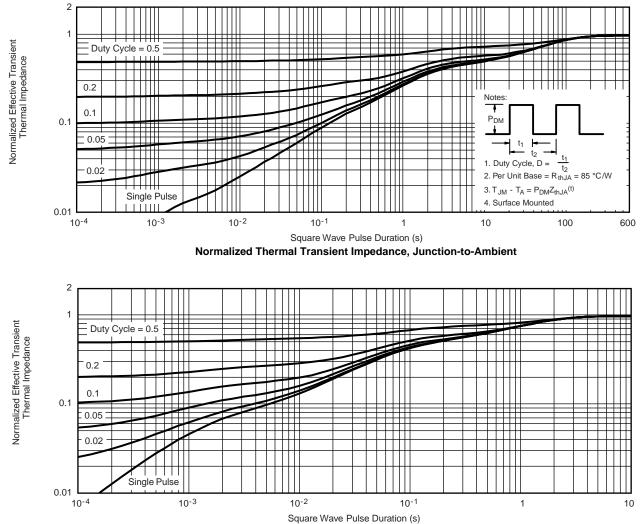
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

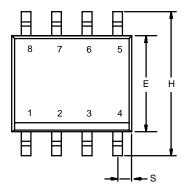


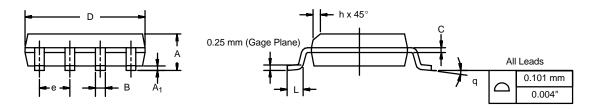
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

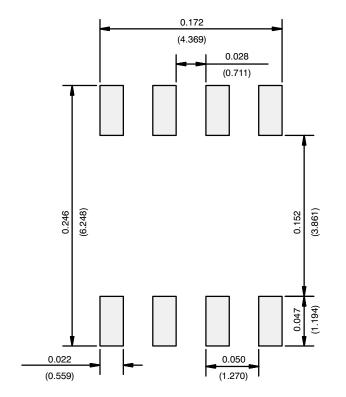




	MILLIM	IETERS	INC	HES	
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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