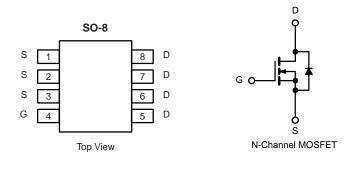


N-Channel 150 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)			
150	0.080 at V _{GS} = 10 V	5.4	23 nC			
150	0.085 at V _{GS} = 8 V	4.5	23110			



FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- Extremely Low Q_{gd} for Switching Losses
- 100 % Rg Tested
- 100 % Avalanche Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

• Primary Side Switch



HALOGEN

FREE

Available

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	150	V	
Gate-Source Voltage		V _{GS}	± 20	v	
	T _C = 25 °C		5.4		
Continuous Drain Current ($T_1 = 150 \ ^{\circ}C$)	T _C = 70 °C		5.1		
Continuous Drain Current $(T_J = 150 \text{ C})$	T _A = 25 °C	I _D	5.0 ^{b, c}		
	T _A = 70 °C		4.5 ^{b, c}	A	
Pulsed Drain Current		I _{DM}	22	~ ^	
Continuous Source-Drain Diode Current	T _C = 25 °C		4.5		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2.6 ^{b, c}		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	20		
Single Pulse Avalanche Energy		E _{AS}	20	mJ	
	T _C = 25 °C		5.9		
Maximum Power Discinction	T _C = 70 °C	P _D	3.8	W	
Maximum Power Dissipation	T _A = 25 °C		3.1 ^{b, c}		
	T _A = 70 °C	1	2 ^{b, c}		
Operating Junction and Storage Temperature	T _J , T _{stq}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, †}	t ≤ 10 s	R _{thJA}	33	40	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	17	21	C/VV		
	Cloudy Cluic	· sinjr		21	l		

Notes:

a. Based on T_C = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under steady state conditions is 80 °C/W.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	-1			•	<u> </u>	•
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	150			V
V _{DS} Temperature Coefficient				172		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 10		- mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.2		2.5	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
Zana Osta Malta na Dusia Osuma at	I _{DSS} -	$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	
Zero Gate Voltage Drain Current		$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 \text{ °C}$			10	μA
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	30			Α
Drain Course On State Desistance	· · ·	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 5 \text{ A}$		0.080		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 8 V, I_{D} = 5 A$		0.085		Ω
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 5 \text{ A}$		23		S
Dynamic ^b					•	
Input Capacitance	C _{iss}			1735		pF
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$		160		
Reverse Transfer Capacitance	C _{rss}			37		
Total Gate Charge	Q _g	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 5 \text{ A}$		28.5	43	
				23	35	nC
Gate-Source Charge	Q _{gs}	$V_{DS} = 75 \text{ V}, V_{GS} = 8 \text{ V}, I_{D} = 5 \text{ A}$		8		
Gate-Drain Charge	Q _{gd}			6.5		
Gate Resistance	R _g	f = 1 MHz		0.85	1.3	Ω
Turn-on Delay Time	t _{d(on)}			14	21	-
Rise Time	t _r	V_{DD} = 50 V, R_{L} = 10 Ω		12	18	
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D} \cong$ 5 A, V_GEN = 10 V, R_g = 1 Ω		22	33	
Fall Time	t _f			6	10	
Turn-On Delay Time	t _{d(on)}			16	24	- ns - -
Rise Time	t _r	V_{DD} = 50 V, R_{L} = 10 Ω		12	18	
Turn-Off Delay Time	t _{d(off)}	${\sf I}_{\sf D}\cong$ 5 A, ${\sf V}_{\sf GEN}$ = 8 V, ${\sf R}_{\sf g}$ = 1 Ω		20	30	
Fall Time	t _f			7	12	
Drain-Source Body Diode Characteristic	cs					
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			7.7	۸
Pulse Diode Forward Current ^a	I _{SM}				50	A
Body Diode Voltage	V_{SD}	I _S = 2.6 A		0.77	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			63	95	ns
Body Diode Reverse Recovery Charge	Q _{rr}	L = 5 A dl/dt = 100 A/tro T = 25 °C		110	165	nC
Reverse Recovery Fall Time	t _a	$I_F = 5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 \text{ °C}$		49		
Reverse Recovery Rise Time	t _b	\neg		14		ns

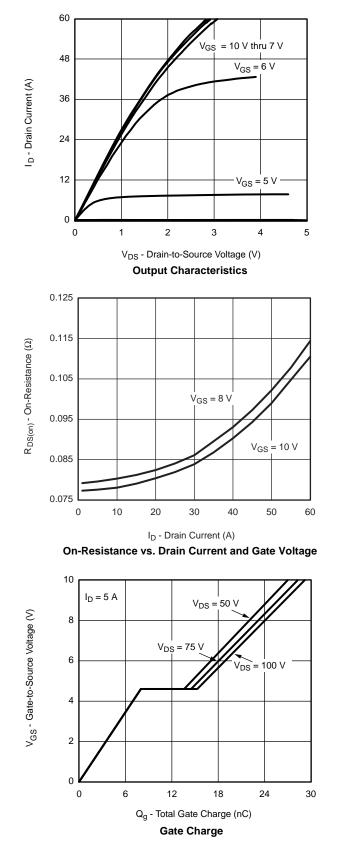
Notes:

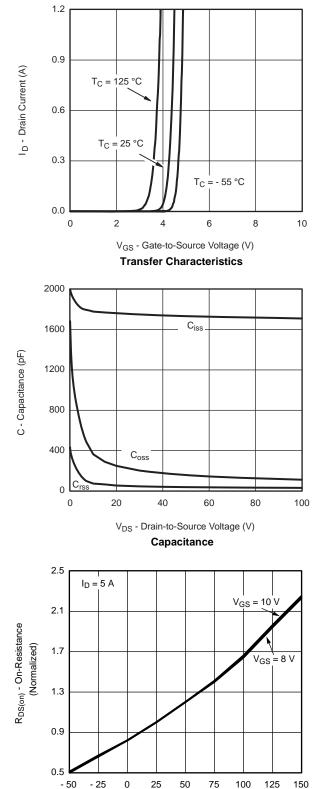
a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$

a. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



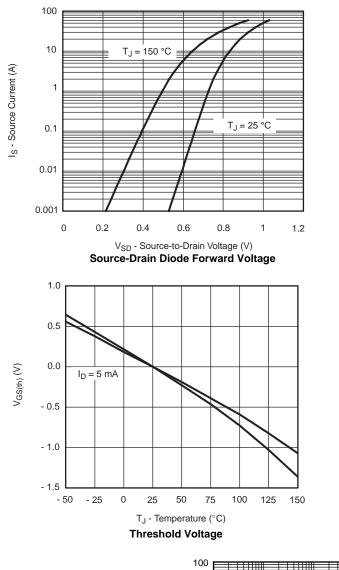


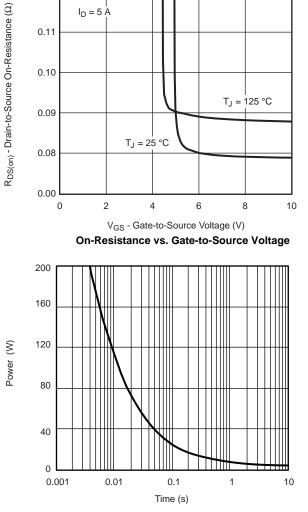


T_J - Junction Temperature (°C)

On-Resistance vs. Junction Temperature

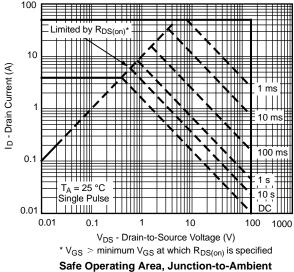




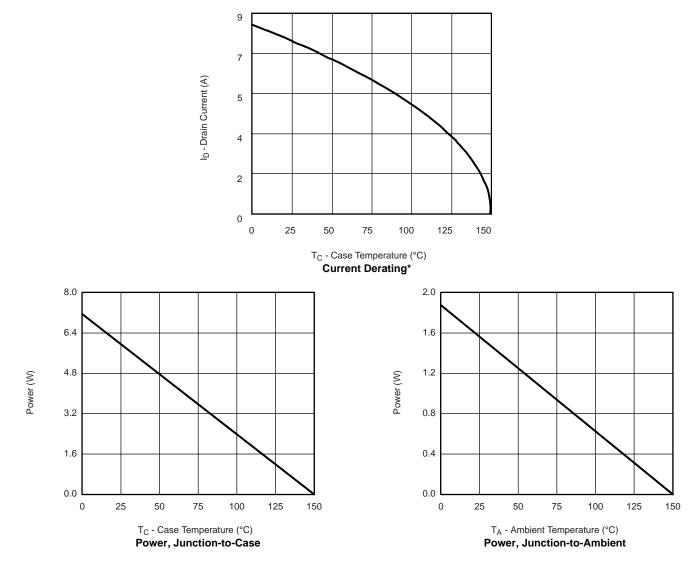


0.12

Single Pulse Power, Junction-to-Ambient

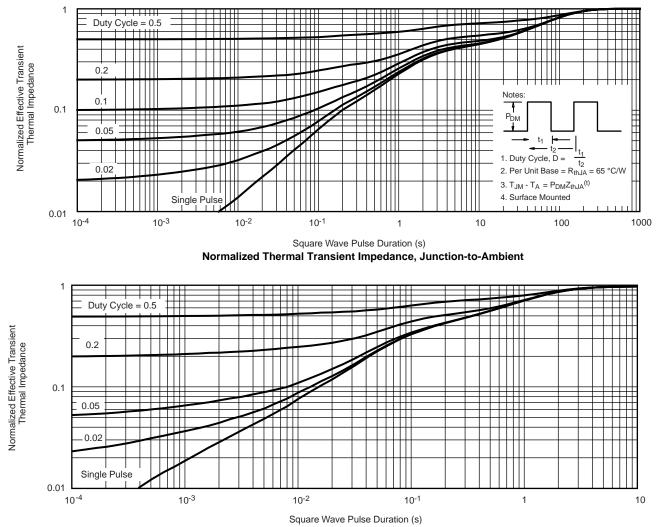






* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

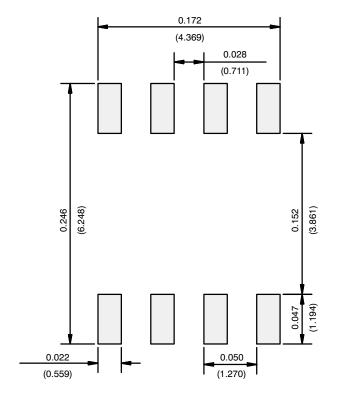




	MILLIM	IETERS	INC	HES		
DIM	Min	Мах	Min	Max		
A	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498						



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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