

## N-Channel 150V (D-S) MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
150	0.035 at V <sub>GS</sub> = 10 V	45
	0.042 at V <sub>GS</sub> = 7.5 V	42

### FEATURES

- TrenchFET<sup>®</sup> Power MOSFETs
- 175 °C Junction Temperature
- New Low Thermal Resistance Package
- PWM Optimized
- Compliant to RoHS Directive 2002/95/EC

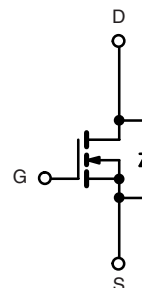
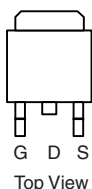


RoHS  
COMPLIANT

### APPLICATIONS

- Primary Side Switch

TO-263



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>C</sub> = 25 °C, unless otherwise noted					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	150	V		
Gate-Source Voltage	V <sub>GS</sub>	± 20			
Continuous Drain Current (T <sub>J</sub> = 175 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	45	A	
		T <sub>C</sub> = 125 °C	31		
Pulsed Drain Current	I <sub>DM</sub>	140			
Avalanche Current	I <sub>AR</sub>	50			
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>	80	mJ		
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	160 <sup>b</sup>	W	
		T <sub>A</sub> = 25 °C <sup>c</sup>	3.7		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount TO-263 <sup>°</sup> )	R <sub>thJA</sub>	40	°C/W	
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.9		

Notes:

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When Mounted on 1" square PCB (FR-4 material).

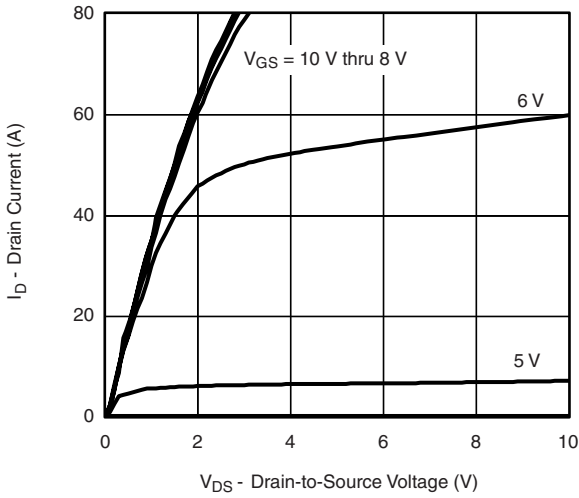
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	150			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	4		6	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	80			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		0.035		$\Omega$
		$V_{GS} = 7.5\text{ V}, I_D = 10\text{ A}$		0.042		
		$V_{GS} = 10\text{ V}, I_D = 15\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.060		
		$V_{GS} = 10\text{ V}, I_D = 15\text{ A}, T_J = 175\text{ }^\circ\text{C}$		0.080		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$	10			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		2200		$\mu\text{F}$
Output Capacitance	$C_{oss}$			290		
Reverse Transfer Capacitance	$C_{rss}$			190		
Gate Resistance	$R_g$			2		$\Omega$
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		38	60	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			13		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			13		
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 75\text{ V}, R_L = 1.80\text{ }\Omega$ $I_D \equiv 40\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\text{ }\Omega$		15	25	ns
Rise Time <sup>c</sup>	$t_r$			130	200	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			30	45	
Fall Time <sup>c</sup>	$t_f$			90	140	
<b>Source-Drain Diode Ratings and Characteristics <math>T_C = 25\text{ }^\circ\text{C}</math><sup>b</sup></b>						
Continuous Current	$I_S$				40	A
Pulsed Current	$I_{SM}$				80	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 40\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 40\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		100	150	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			5	8	A
Reverse Recovery Charge	$Q_{rr}$			0.25	0.6	$\mu\text{C}$

Notes:

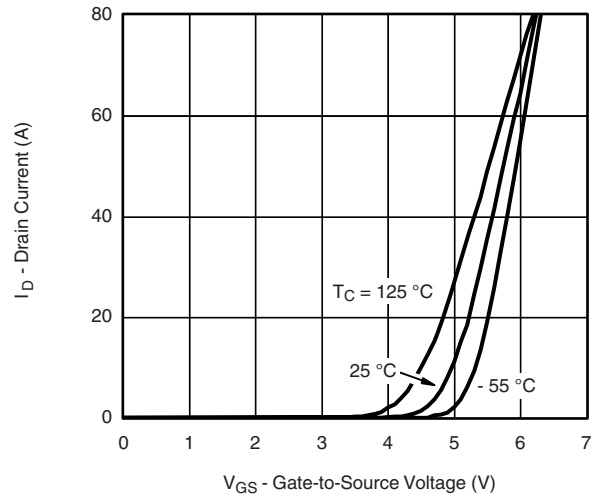
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

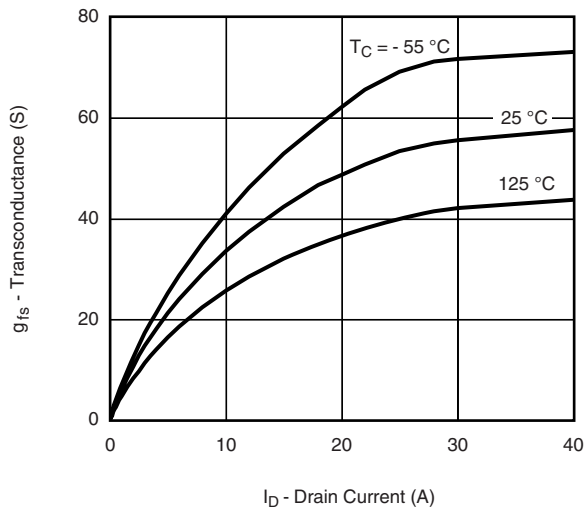
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Output Characteristics**



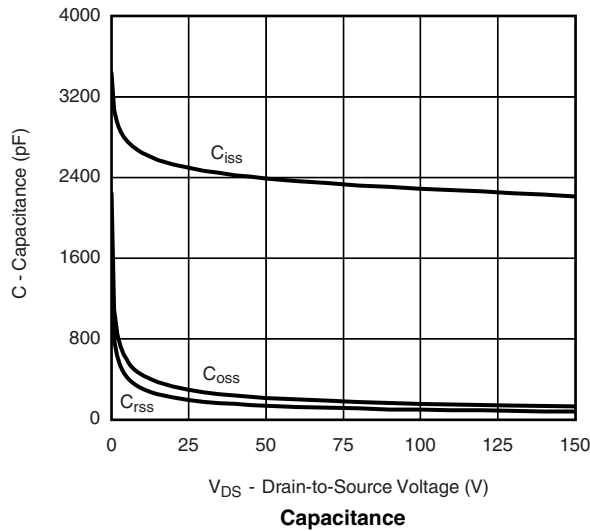
**Transfer Characteristics**



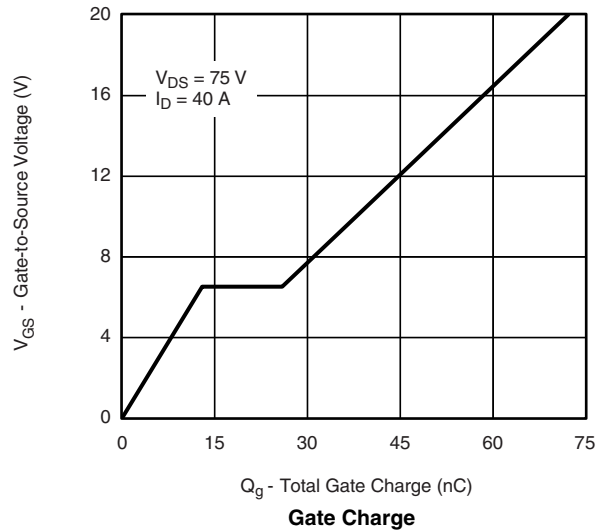
**Transconductance**



**On-Resistance vs. Drain Current**

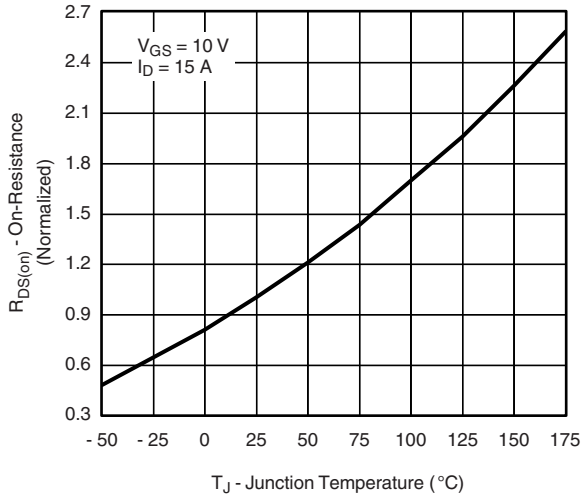


**Capacitance**

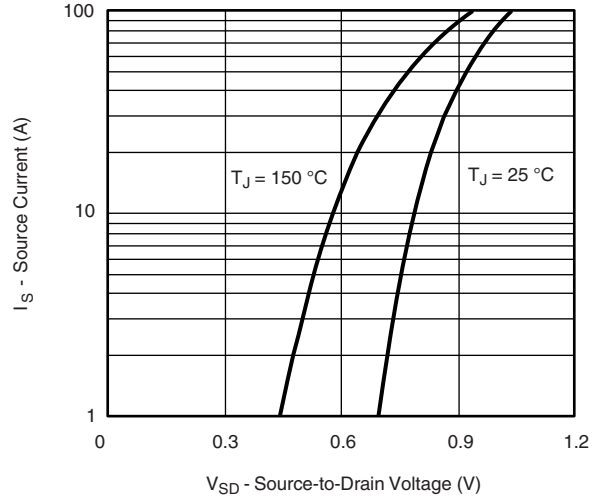


**Gate Charge**

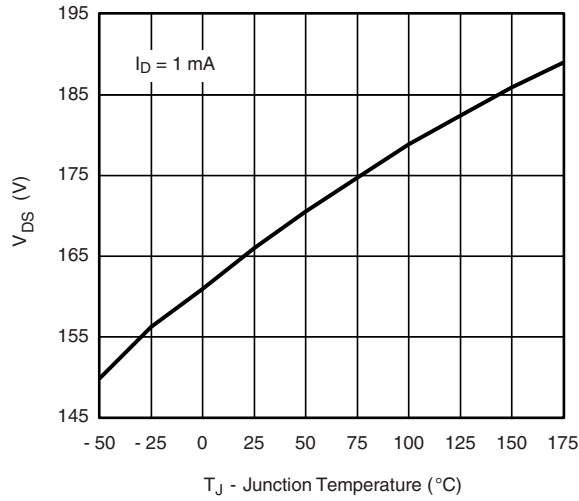
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**On-Resistance vs. Junction Temperature**

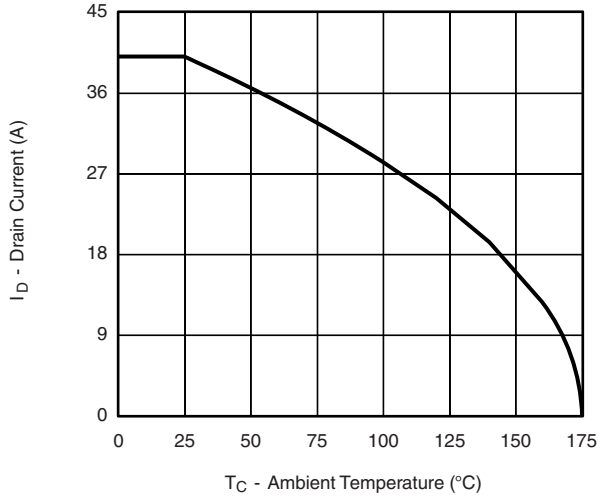


**Source-Drain Diode Forward Voltage**

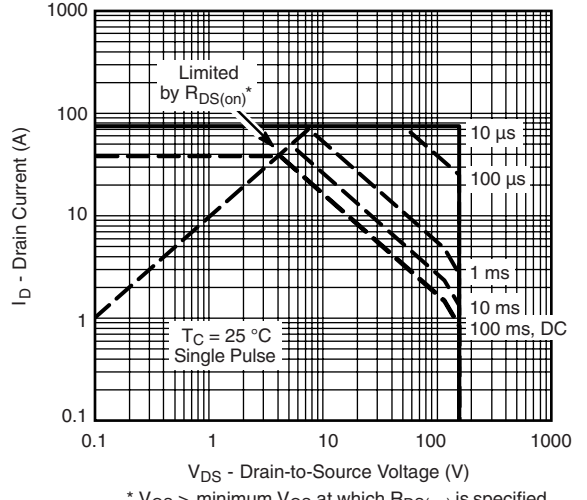


**Drain Source Breakdown vs. Junction Temperature**

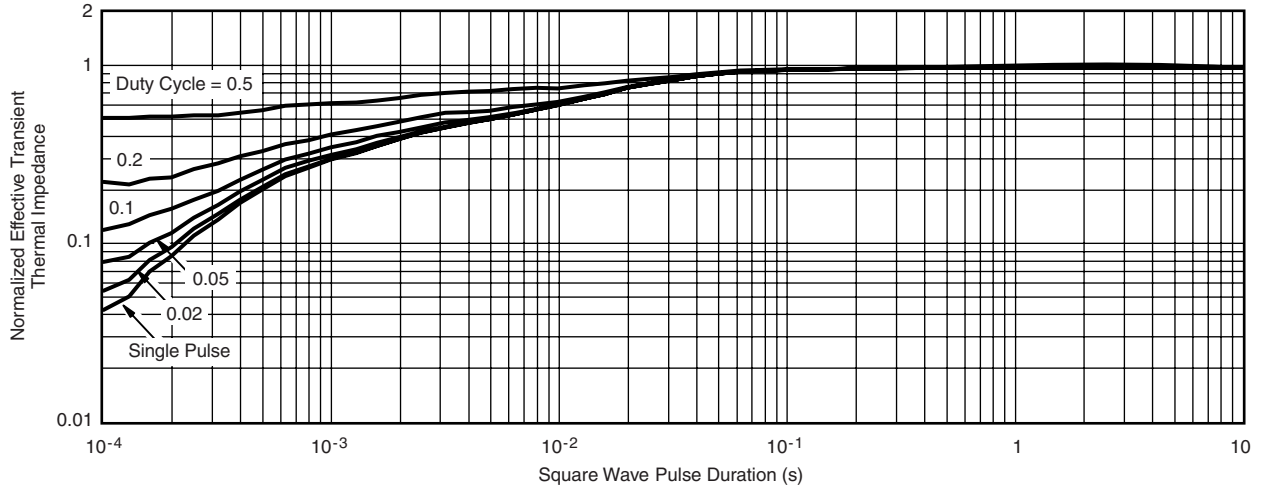
**THERMAL RATINGS**



**Maximum Avalanche and Drain Current vs. Case Temperature**

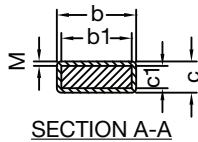
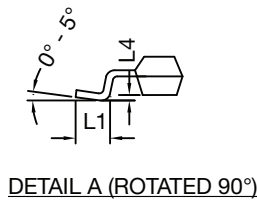
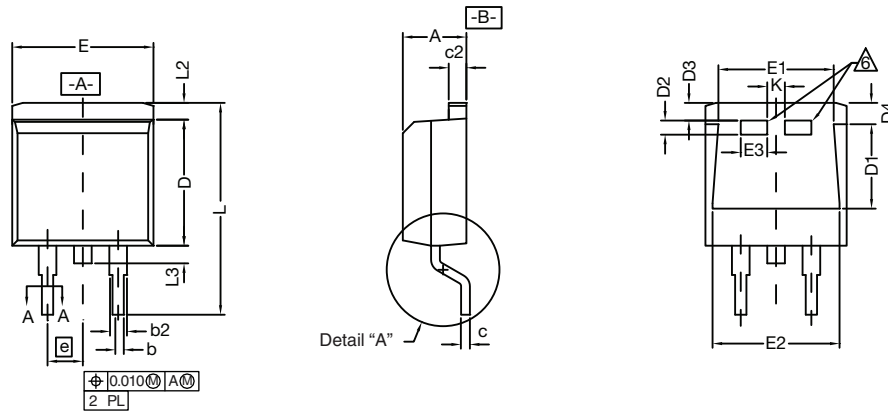


**Safe Operating Area**  
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**Normalized Thermal Transient Impedance, Junction-to-Case**

### TO-263 (D<sup>2</sup>PAK): 3-LEAD

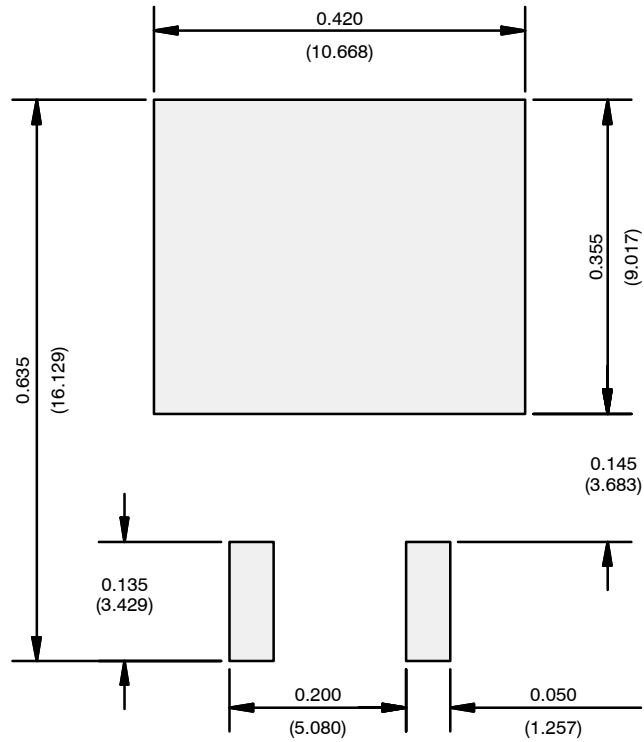


DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
<b>E3</b>	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

**Notes**

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- E3**: This feature is for thick lead.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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