

## P-Channel 60-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>d</sup>
- 60	0.0065 at $V_{GS} = - 10$ V	- 110
	0.0085 at $V_{GS} = - 4.5$ V	

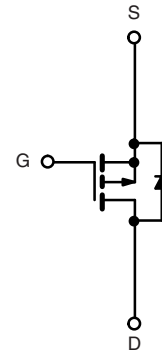
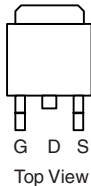
### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- Package with Low Thermal Resistance
- 100 %  $R_g$  Tested



Available  
**RoHS\***  
COMPLIANT

TO-263



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	- 60	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current <sup>d</sup> ( $T_J = 175$ °C)	$I_D$	$T_C = 25$ °C	- 110	A
		$T_C = 125$ °C	- 75	
Pulsed Drain Current	$I_{DM}$	- 200		
Avalanche Current	$I_{AS}$	- 85		
Single Pulse Avalanche Energy <sup>d</sup>	$E_{AS}$	L = 0.1 mH	211	mJ
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	272 <sup>c</sup>	W
		$T_A = 25$ °C <sup>b</sup>	3.75 <sup>b</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient	$R_{thJA}$	40	°C/W	PCB Mount <sup>d</sup>
Junction-to-Case	$R_{thJC}$	0.55		

Notes:

- Duty cycle  $\leq 1$  %.
- When Mounted on 1" square PCB (FR-4 material).
- See SOA curve for voltage derating.
- Limited by Package.

\* Pb containing terminations are not RoHS compliant, exemptions may apply.

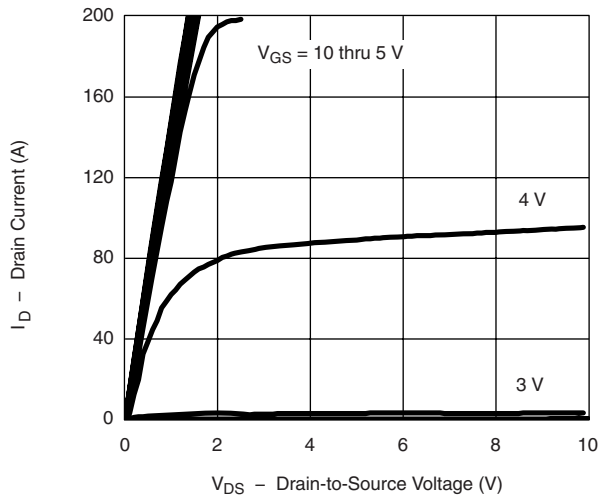
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 60			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1		- 3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$			- 1	$\mu\text{A}$
		$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			- 50	
		$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			- 250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	- 120			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -30\text{ A}$		0.0065		$\Omega$
		$V_{GS} = -10\text{ V}, I_D = -30\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.0129		
		$V_{GS} = -10\text{ V}, I_D = -30\text{ A}, T_J = 175\text{ }^\circ\text{C}$		0.016		
		$V_{GS} = -4.5\text{ V}, I_D = -20\text{ A}$		0.0085		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -50\text{ A}$	20			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1\text{ MHz}$		9200		$\text{pF}$
Output Capacitance	$C_{oss}$			975		
Reverse Transfer Capacitance	$C_{rss}$			760		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = -30\text{ V}, V_{GS} = -10\text{ V}, I_D = -110\text{ A}$		160	240	$\text{nC}$
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			40		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			36		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	1.5	3	4.5	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -30\text{ V}, R_L = 0.27\text{ }\Omega$ $I_D \cong -110\text{ A}, V_{GEN} = -10\text{ V}, R_G = 2.5\text{ }\Omega$		20	30	ns
Rise Time <sup>c</sup>	$t_r$			190	285	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			140	210	
Fall Time <sup>c</sup>	$t_f$			300	450	
<b>Source-Drain Diode Ratings and Characteristics</b> $T_C = 25\text{ }^\circ\text{C}^b$						
Continuous Current	$I_S$				- 110	A
Pulsed Current	$I_{SM}$				- 200	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = -50\text{ A}, V_{GS} = 0\text{ V}$		- 1.0	- 1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = -50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		60	90	ns
Peak Reverse Recovery Charge	$I_{RM(REC)}$			- 3	- 4.5	A
Reverse Recovery Charge	$Q_{rr}$			0.09	0.2	$\mu\text{C}$

## Notes:

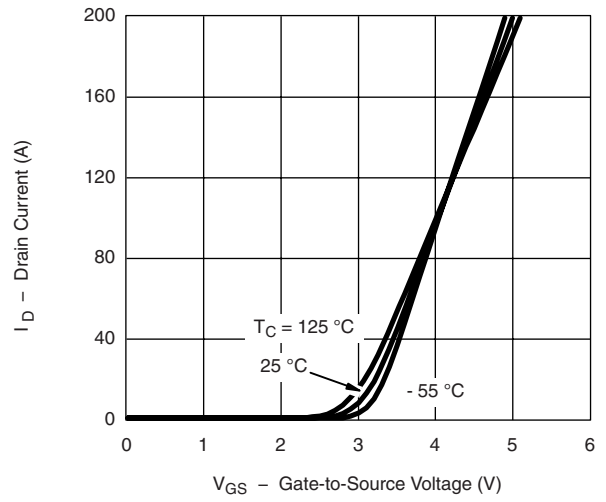
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

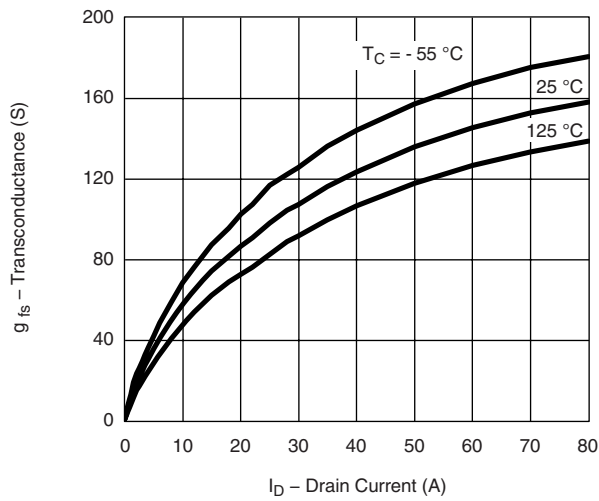
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



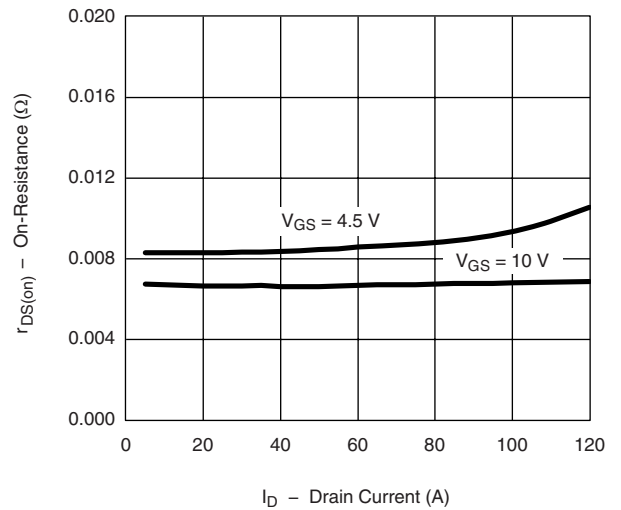
**Output Characteristics**



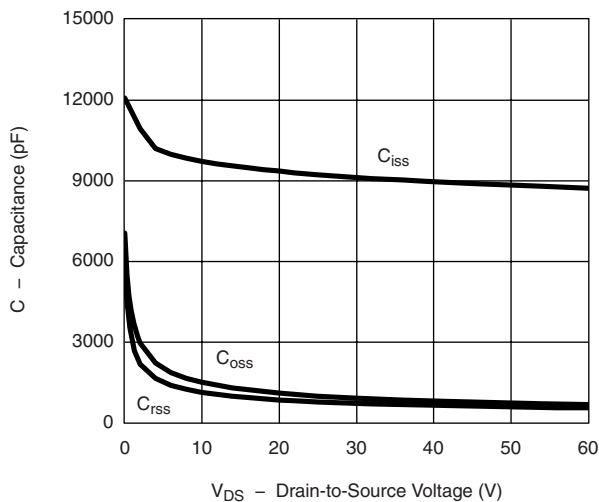
**Transfer Characteristics**



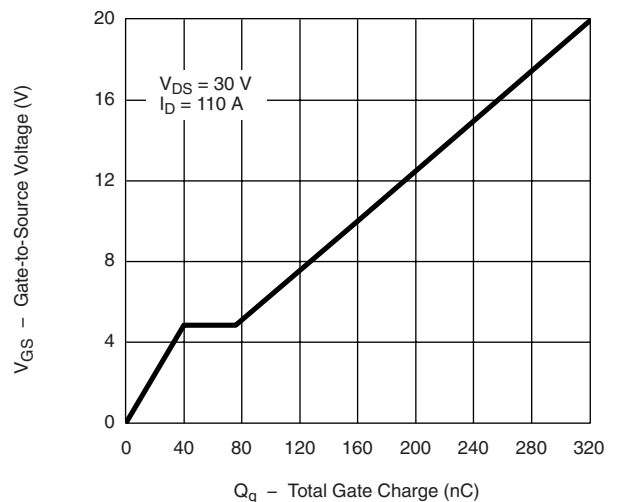
**Transconductance**



**On-Resistance vs. Drain Current**

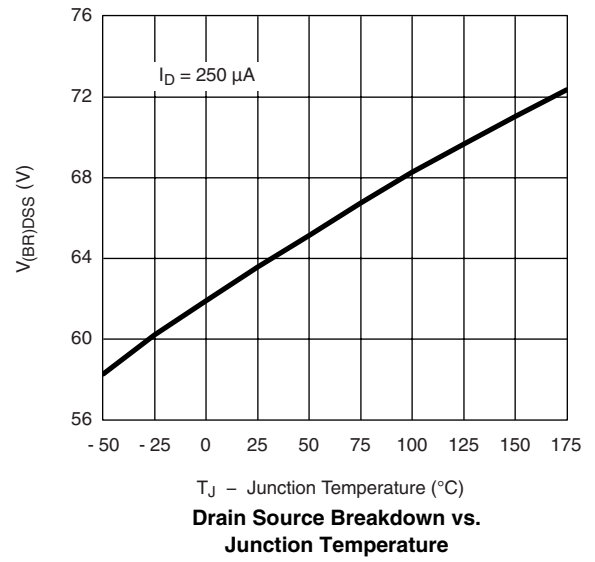
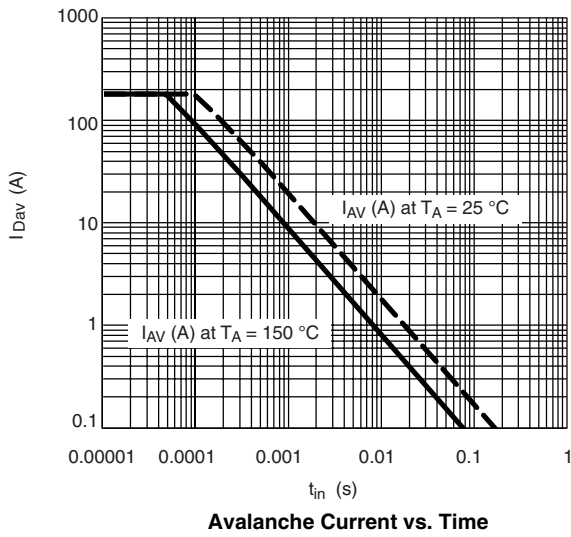
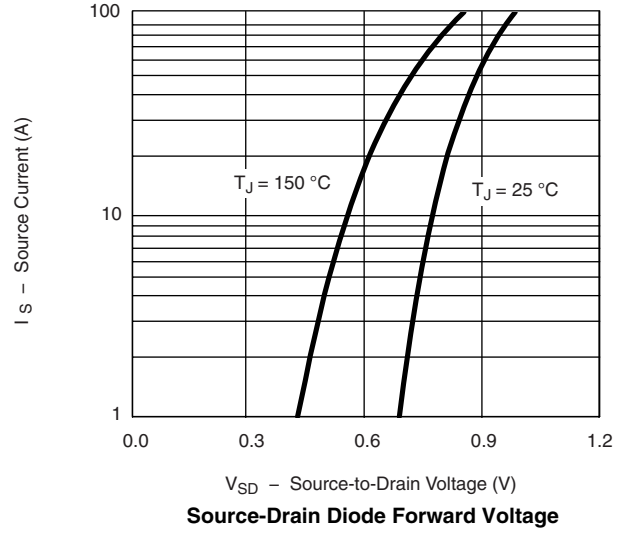
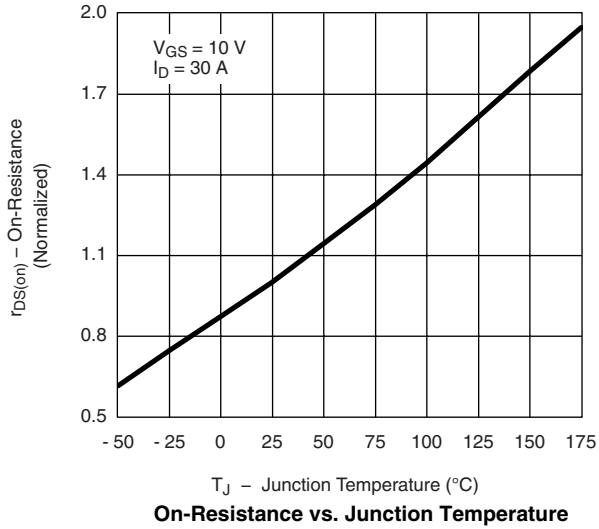


**Capacitance**

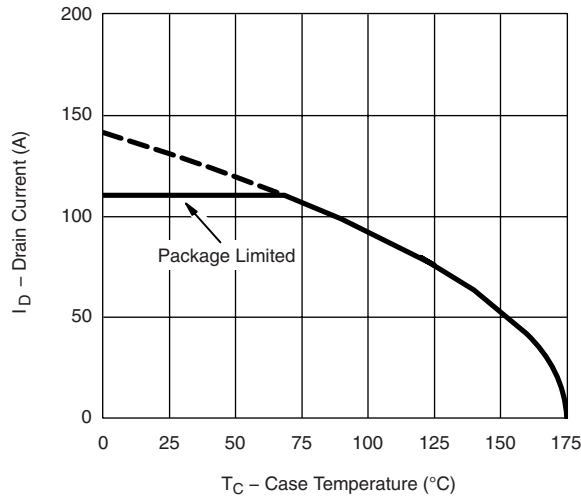


**Gate Charge**

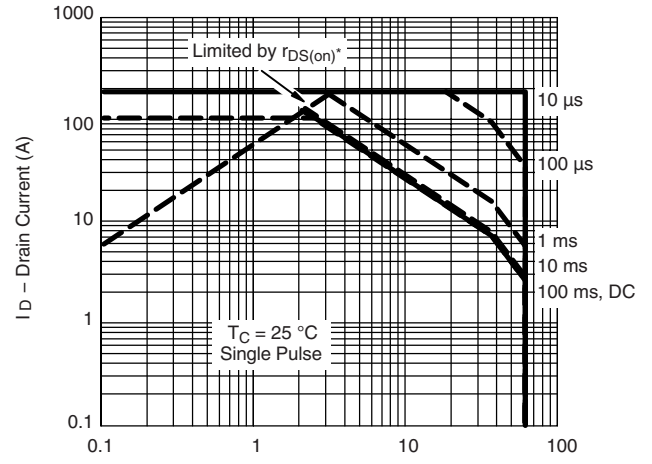
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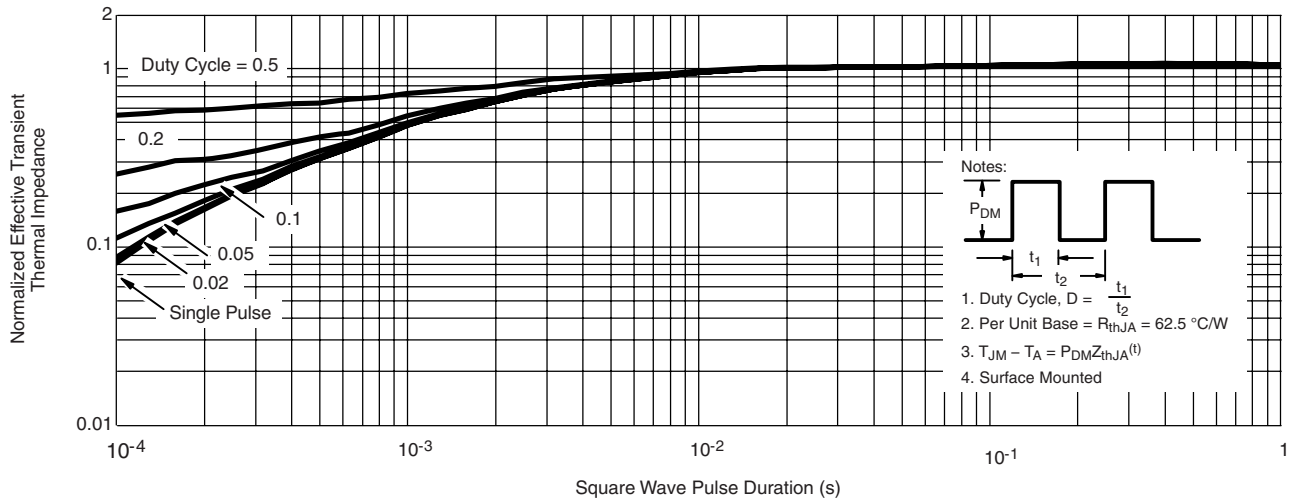
**THERMAL RATINGS**



**Maximum Avalanche and Drain Current vs. Case Temperature**

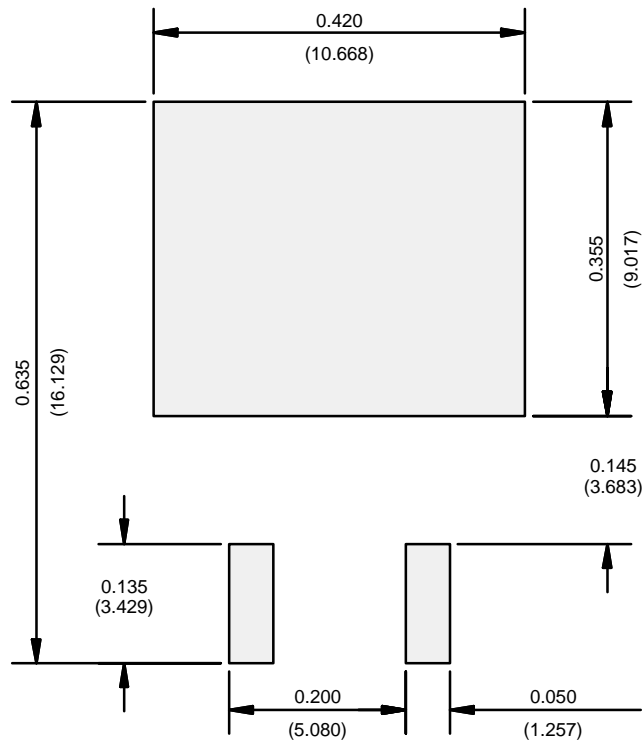


**Safe Operating Area**  
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified



**Normalized Thermal Transient Impedance, Junction-to-Case**

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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