

## N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a, e</sup>	$Q_g$ (Typ.)
30	0.023 at $V_{GS} = 10$ V	4.5	4.2 nC
	0.027 at $V_{GS} = 4.5$ V	4.0	

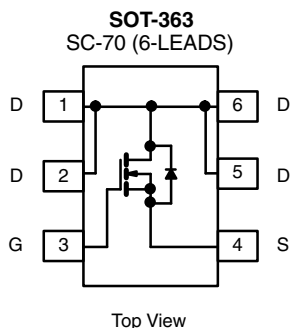
### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- Low On-Resistance
- 100 %  $R_g$  Tested
- Compliant to RoHS Directive 2002/95/EC


**RoHS**  
 COMPLIANT

### APPLICATIONS

- DC/DC Converters, High Speed Switching



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	30	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	4.5 <sup>e</sup>	A
		$T_C = 70$ °C	4.0 <sup>e</sup>	
		$T_A = 25$ °C	4.1 <sup>b, c</sup>	
		$T_A = 70$ °C	3.6 <sup>b, c</sup>	
Pulsed Drain Current ( $t = 300$ $\mu$ s)	$I_{DM}$	25		
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C	2.1	
		$T_A = 25$ °C	1.1 <sup>b, c</sup>	
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	2.5	W
		$T_C = 70$ °C	1.6	
		$T_A = 25$ °C	1.3 <sup>b, c</sup>	
		$T_A = 70$ °C	0.8 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature)		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, d</sup>	$R_{thJA}$	75	100	°C/W	
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	40	50		

Notes:

- Based on  $T_C = 25$  °C.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$  s.
- Maximum under steady state conditions is 166 °C/W.
- Package limited.

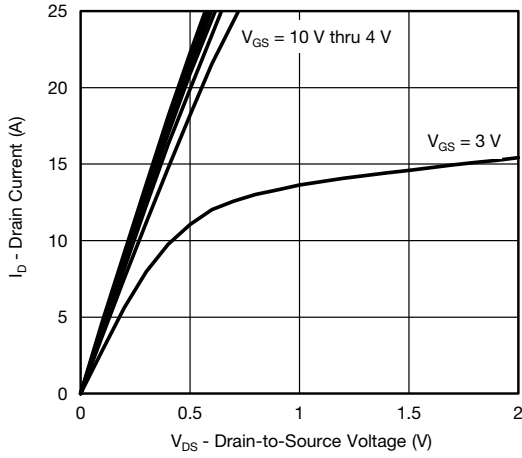
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		30		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 4.8		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.5		2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ 5 V, V <sub>GS</sub> = 10 V	20			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A		0.023		Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3 A		0.027		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.5 A		24		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		424		pF
Output Capacitance	C <sub>oss</sub>			100		
Reverse Transfer Capacitance	C <sub>rss</sub>			42		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A		8.2	13	nC
		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.5 A		4.2	7	
Gate-Source Charge	Q <sub>gs</sub>		1.4			
Gate-Drain Charge	Q <sub>gd</sub>		1.4			
Gate Resistance	R <sub>g</sub>	f = 1 MHz	2.5	12.6	25.2	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 3.4 Ω I <sub>D</sub> = 4.4 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		6	12	ns
Rise Time	t <sub>r</sub>			20	30	
Turn-Off Delay Time	t <sub>d(off)</sub>			14	21	
Fall Time	t <sub>f</sub>			10	20	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 3.4 Ω I <sub>D</sub> = 4.4 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		3	6	
Rise Time	t <sub>r</sub>			11	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			20	30	
Fall Time	t <sub>f</sub>			7	14	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			2.1	A
Pulse Diode Forward Current	I <sub>SM</sub>				25	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 4.4 A, V <sub>GS</sub> = 0 V		0.82	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 4.4 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		13	20	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			6	12	nC
Reverse Recovery Fall Time	t <sub>a</sub>			8		ns
Reverse Recovery Rise Time	t <sub>b</sub>			5		

Notes:

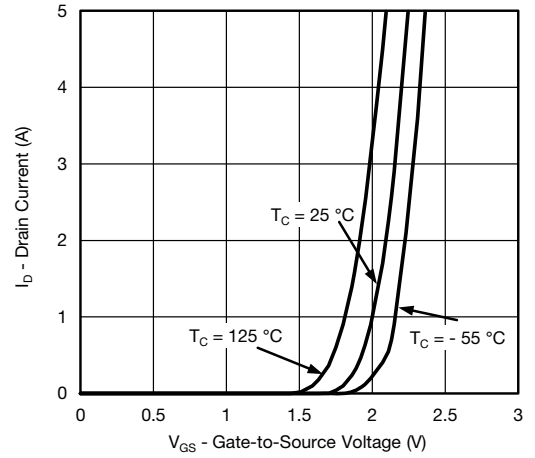
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

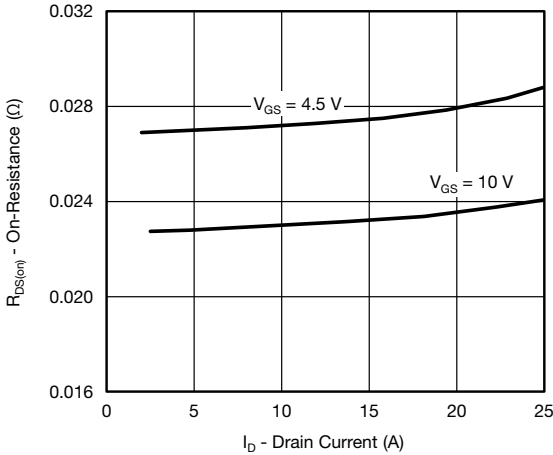
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



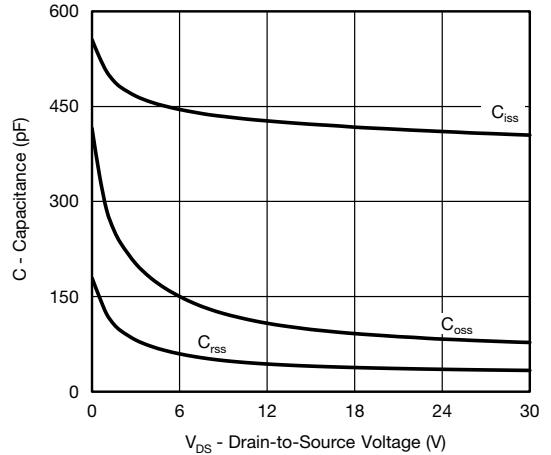
**Output Characteristics**



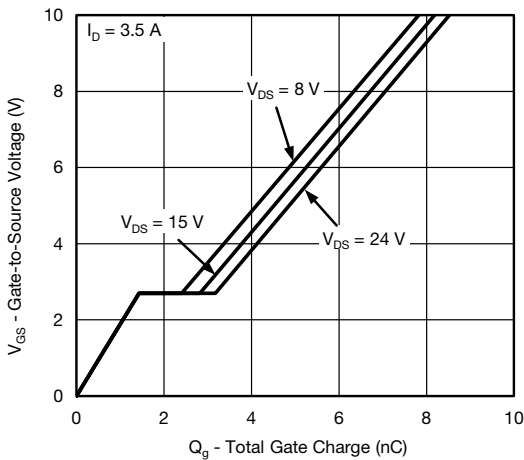
**Transfer Characteristics**



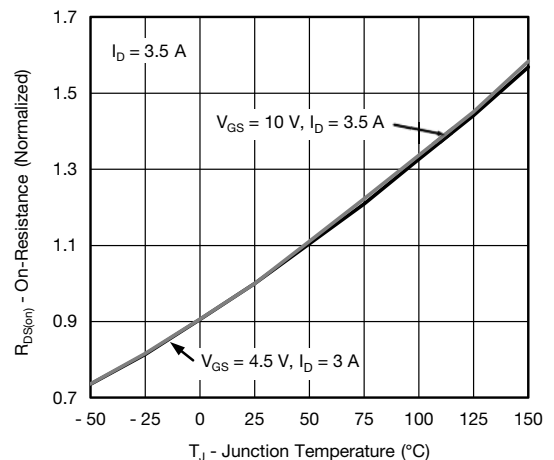
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

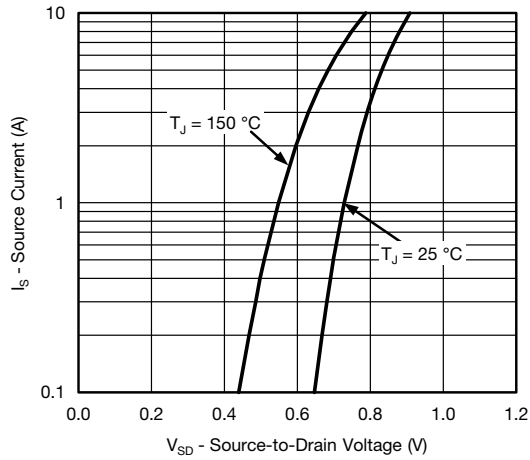


**Gate Charge**

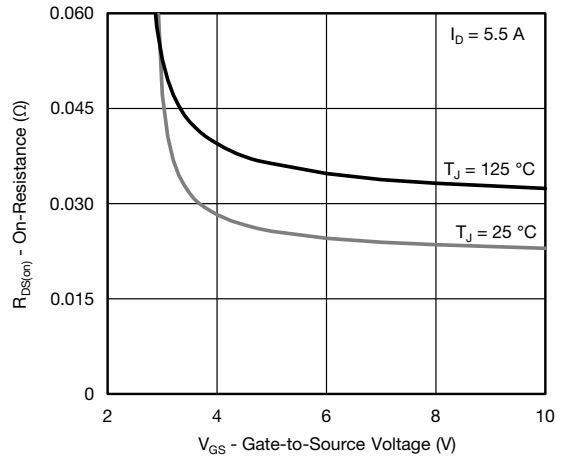


**On-Resistance vs. Junction Temperature**

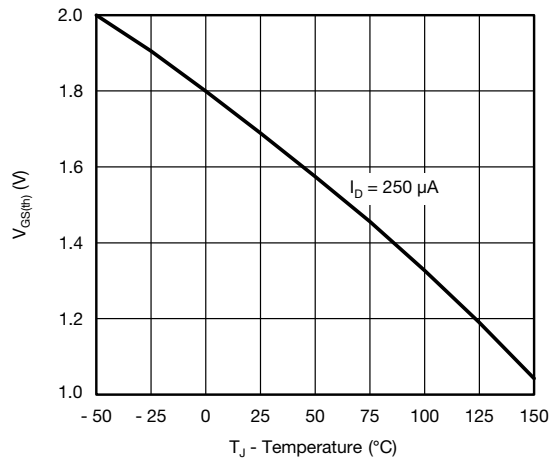
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



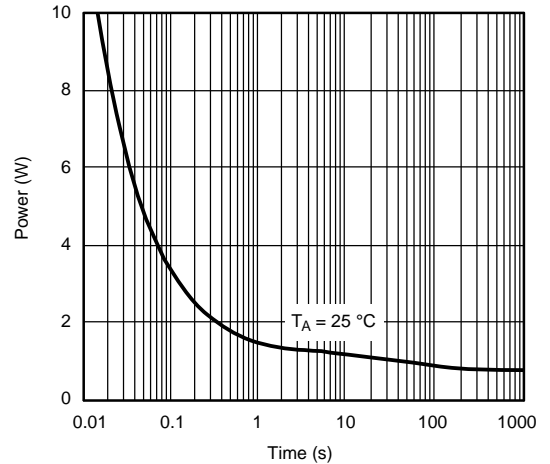
**Source-Drain Diode Forward Voltage**



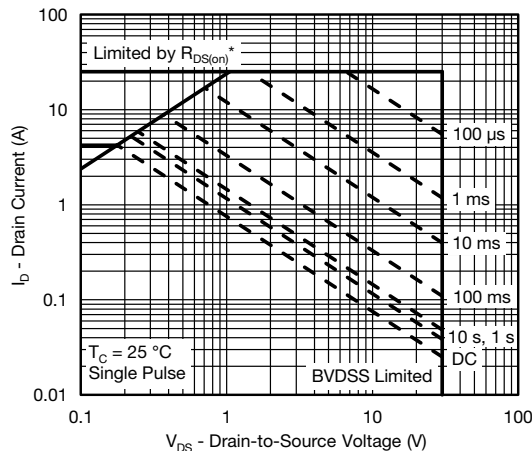
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



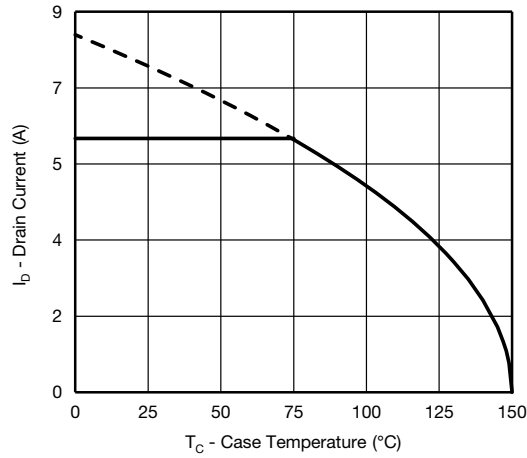
**Single Pulse Power (Junction-to-Ambient)**



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

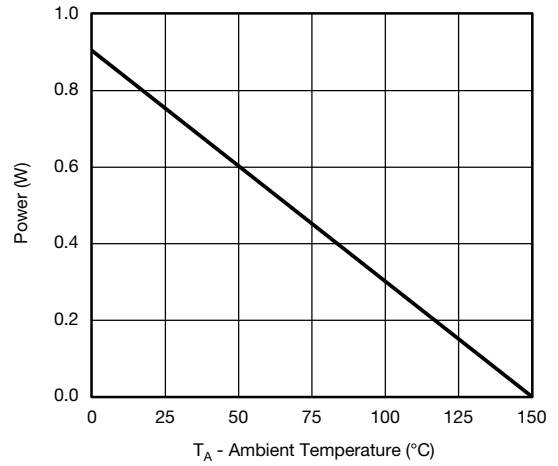
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating\***



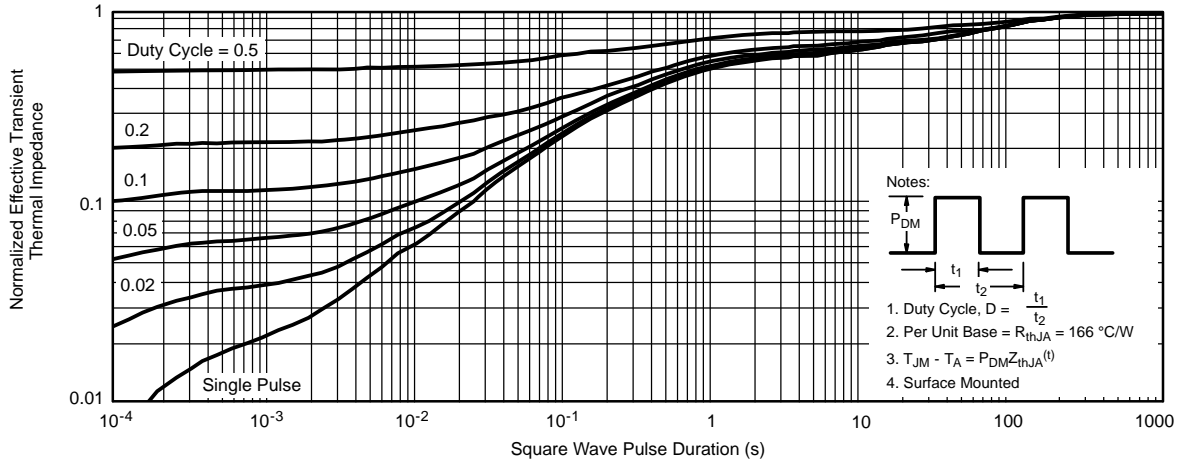
**Power Derating, Junction-to-Foot**



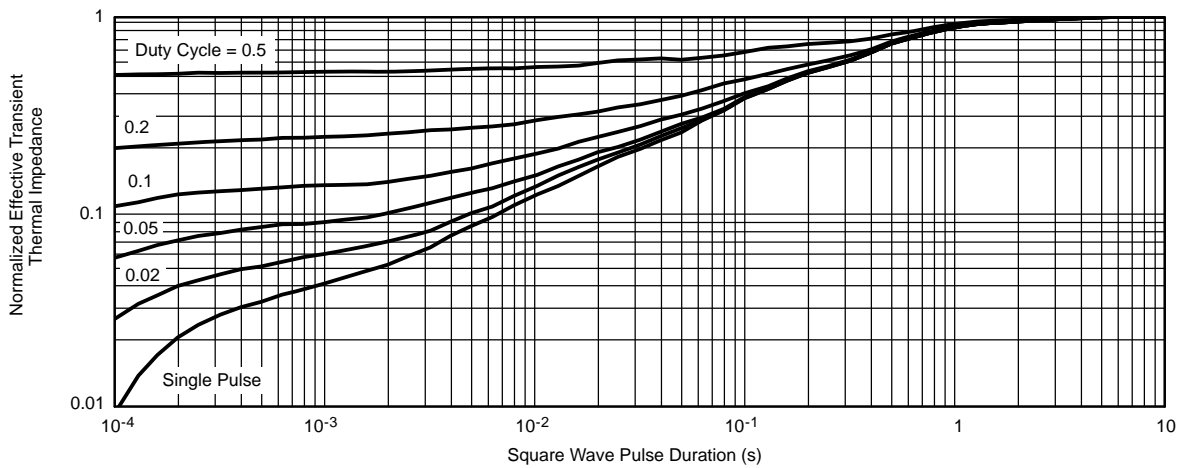
**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

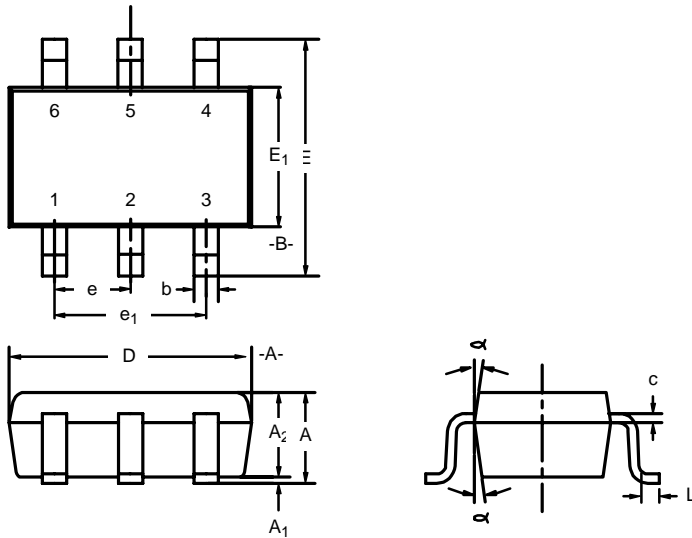


**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

**SC-70: 6-LEADS**



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	-	1.10	0.035	-	0.043
A <sub>1</sub>	-	-	0.10	-	-	0.004
A <sub>2</sub>	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	-	0.012
c	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E <sub>1</sub>	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e <sub>1</sub>	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		
ECN: S-03946—Rev. B, 09-Jul-01 DWG: 5550						

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