

SI7972DP-T1-GE3-VB Datasheet

Dual N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	60			
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.032			
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.038			
Q _g typ. (nC)	7.1			
I _D (A)	17			
Configuration	Dual			

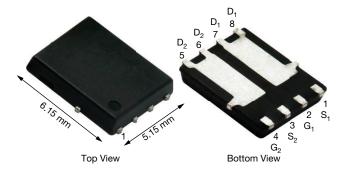
FEATURES

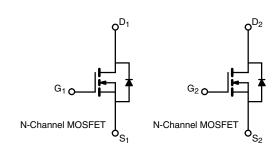
- TrenchFET® power MOSFET
- PWM optimized
- + 100 % $\rm R_g$ and UIS tested

APPLICATIONS

• System power DC/DC







PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	60	v
Gate-source voltage		V _{GS}	± 20	v
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		17	
	T _C = 70 °C		8 ^a	-
	T _A = 25 °C	I _D	8 ^a	
	T _A = 70 °C		8 a	А
Pulsed drain current		I _{DM}	40	7
Source-drain current diode current	T _C = 25 °C		19	
	T _A = 25 °C	I _S	3 ^{b, c}	
Maximum power dissipation	T _C = 25 °C		22	
	T _C = 70 °C		14	- W
	T _A = 25 °C	P _D	3.6 ^{b, c}	
	T _A = 70 °C	1 –	2.3 ^{b, c}	
Operating junction and storage temperature range		T _J , T _{stq}	-55 to +150	
Soldering recommendations (peak temperature) ^{d, e}			260	- °C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient b, f	t ≤ 10 s	R _{thJA}	26	35	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	4	5.5	0/10

Notes

a. Package limited

b. Surface mounted on 1" x 1" FR4 board

d. The DFN 5x6 package is a leadless package. The end of the lead terminal is exposed copper(not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

f. Maximum under steady state conditions is 80 °C/W

c. t = 10 s

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			•	•			
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 V, I_D = 250 \mu A$	60	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA	-	38	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-4.9	-	— mV/°C	
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.2	-	2.7	V	
Gate-body leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	100	nA	
Zero gate voltage drain current		$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1		
	I _{DSS}	$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 85 ^{\circ}\text{C}$	-	-	10	μA	
On-state drain current ^b	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	60	-	-	Α	
Drain-source on-state resistance b	_	V _{GS} = 10 V, I _D = 11 A	-	0.032	-		
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	-	0.038	-	Ω	
Forward transconductance b	9 _{fs}	V _{DS} = 30 V, I _D = 11 A	-	38	-	S	
Dynamic ^a			•	•		•	
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz -	-	1050	-	pF	
Output capacitance	C _{oss}		-	435	-		
Reverse transfer capacitance	C _{rss}		20	-	1		
Tatal asta abavas		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 11 \text{ A}$	-	15.2	23	nC	
Total gate charge	Qg		-	7.1	11		
Gate-source charge	Q _{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 11 \text{ A}$	-	4.4	-		
Gate-drain charge	Q _{gd}		-	1.3	-		
Gate resistance	Rg	f = 1 MHz	0.12	0.6	1.2	Ω	
Turn-on delay time	t _{d(on)}		-	15	120	-	
Rise time	t _r	V_{DD} = 30 V, R_L = 3.45 Ω	-	80	30		
Turn-off delay time	t _{d(off)}	$\text{I}_\text{D}\cong \textbf{8.7}~\text{A},~\text{V}_\text{GEN}=\textbf{4.5}~\text{V},~\text{R}_\text{g}=\textbf{1}~\Omega$	-	15	30		
Fall time	t _f		-	15	30		
Turn-on delay time	t _{d(on)}		-	10	15	ns	
Rise time	t _r	V_{DD} = 30 V, R_L = 3.45 Ω I_D \cong 8.7 A, V_{GEN} = 10 V, R_g = 1 Ω	-	25	40	-	
Turn-off delay time	t _{d(off)}		-	20	30		
Fall time	t _f		-	10	15		
Drain-Source Body Diode Characteristic	s		•	•	•		
Continuous source-drain diode Current	Is	T _C = 25 °C	-	-	8	٨	
Pulse diode forward current ^a	I _{SM}	-		-	40	A	
Body diode voltage	V _{SD}	I _S = 8.7 A	-	0.8	1.2	V	
Body diode reverse recovery time	t _{rr}		-	34	51	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = 8.7 A, di/dt = 100 A/μs,	-	30	45	nC	
Reverse recovery fall time	ta	$T_J = 25 \ ^{\circ}C$	-	16	-	ns	
Reverse recovery rise time	t _b		-	18	-		

Notes

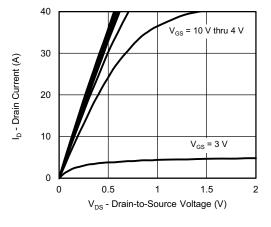
a. Guaranteed by design, not subject to production testing

b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

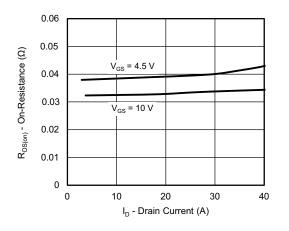
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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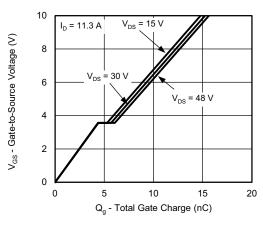




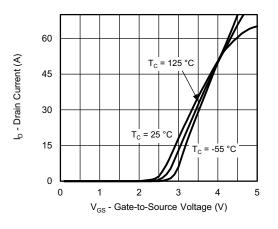
Output Characteristics



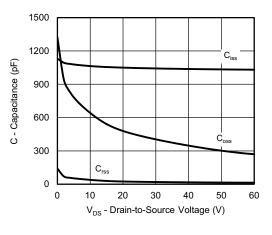
On-Resistance vs. Drain Current



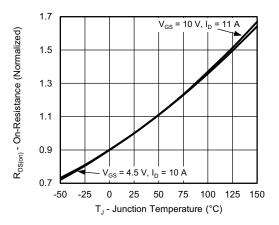
Gate Charge



Transfer Characteristics

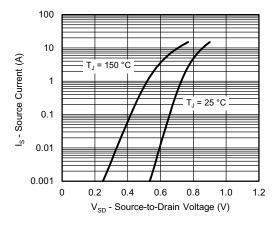


Capacitance

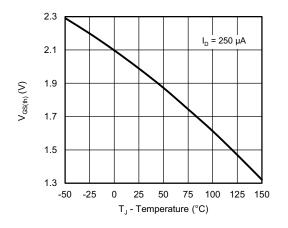


On-Resistance vs. Junction Temperature

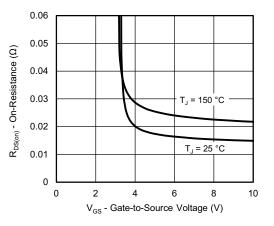




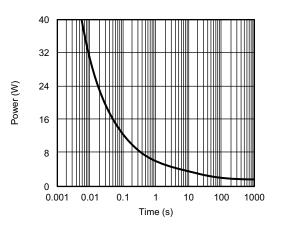
Source-Drain Diode Forward Voltage



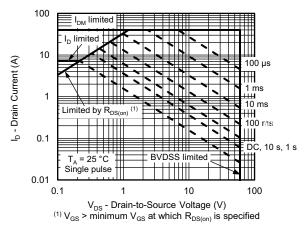
Threshold Voltage



On-Resi.0stance vs. Gate-to-Source Voltage

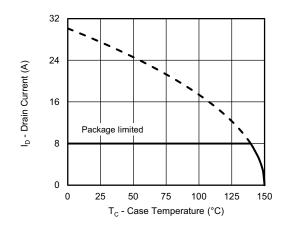




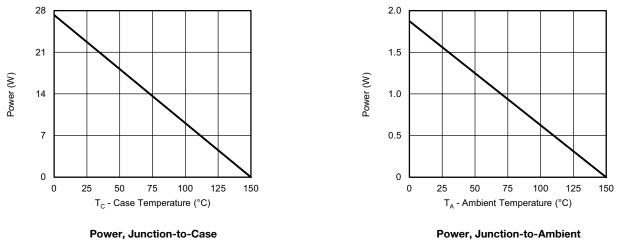


Safe Operating Area, Junction-to-Ambient





Current Derating a

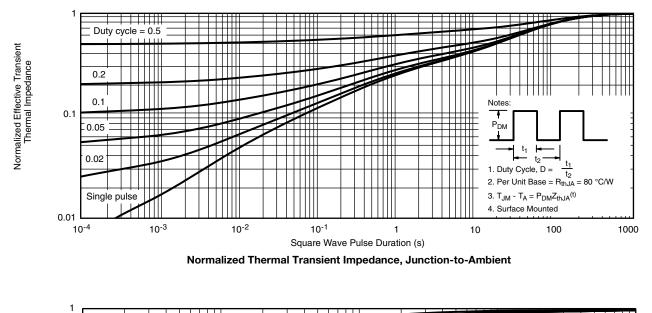


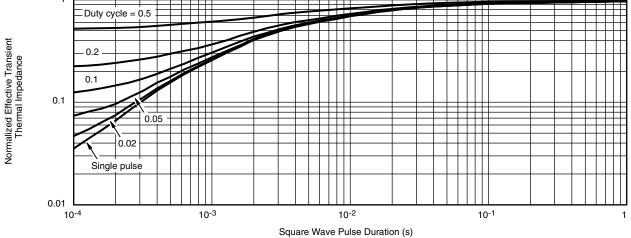
Power, Junction-to-Ambient

Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit







Normalized Thermal Transient Impedance, Junction-to-Case



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