

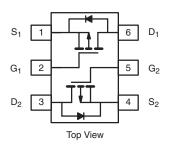
### Dual P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)			
- 20	0.155 at V <sub>GS</sub> = - 4.5V	- 1.8	2.7 nC			
	0.235 at V <sub>GS</sub> = - 2.5 V	- 1.5	2.7 110			

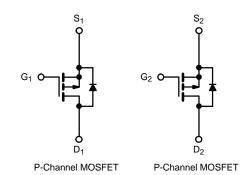
#### FEATURES

- Halogen-free According to IEC 61249-2-21
   Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC





SC-70-6



Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	- 20	V	
Gate-Source Voltage		V <sub>GS</sub>	± 12	V	
	T <sub>C</sub> = 25 °C		- 1.8		
Continuous Drain Current (T $= 150$ °C)	T <sub>C</sub> = 70 °C	I <sub>D</sub>	- 1.5		
Continuous Drain Current ( $T_J = 150 \ ^{\circ}C$ )	T <sub>A</sub> = 25 °C		- 1.6 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		-1.1 <sup>b, c</sup>	A	
Pulsed Drain Current		I <sub>DM</sub>	- 2.5		
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C		- 1.17		
	T <sub>A</sub> = 25 °C	۱ <sub>s</sub>	- 0.95 <sup>b, c</sup>		
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		1.4		
	T <sub>C</sub> = 70 °C		0.9	w	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	1.14 <sup>b, c</sup>	VV	
	T <sub>A</sub> = 70 °C	1	0.73 <sup>b, c</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	al Maximum		
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 5 s	R <sub>thJA</sub>	93	110	°C/W	
Maximum Junction-to-Foot	Steady State	R <sub>thJF</sub>	75	90		

Notes:

c. t = 5 s.

d. Maximum under steady state conditions is 150 °C/W.

<sup>a. T<sub>C</sub> = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.</sup> 



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = -250 \mu A$	- 20			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = - 250 μA		- 17		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = -250 \mu\text{A}$		3.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -250 \ \mu A$	- 0.5		- 1.5	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 12 V$			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -20 V, V_{GS} = 0 V$	<sub>S</sub> = 0 V		1	
		$V_{DS}$ = - 20 V, $V_{GS}$ = 0 V, $T_{J}$ = 55 °C			10	- μΑ
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \leq$ - 5 V, $V_{GS}$ = - 4.5V	- 8			Α
		$V_{GS} = -4.5 V$ , $I_{D} = -2.5 A$		0.155		Ω
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 1 A		0.235		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 2.6 A		5		S
Dynamic <sup>b</sup>	-1					
Input Capacitance	C <sub>iss</sub>			210		pF
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		45		
Reverse Transfer Capacitance	C <sub>rss</sub>			33		
Total Gate Charge		$V_{DS}$ = - 15 V, $V_{GS}$ = - 4.5 V, I <sub>D</sub> = - 2.6 A		5.2	8	nC
Total Gale Charge				2.7	4	
Gate-Source Charge	Q <sub>gs</sub>	$V_{\text{DS}}$ = - 15 V, $V_{\text{GS}}$ = - 4.5 V, $I_{\text{D}}$ = - 2.6 A		0.94		
Gate-Drain Charge	Q <sub>gd</sub>			1.3		
Gate Resistance	Rg	f = 1 MHz	2	7	14	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			39	59	ns
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 15 V, $R_L$ = 7.1 $\Omega$		25	38	
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong$ - 2.1 A, $\text{V}_\text{GEN}$ = - 4.5 V, $\text{R}_\text{g}$ = 1 $\Omega$		13	20	
Fall Time	t <sub>f</sub>			9	18	
Turn-On Delay Time	t <sub>d(on)</sub>			5	10	
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 15 V, $R_L$ = 7.1 $\Omega$		10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong$ - 2.1 A, $\text{V}_\text{GEN}$ = - 4.5 V, Rg= 1 $\Omega$		14	21	
Fall Time	t <sub>f</sub>			7	14	
Drain-Source Body Diode Characteristi	cs					
Continuous Source-Drain Diode Current	ا <sub>S</sub>	$T_{\rm C} = 25 \ ^{\circ}{\rm C}$		1.17		A
Pulse Diode Forward Current	I <sub>SM</sub>			8		
Body Diode Voltage	V <sub>SD</sub>	$I_{S} = -2.1 \text{ A}, V_{GS} = 0 \text{ V}$		0.85	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>			13	20	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = - 2.1 A, dl/dt = 100 A/μs, T <sub>.1</sub> = 25 °C		6	12	nC
Reverse Recovery Fall Time	t <sub>a</sub>	$r_{\rm F} = 2.173, a_{\rm F} a_{\rm C} = 10070\mu_0, r_{\rm J} = 20.0$		9		200
Reverse Recovery Rise Time	t <sub>b</sub>			4		ns

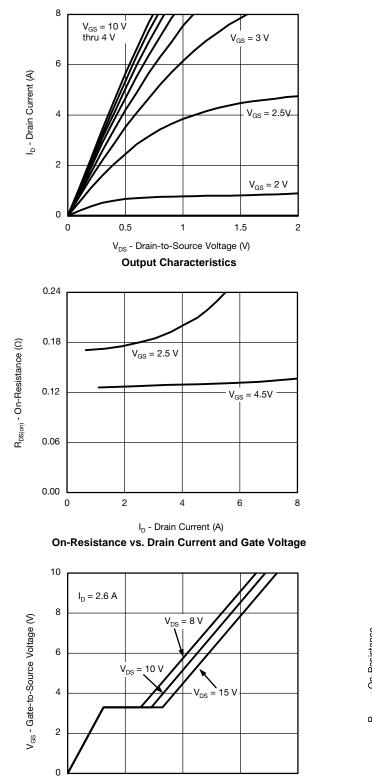
Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





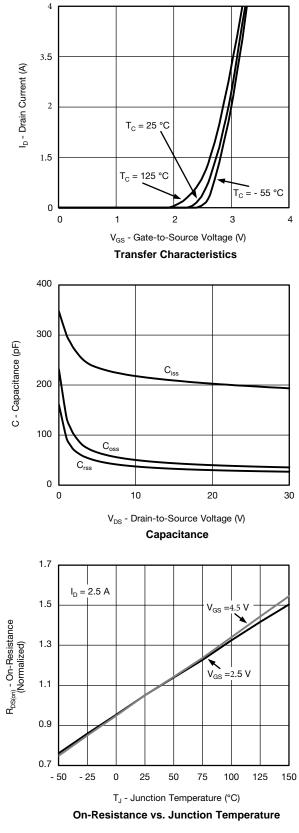
Q<sub>g</sub> - Total Gate Charge (nC) Gate Charge

3

4.5

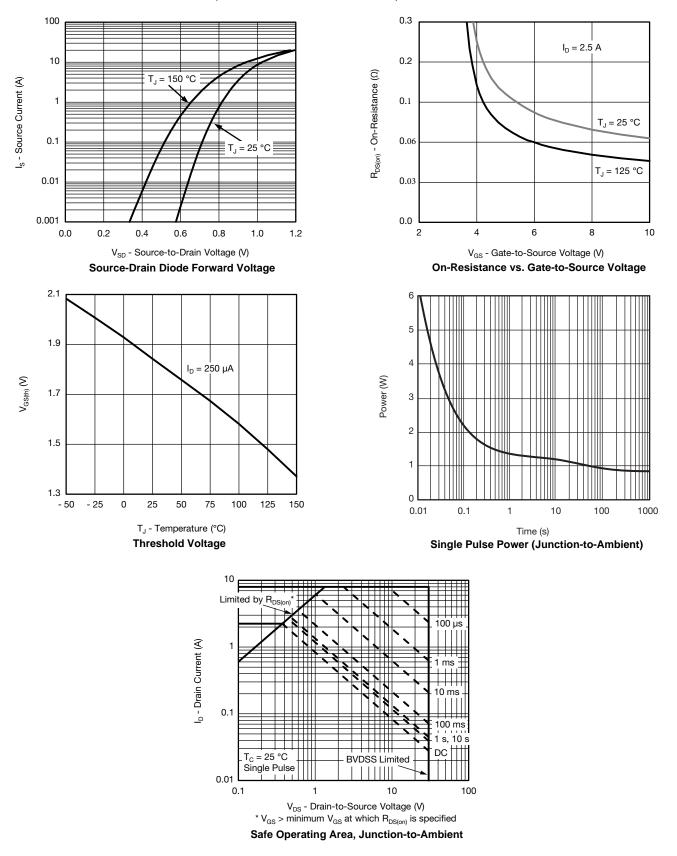
6

1.5

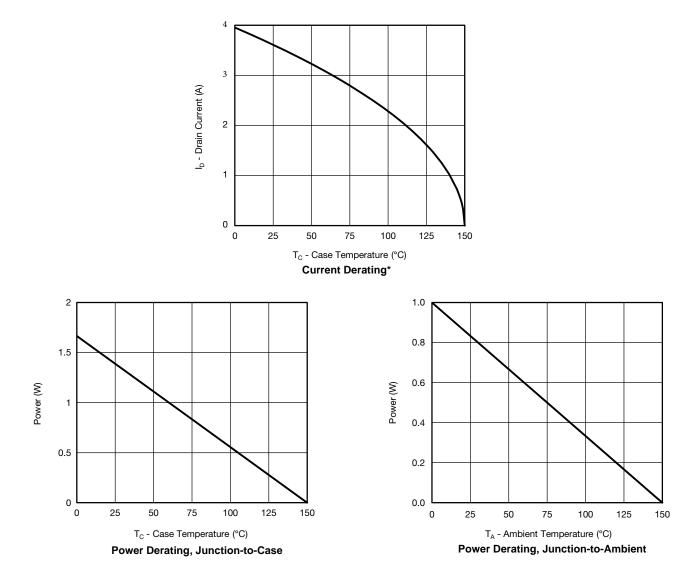


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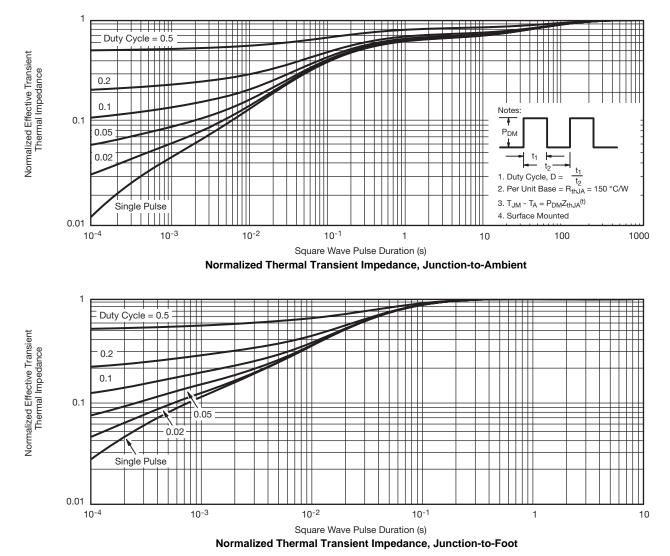






\* The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.







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