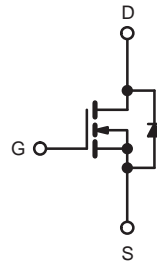


Power MOSFET

| PRODUCT SUMMARY | | |
|---------------------------|------------------------|-------|
| V_{DS} (V) | 100 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10\text{ V}$ | 0.020 |
| Q_g (Max.) (nC) | 70 | |
| Q_{gs} (nC) | 13 | |
| Q_{gd} (nC) | 39 | |
| Configuration | Single | |

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Low-Profile Through-Hole
- Available in Tape and Reel
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | |
|---|----------------------------------|-----------------------------------|----------------|------------------|---------------------|
| PARAMETER | | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | | V_{DS} | 100 | V |
| Gate-Source Voltage | | | V_{GS} | ± 20 | |
| Continuous Drain Current | V_{GS} at 10 V | $T_C = 25\text{ }^\circ\text{C}$ | I_D | 70 | A |
| | | $T_C = 100\text{ }^\circ\text{C}$ | | 56 | |
| Pulsed Drain Current ^{a, e} | | | I_{DM} | 250 | |
| Linear Derating Factor | | | | 1.0 | W/ $^\circ\text{C}$ |
| Single Pulse Avalanche Energy ^{b, e} | | | E_{AS} | 580 | mJ |
| Avalanche Current ^a | | | I_{AR} | 20 | A |
| Repetitive Avalanche Energy ^a | | | E_{AR} | 13 | mJ |
| Maximum Power Dissipation | $T_C = 25\text{ }^\circ\text{C}$ | | P_D | 3.1 | W |
| | $T_A = 25\text{ }^\circ\text{C}$ | | | 130 | |
| Peak Diode Recovery dV/dt ^{c, e} | | | dV/dt | 5.0 | V/ns |
| Operating Junction and Storage Temperature Range | | | T_J, T_{stg} | - 55 to + 150 | $^\circ\text{C}$ |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300 ^d | |

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 2.7\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 18\text{ A}$ (see fig. 12).
- $I_{SD} \leq 20\text{ A}$, $dI/dt \leq 150\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | |
|--|-------------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient (PCB Mounted, Steady-State) ^a | R _{thJA} | - | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | R _{thJC} | - | 1.0 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | | |
|---|----------------------------------|--|--|------|-------|-------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | | 100 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA ^c | | - | 0.29 | - | V/°C |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 20 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 100 V, V _{GS} = 0 V | | - | - | 25 | μA |
| | | V _{DS} = 80 V, V _{GS} = 0 V, T _J = 125 °C | | - | - | 250 | |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 11 A ^b | - | 0.020 | - | Ω |
| Forward Transconductance | g _{fs} | V _{DS} = 50 V, I _D = 11 A ^d | | 6.7 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^d | | - | 1300 | - | pF |
| Output Capacitance | C _{oss} | | | - | 430 | - | |
| Reverse Transfer Capacitance | C _{rss} | | | - | 130 | - | |
| Total Gate Charge | Q _g | V _{GS} = 10 V | I _D = 20 A, V _{DS} = 160 V, see fig. 6 and 13 ^{b, c} | - | - | 70 | nC |
| Gate-Source Charge | Q _{gs} | | | - | - | 13 | |
| Gate-Drain Charge | Q _{gd} | | | - | - | 39 | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 50 V, I _D = 20 A, R _g = 9.1 Ω, R _D = 5.4 Ω, see fig. 10 ^{b, c} | | - | 14 | - | ns |
| Rise Time | t _r | | | - | 51 | - | |
| Turn-Off Delay Time | t _{d(off)} | | | - | 45 | - | |
| Fall Time | t _f | | | - | 36 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 20 | A |
| Pulsed Diode Forward Current ^a | I _{SM} | | | - | - | 72 | |
| Body Diode Voltage | V _{SD} | T _J = 25 °C, I _S = 20 A, V _{GS} = 0 V ^b | | - | - | 2.0 | V |
| Body Diode Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = 20 A, di/dt = 100 A/μs ^{b, c} | | - | 300 | 610 | ns |
| Body Diode Reverse Recovery Charge | Q _{rr} | | | - | 3.4 | 7.1 | μC |
| Forward Turn-On Time | t _{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D) | | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- c. Uses IRF640/SiHF640 data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

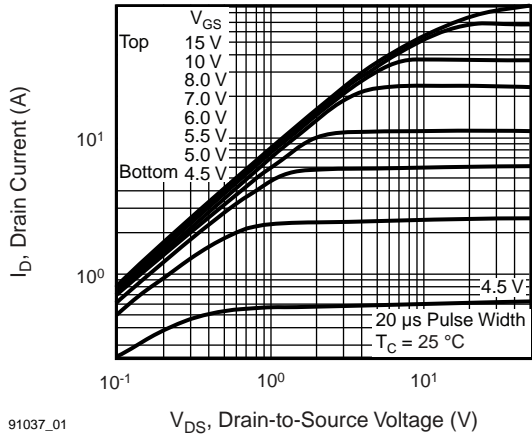


Fig. 1 - Typical Output Characteristics, $T_J = 25\text{ °C}$

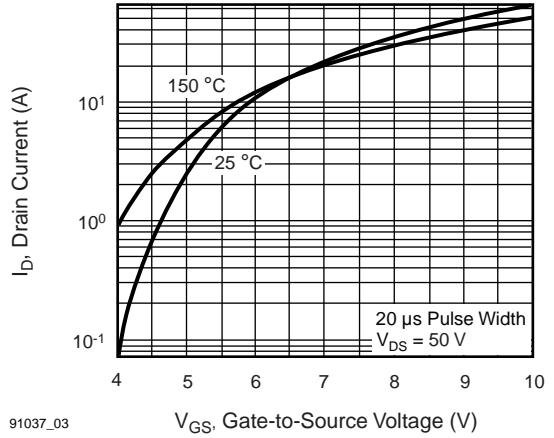


Fig. 3 - Typical Transfer Characteristics

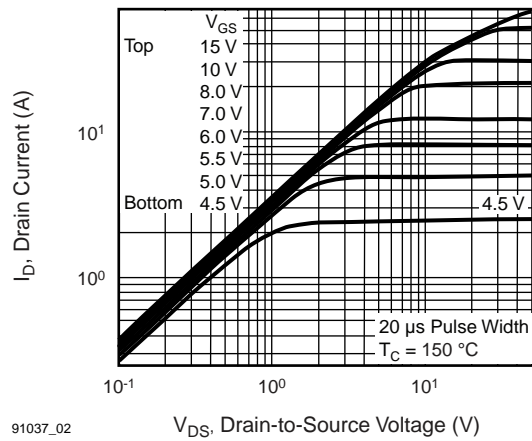


Fig. 2 - Typical Output Characteristics, $T_J = 175\text{ °C}$

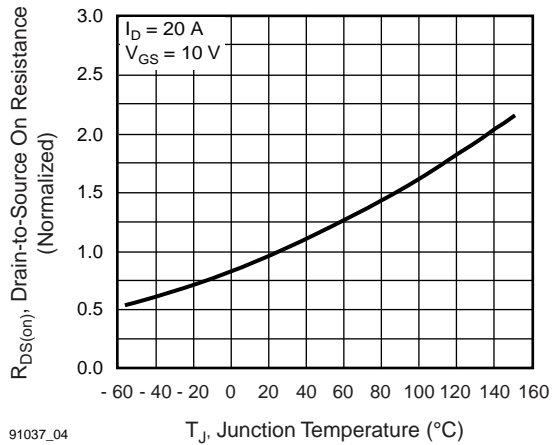


Fig. 4 - Normalized On-Resistance vs. Temperature

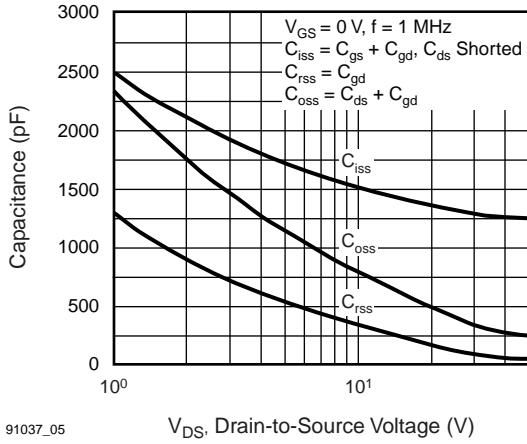


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

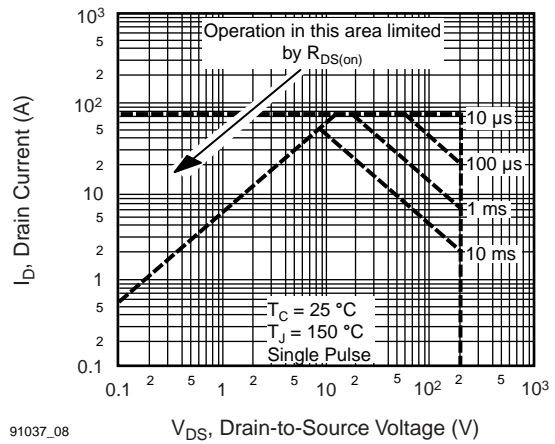


Fig. 8 - Maximum Safe Operating Area

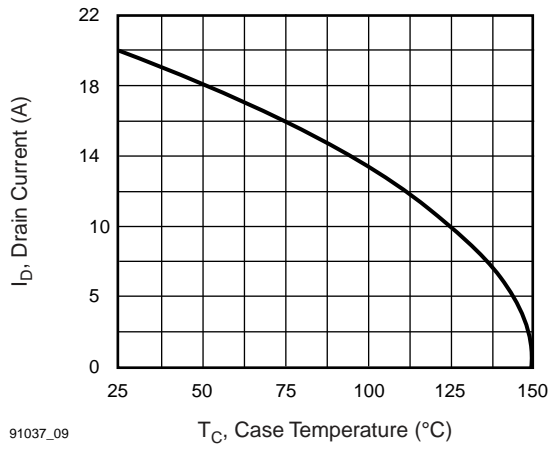


Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 10a - Switching Time Test Circuit

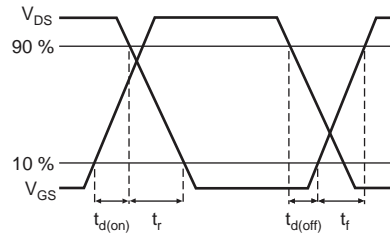


Fig. 10b - Switching Time Waveforms

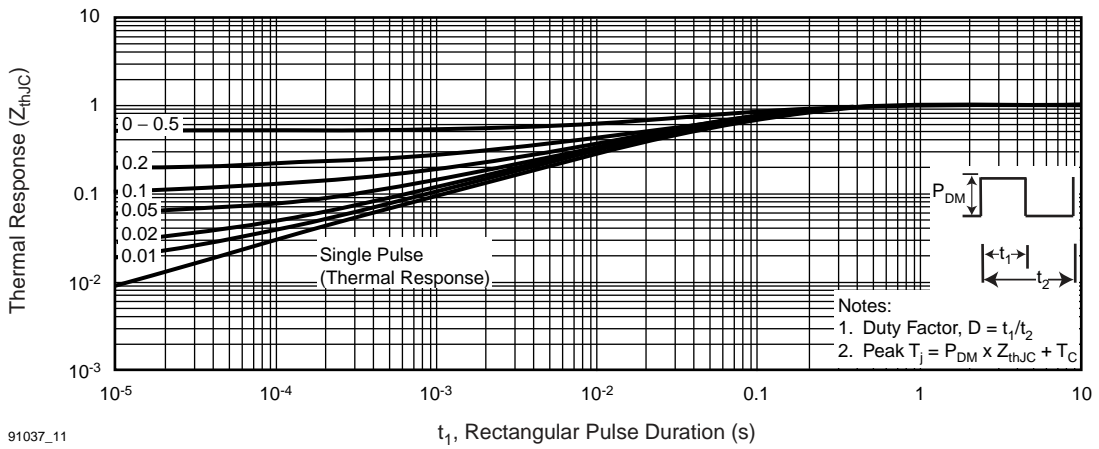


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms

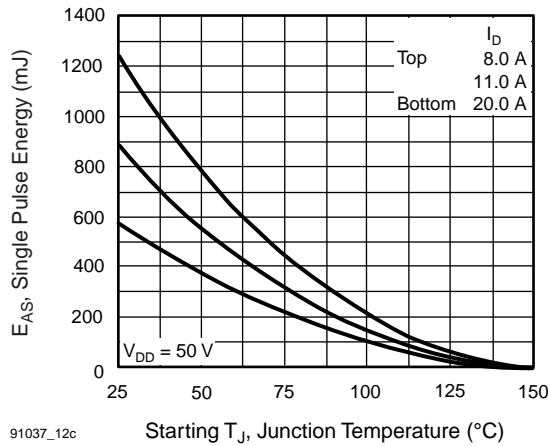


Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 13a - Basic Gate Charge Waveform

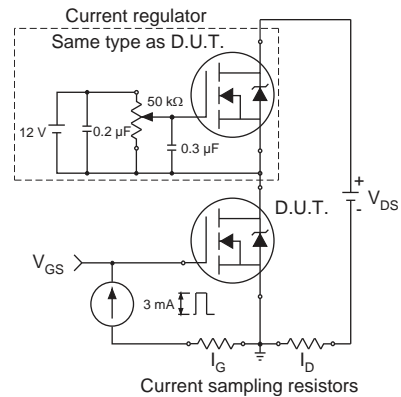
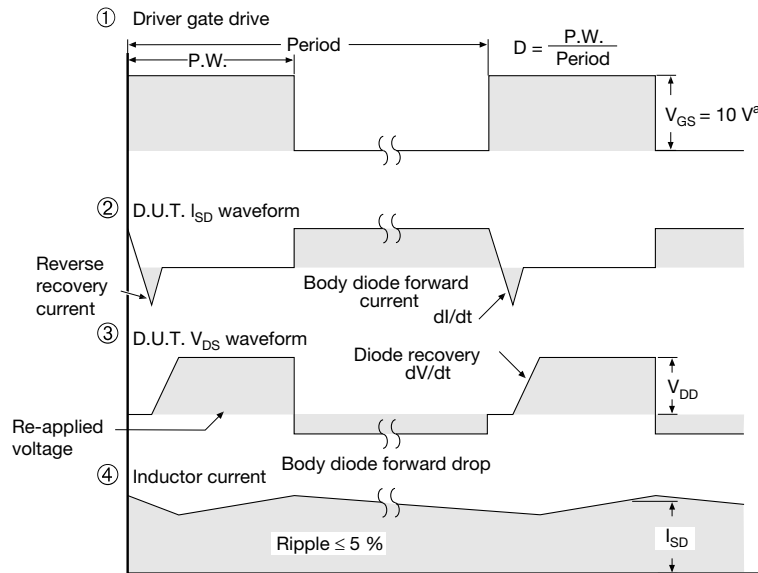


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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