

STM8309-VB Datasheet

N- and P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
N-Channel	30	0.018 at V <sub>GS</sub> = 10 V	8 <sup>e</sup>	6.2
		0.020 at V <sub>GS</sub> = 8 V	8 <sup>e</sup>	
		0.024 at V <sub>GS</sub> = 4.5 V	8 <sup>e</sup>	
P-Channel	- 30	0.040 at V <sub>GS</sub> = - 10 V	- 8 <sup>e</sup>	18.5
		0.044 at V <sub>GS</sub> = - 8 V	- 8 <sup>e</sup>	
		0.050 at V <sub>GS</sub> = - 4.5 V	- 7.5	

FEATURES

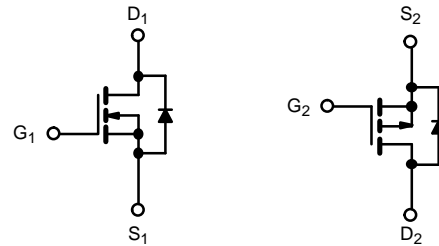
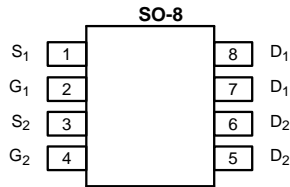
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

APPLICATIONS

- Motor Drive
- Mobile Power Bank



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V <sub>DS</sub>	30	- 30	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	8 <sup>e</sup>	- 8 <sup>e</sup>	A
		T <sub>C</sub> = 70 °C	6.8	- 6.8	
		T <sub>A</sub> = 25 °C	6.8 <sup>b, c</sup>	- 6.6 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	5.4 <sup>b, c</sup>	- 5.3 <sup>b, c</sup>	
Pulsed Drain Current (10 μs Pulse Width)	I <sub>DM</sub>	40	- 40	A	
Source-Drain Current Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	2.6		- 2.6
		T <sub>A</sub> = 25 °C	1.6 <sup>b, c</sup>		- 1.6 <sup>b, c</sup>
Pulsed Source-Drain Current	I <sub>SM</sub>	40	- 40	mJ	
Single Pulse Avalanche Current	I <sub>AS</sub>	10	- 20		
Single Pulse Avalanche Energy	E <sub>AS</sub>	5	20	W	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	3.1		3.2
		T <sub>C</sub> = 70 °C	2		2.1
		T <sub>A</sub> = 25 °C	2 <sup>b, c</sup>		2 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	1.28 <sup>b, c</sup>	1.28 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient <sup>b, d</sup>	R <sub>thJA</sub>	50	62.5	47	62.5	°C/W	
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	30	40	29	38		

Notes:

- a. Based on T<sub>C</sub> = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under steady state conditions is 120 °C/W (n-channel) and 110 °C/W (p-channel).
- e. Package limited.

<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	30		V	
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-30			
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		40	mV/ $^\circ\text{C}$	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-34		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-4.1		
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		5		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	1.0		2.0	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-1.0		-2.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	N-Ch			$\pm 100$	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	P-Ch			$\pm 100$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	$\mu\text{A}$
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-10	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	20		A	
		$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch	-20			
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6.8\text{ A}$	N-Ch		0.018	$\Omega$	
		$V_{GS} = -10\text{ V}, I_D = -8\text{ A}$	P-Ch		0.040		
		$V_{GS} = 8\text{ V}, I_D = 6.7\text{ A}$	N-Ch		0.020		
		$V_{GS} = -8\text{ V}, I_D = -6.5\text{ A}$	P-Ch		0.044		
		$V_{GS} = 4.5\text{ V}, I_D = 6.6\text{ A}$	N-Ch		0.024		
		$V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$	P-Ch		0.050		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 6.8\text{ A}$	N-Ch		27	S	
		$V_{DS} = -15\text{ V}, I_D = -6.7\text{ A}$	P-Ch		25		
<b>Dynamic<sup>a</sup></b>							
Input Capacitance	$C_{iss}$	N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$  P-Channel $V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		510	pF	
Output Capacitance	$C_{oss}$		P-Ch		620		
			N-Ch		95		
Reverse Transfer Capacitance	$C_{rss}$		P-Ch		115		
			N-Ch		33		
Total Gate Charge	$Q_g$		$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	N-Ch			6
		$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$	P-Ch		41.5	63	
		N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	N-Ch		5.8	7	
			P-Ch		16	22	
Gate-Source Charge	$Q_{gs}$	P-Channel $V_{DS} = -20\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$	N-Ch		1.6		
			P-Ch		4.3		
Gate-Drain Charge	$Q_{gd}$		N-Ch		1.4		
			P-Ch		7		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	N-Ch	0.3	1.1	2.3	$\Omega$
			P-Ch	1.2	5.7	9.6	

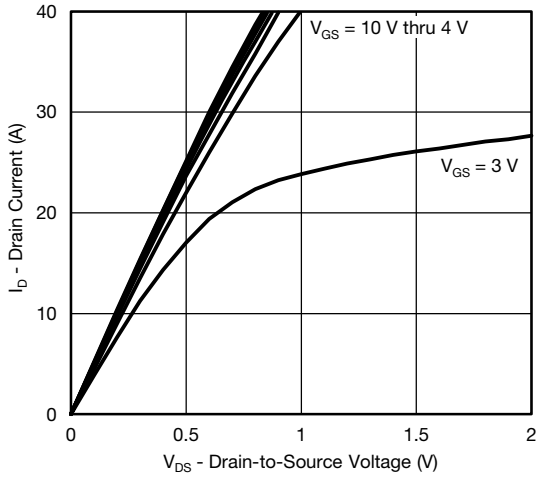
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 20 V, R <sub>L</sub> = 3.7 Ω I <sub>D</sub> ≅ 5.4 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω  P-Channel V <sub>DD</sub> = -20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ -10 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω  N-Channel V <sub>DD</sub> = 20 V, R <sub>L</sub> = 3.7 Ω I <sub>D</sub> ≅ 5.4 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω  P-Channel V <sub>DD</sub> = -20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ -10 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 1 Ω	N-Ch		4	8	ns
			P-Ch		10	16	
Rise Time	t <sub>r</sub>		N-Ch		10	17	
			P-Ch		9	15	
Turn-Off Delay Time	t <sub>d(off)</sub>		N-Ch		16	22	
			P-Ch		23	26	
Fall Time	t <sub>f</sub>		N-Ch		5	9	
			P-Ch		10	16	
Turn-On Delay Time	t <sub>d(on)</sub>	N-Ch		10	16		
		P-Ch		26	35		
Rise Time	t <sub>r</sub>	N-Ch		11	20		
		P-Ch		16	26		
Turn-Off Delay Time	t <sub>d(off)</sub>	N-Ch		13	22		
		P-Ch		16	26		
Fall Time	t <sub>f</sub>	N-Ch		5	9		
		P-Ch		16	26		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	N-Ch			2.6	A
			P-Ch			-2.6	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>		N-Ch			40	
			P-Ch			-40	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 5.4 A	N-Ch		0.81	1.2	V
		I <sub>S</sub> = -2 A	P-Ch		-0.77	-1.2	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	N-Channel I <sub>F</sub> = 5 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C  P-Channel I <sub>F</sub> = -5 A, dI/dt = -100 A/μs, T <sub>J</sub> = 25 °C	N-Ch		12	25	ns
			P-Ch		31	57	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		N-Ch		10	17	nC
			P-Ch		29	47	
Reverse Recovery Fall Time	t <sub>a</sub>		N-Ch		10		ns
			P-Ch		13		
Reverse Recovery Rise Time	t <sub>b</sub>		N-Ch		7		
			P-Ch		23		

Notes:

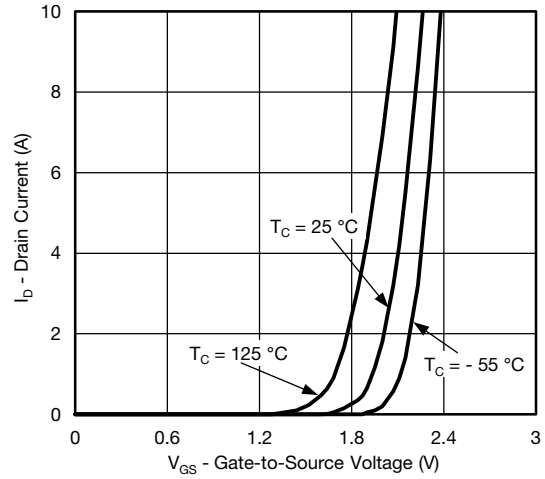
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

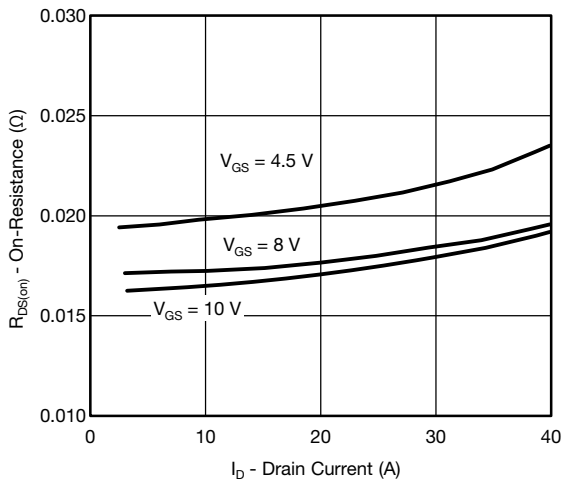
**N-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



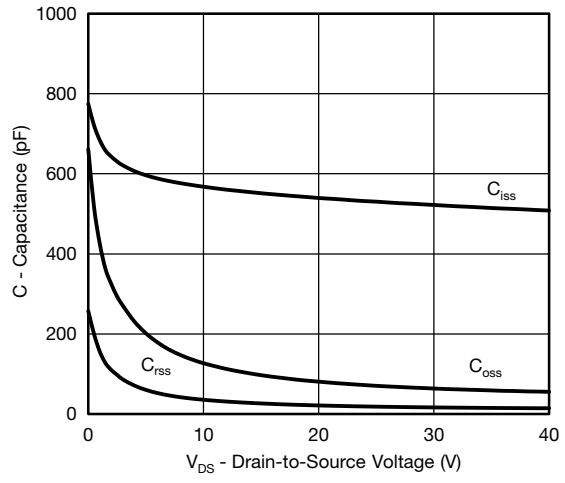
**Output Characteristics**



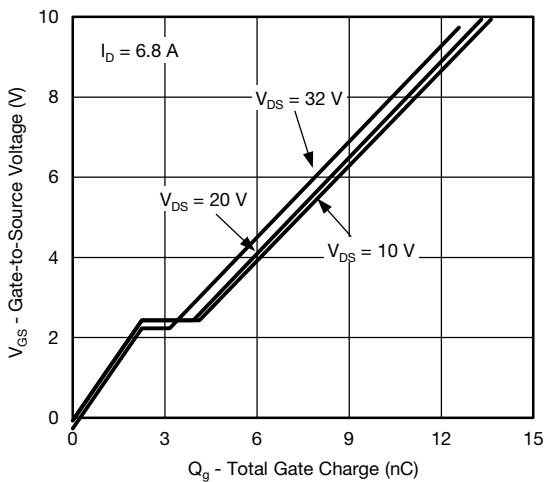
**Transfer Characteristics**



**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

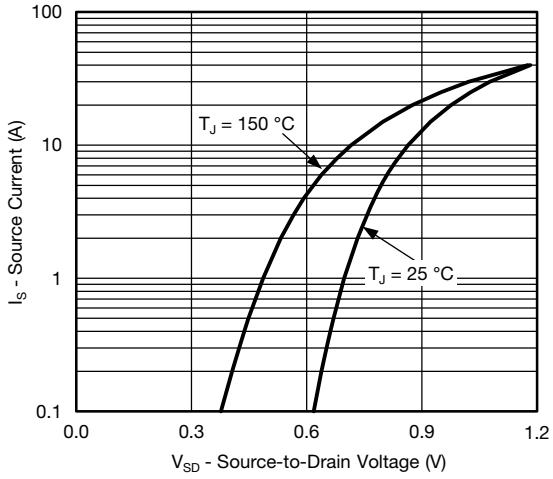


**Gate Charge**

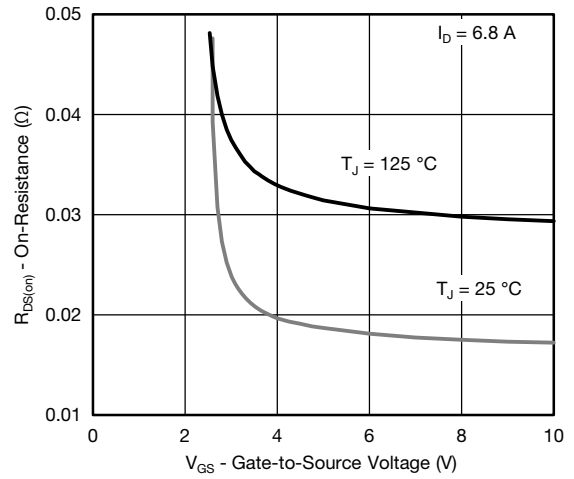


**On-Resistance vs. Junction Temperature**

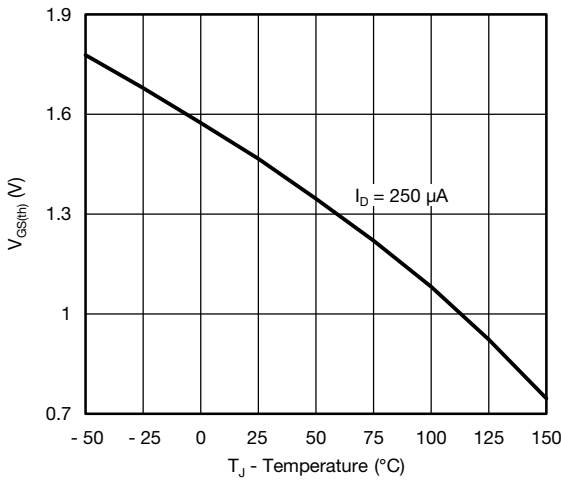
**N-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



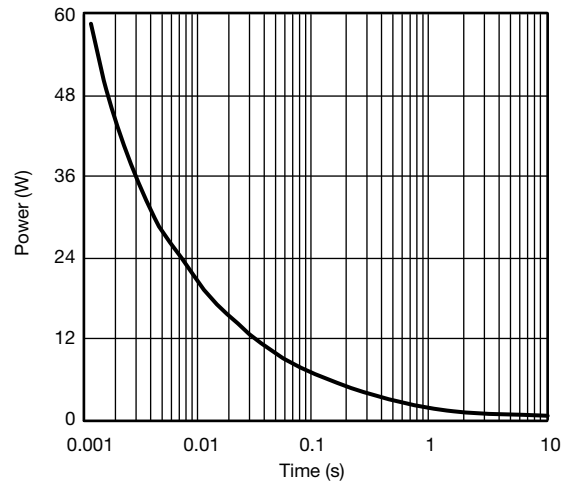
**Source-Drain Diode Forward Voltage**



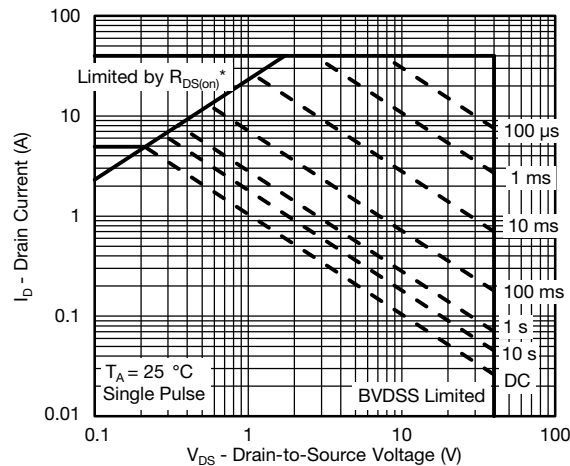
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**

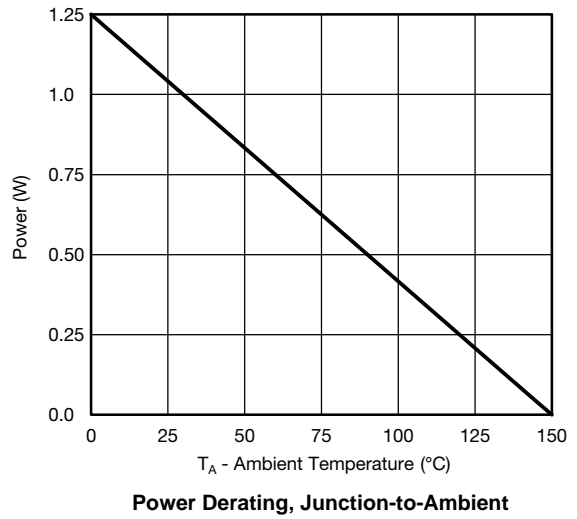
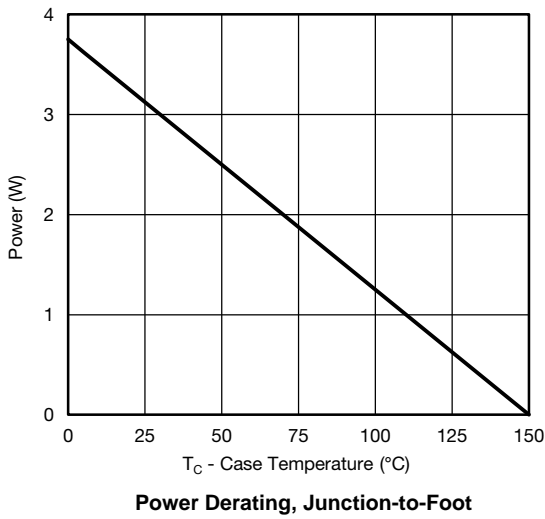
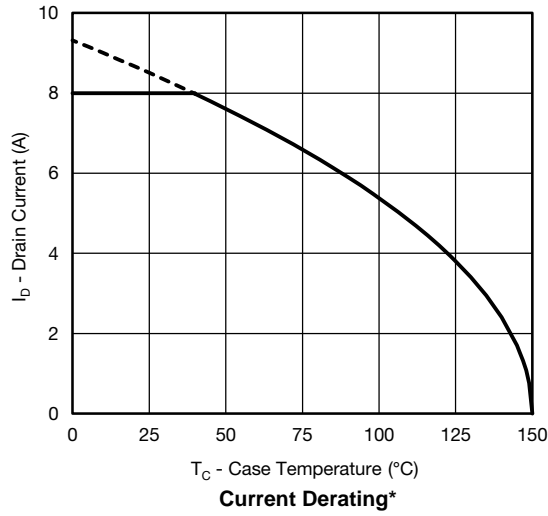


**Single Pulse Power, Junction-to-Ambient**



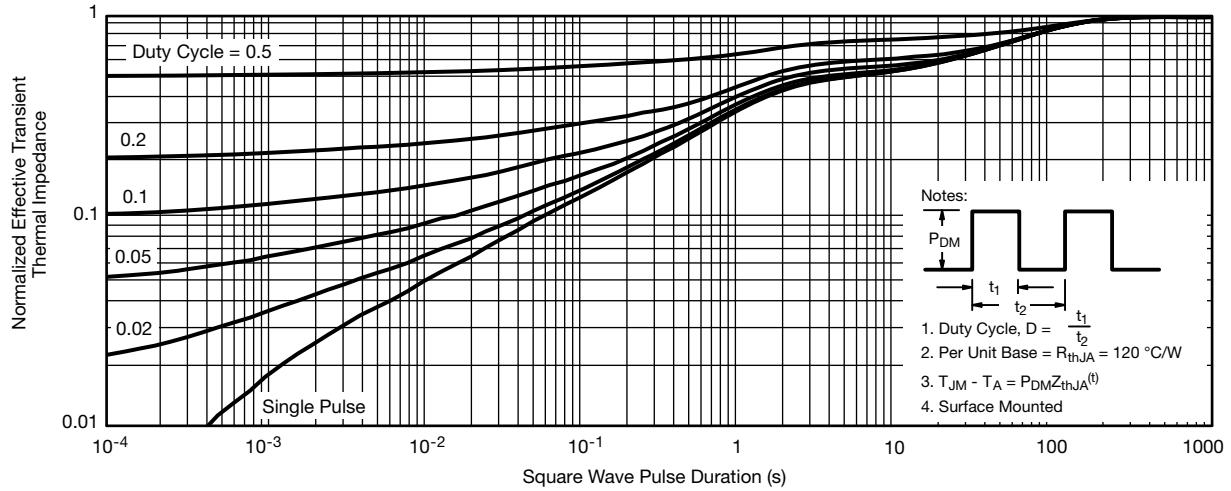
**Safe Operating Area, Junction-to-Ambient**

**N-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

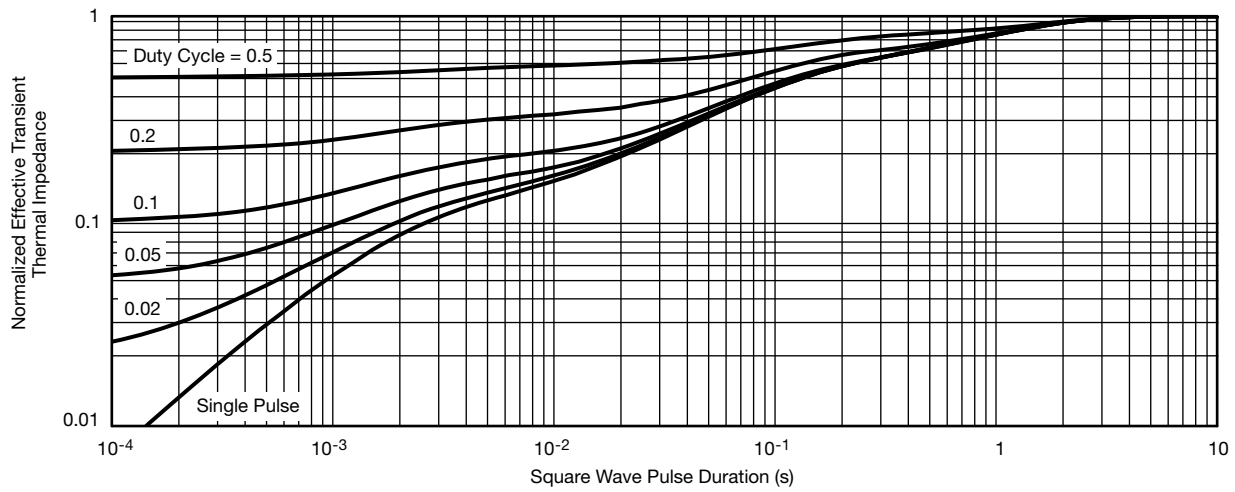


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**N-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

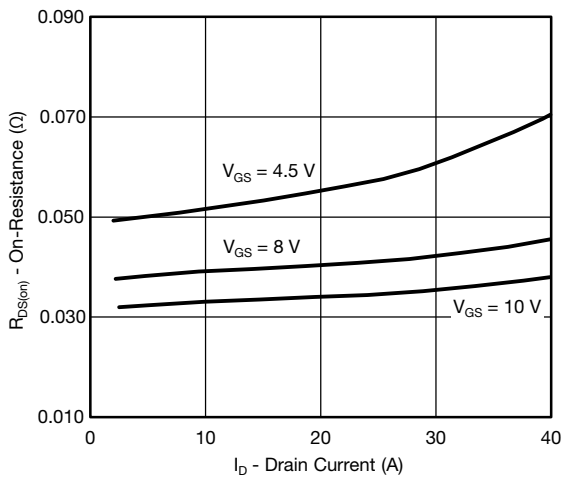
**P-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



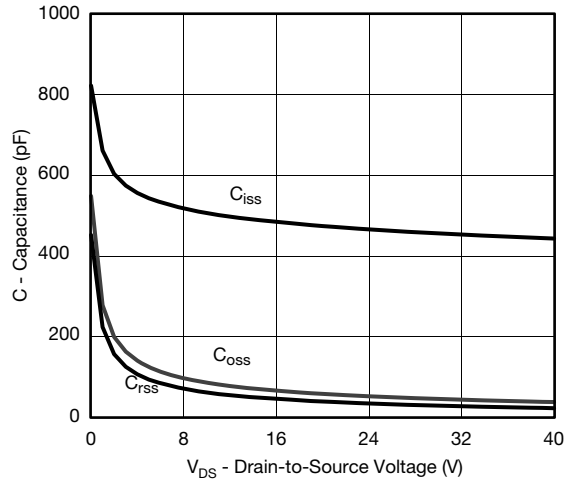
**Output Characteristics**



**Transfer Characteristics**



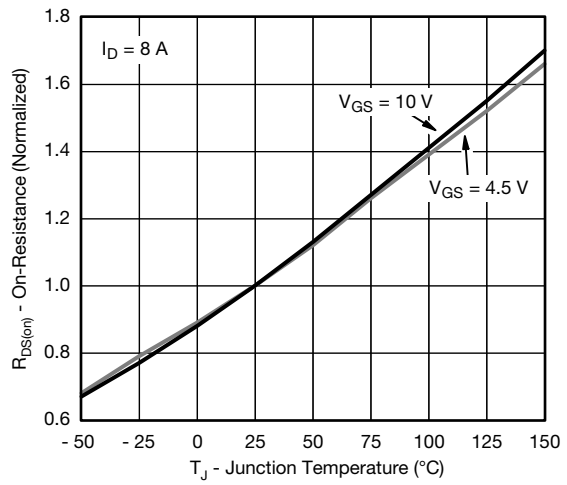
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



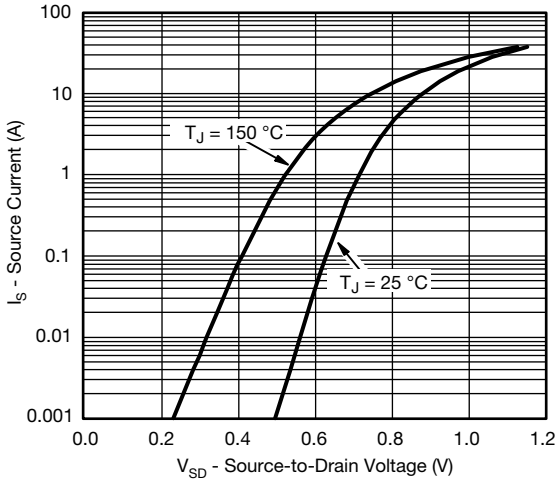
**Gate Charge**



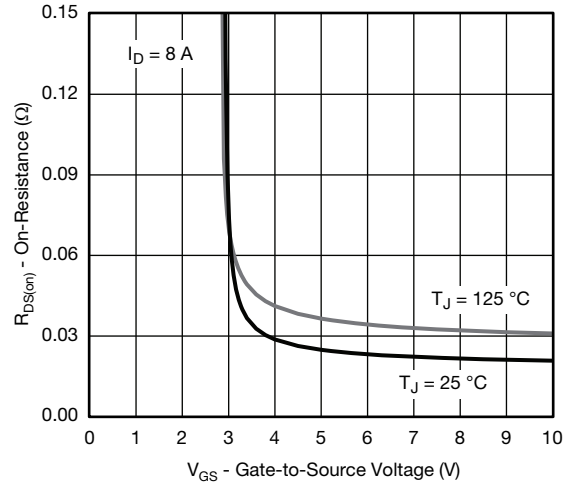
**On-Resistance vs. Junction Temperature**



**P-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



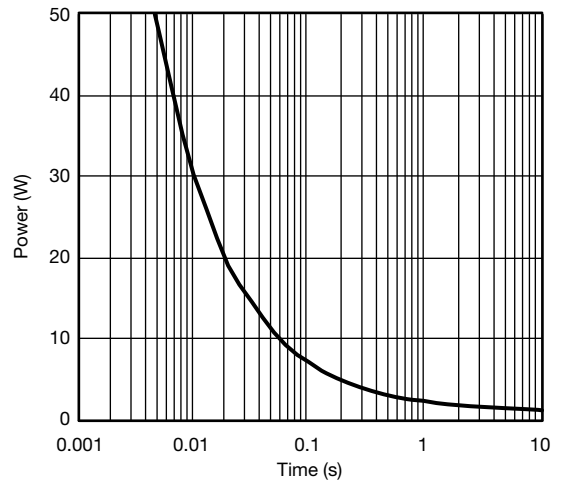
Source-Drain Diode Forward Voltage



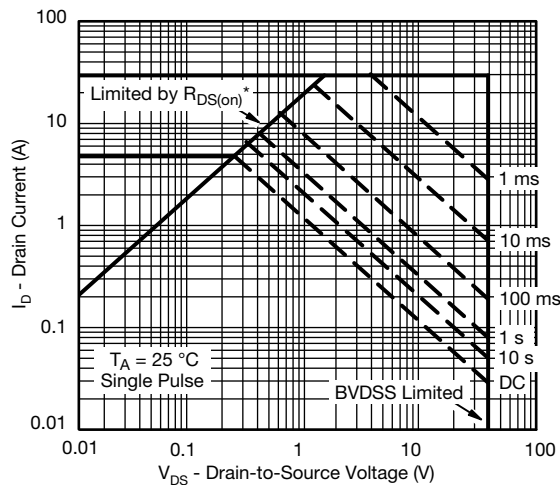
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

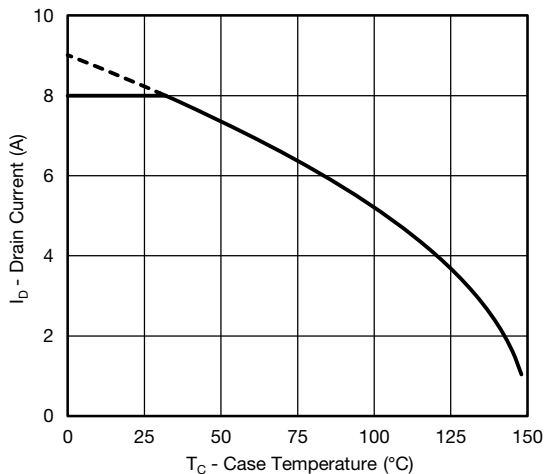


Single Pulse Power, Junction-to-Ambient

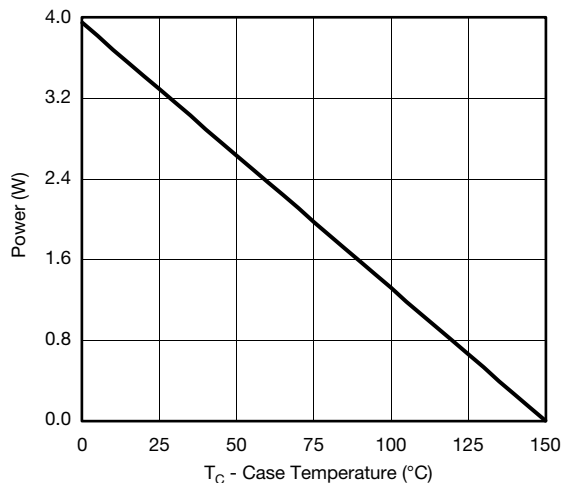


Safe Operating Area, Junction-to-Ambient

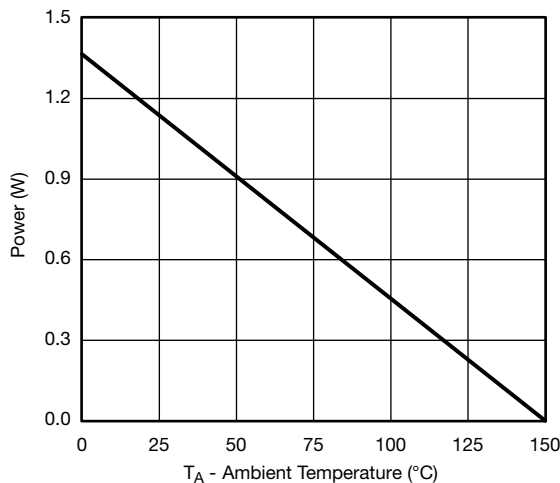
**P-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating\***



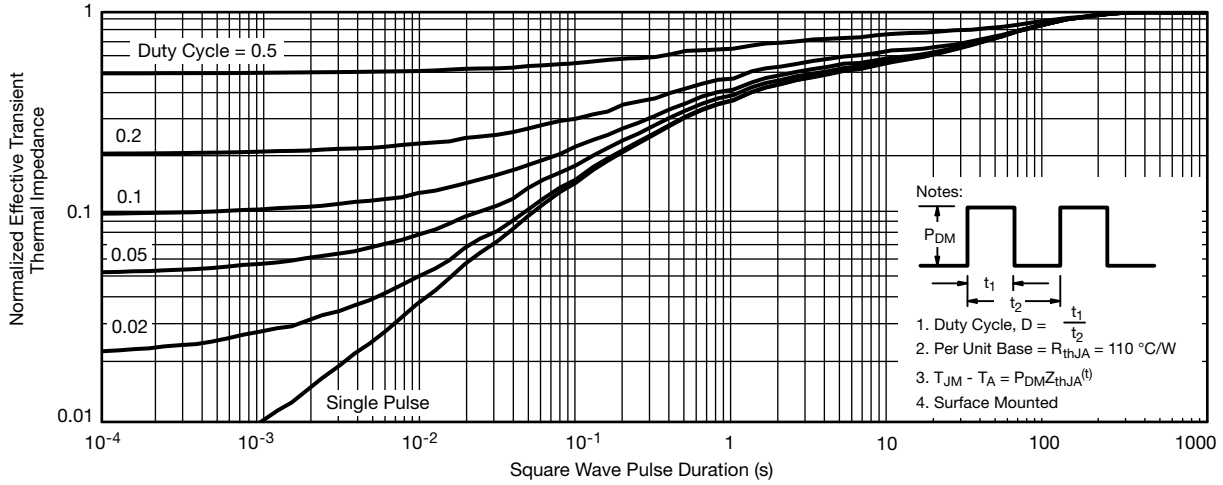
**Power Derating, Junction-to-Foot**



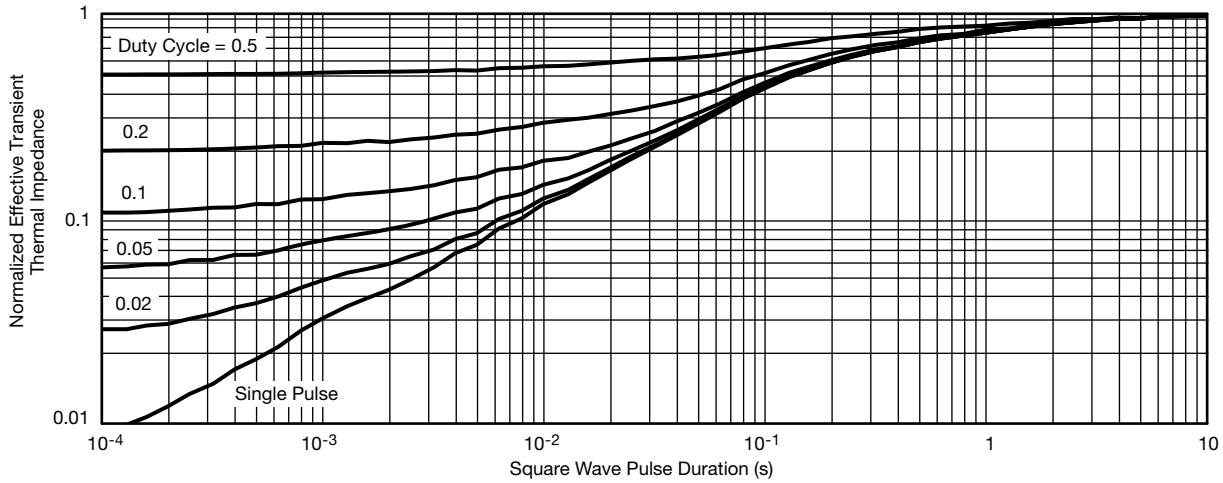
**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**P-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



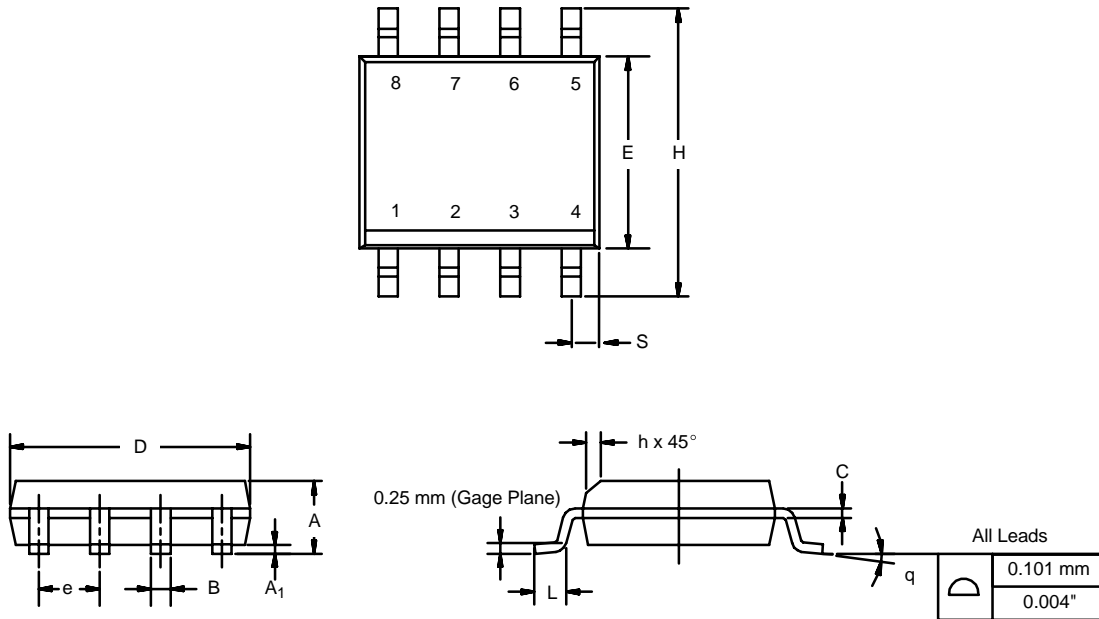
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

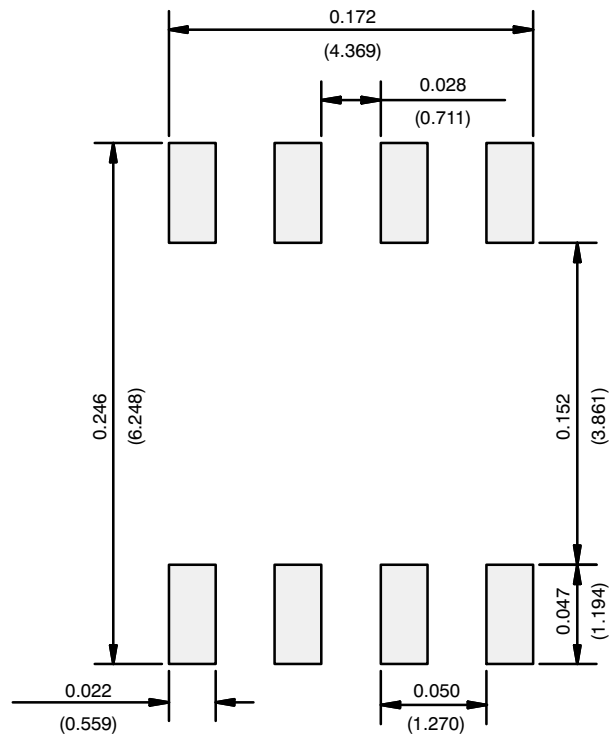
**SOIC (NARROW): 8-LEAD**

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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