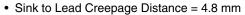


N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	100			
$R_{DS(on)}\left(\Omega\right)$	V _{GS} = 10 V	0.086		
Q _g (Max.) (nC)	72			
Q _{gs} (nC)	11			
Q _{gd} (nC)	32			
Configuration	Single			

FEATURES

- · Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz

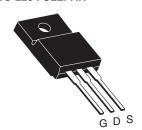


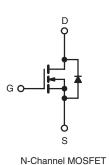
- 175 °C Operating Temperature
- · Dynamic dV/dt Rating
- · Low Thermal Resistance
- Lead (Pb)-free Available











ABSOLUTE MAXIMUM RATINGS T	_C = 25 °C, u	nless otherw	ise noted			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V_{DS}	100	V	
Gate-Source Voltage			V_{GS}	± 20	\	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	- I _D	18		
	VGS at 10 V	T _C = 100 °C		12	A	
Pulsed Drain Current ^a			I _{DM}	68		
Linear Derating Factor				0.32	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	720	mJ	
Repetitive Avalanche Current ^a			I _{AR}	17	Α	
Repetitive Avalanche Energy ^a			E_{AR}	4.8	mJ	
Maximum Power Dissipation	T _C =	: 25 °C	P_{D}	48	W	
Peak Diode Recovery dV/dt ^c			dV/dt	5.5	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature)	for	10 s		300 ^d	°C	
Mounting Torque	6-32 or M3 screw			10	lbf ⋅ in	
				1.1	N⋅m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. $V_{DD} = 25 \text{ V}$, starting $T_J = 25 \,^{\circ}\text{C}$, $L = 3.7 \,\text{mH}$, $R_G = 25 \,\Omega$, $I_{AS} = 17 \,\text{A}$ (see fig. 12). c. $I_{SD} \le 17 \,\text{A}$, $dI/dt \le 200 \,\text{A}/\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_J \le 175 \,^{\circ}\text{C}$.
- d. 1.6 mm from case.



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	65	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	3.1	C/VV	

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	100	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	-	0.13	-	V/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		1.0	-	3.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zana Oata Wallana Busin Oamani		V _{DS} =	V _{DS} = 100 V, V _{GS} = 0 V		-	25	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V	V _{GS} = 0 V, T _J = 150 °C	-	-	250	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A ^b	-	0.086	-	Ω
Forward Transconductance	9 _{fs}	$V_{DS} = 50 \text{ V}, I_{D} = 10 \text{ Ab}$		9.1	-	-	S
Dynamic							
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ $f = 1.0 \text{ MHz}, \text{ see fig. 5}$ $f = 1.0 \text{ MHz}$		-	1700	-	_
Output Capacitance	C _{oss}			-	560	-	
Reverse Transfer Capacitance	C _{rss}			-	120	-	pF
Drain to Sink Capacitance	С			-	12	-	
Total Gate Charge	Qg		I _D = 17 A, V _{DS} = 80 V, see fig. 6 and 13 ^b	-	-	72	nC
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V		-	-	11	
Gate-Drain Charge	Q _{gd}			-	-	32	
Turn-On Delay Time	t _{d(on)}		-		11	-	- ns
Rise Time	t _r	$V_{DD} = 50 \text{ V, } I_D = 17 \text{ A,}$ $R_G = 9.1 \Omega, R_D = 2.9 \Omega,$ see fig. 10^b		-	44	-	
Turn-Off Delay Time	t _{d(off)}			-	53	-	
Fall Time	t _f			-	43	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	
Internal Source Inductance	L _S			-	7.5	-	- nH
Drain-Source Body Diode Characteristic	s					<u>'</u>	,
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	17	- A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	68	
Body Diode Voltage	V_{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 17 \text{A}, V_{GS} = 0 \text{V}^{\text{b}}$		-	-	2.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 17 A, dl/dt = 100 A/μs ^b		_	180	360	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	1.3	2.6	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					_D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300~\mu s;$ duty cycle $\leq 2~\%.$



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

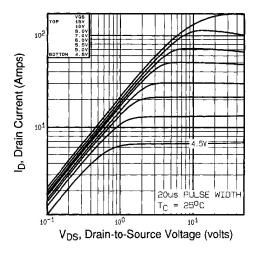


Fig. 1 - Typical Output Characteristics, $T_C = 25$ °C

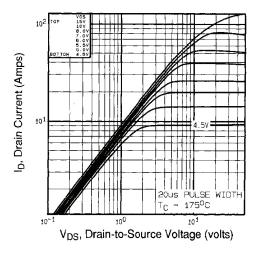


Fig. 2 - Typical Output Characteristics, $T_C = 175$ °C

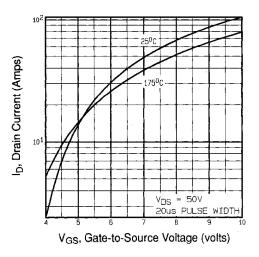


Fig. 3 - Typical Transfer Characteristics

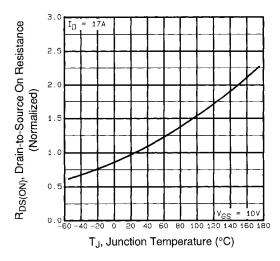


Fig. 4 - Normalized On-Resistance vs. Temperature



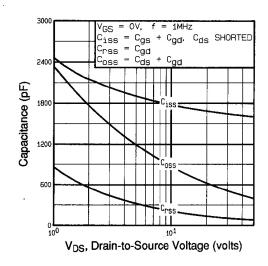


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

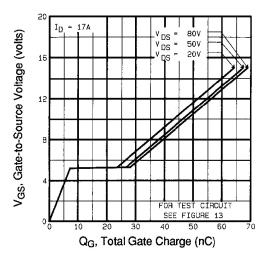


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

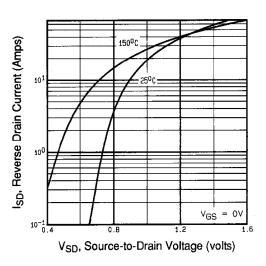


Fig. 7 - Typical Source-Drain Diode Forward Voltage

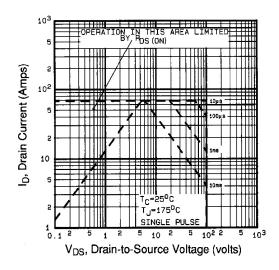


Fig. 8 - Maximum Safe Operating Area



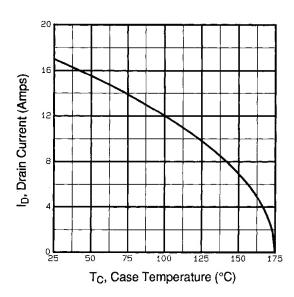


Fig. 9 - Maximum Drain Current vs. Case Temperature

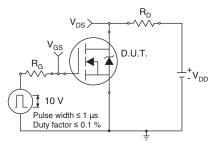


Fig. 10a - Switching Time Test Circuit

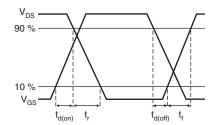


Fig. 10b - Switching Time Waveforms

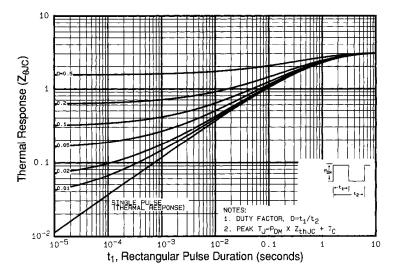


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

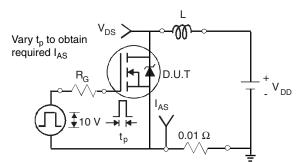


Fig. 12a - Unclamped Inductive Test Circuit

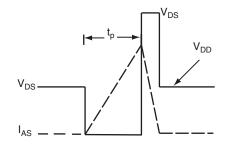


Fig. 12b - Unclamped Inductive Waveforms



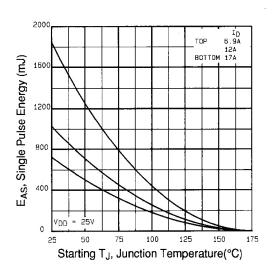


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

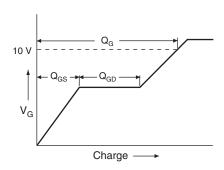


Fig. 13a - Basic Gate Charge Waveform

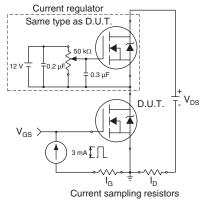
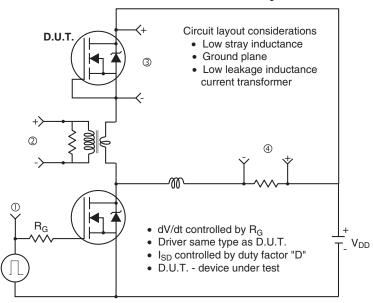
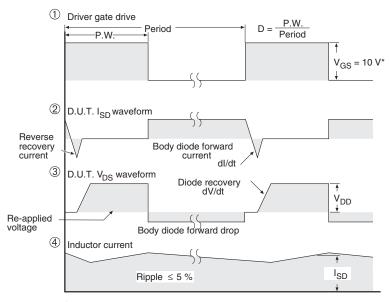


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit





* $V_{GS} = 5 V$ for logic level devices

Fig.14 - For N-Channel



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STF5N65M6 IRF40H233XTMA1 STU5N65M6 DMN6022SSD-13 DMN13M9UCA6-7 DMTH10H4M6SPS-13 DMN2990UFB-7B
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WMJ80N60C4 BXP2N20L BXP2N65D BXT1150N10J BXT1700P06M TSM60NB380CP ROG RQ7L055BGTCR DMNH15H110SK3-13
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