

## Dual N-Channel 60 V (D-S) 175 °C MOSFET

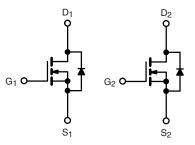
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	60			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.028			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 4.5 V$	0.030			
I <sub>D</sub> (A) per leg	7			
Configuration	Dual			



#### FEATURES

- TrenchFET<sup>®</sup> power MOSFET
- 100 %  $\rm R_g$  and UIS tested





N-Channel MOSFET N-C

N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25 \text{ °C}$ , unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	60	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
Continuous Drain Current	T <sub>C</sub> = 25 °C	I	7		
Continuous Drain Current	T <sub>C</sub> = 125 °C	l <sub>D</sub>	4		
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	3.6	А	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	28		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	18		
Single Pulse Avalanche Energy	L = 0.1 mm	E <sub>AS</sub>	16.2	mJ	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	PD	4	W	
	T <sub>C</sub> = 125 °C		1.3	٧V	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-Ambient	PCB Mount <sup>c</sup>	R <sub>thJA</sub>	110	°C/W		
Junction-to-Foot (Drain)		R <sub>thJF</sub>	34	0/10		

#### Notes

a. Package limited.

b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

c. When mounted on 1" square PCB (FR4 material).

<b>SPECIFICATIONS</b> ( $T_C = 25 \text{ °C}$ ,	SYMBOL	,		MIN.	TYP.	MAX.	LINUT
PARAMETER	STMBUL	TEST CONDITIONS		MIN.	TTP.	MAX.	UNIT
Static					1	[	T
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 250 \mu A$		60	-	-	v
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$		1.5	2.0	2.5	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 60 V	-	-	1	_
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	μA
		$V_{GS} = 0 V$	$V_{DS} = 60 \text{ V}, \text{ T}_{J} = 175 \text{ °C}$	-	-	150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	20	-	-	A
		$V_{GS} = 10 V$	$I_{\rm D} = 4.5 \text{ A}$ -	-	0.028	-	Ω
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.5 A, T <sub>J</sub> = 125 °C I <sub>D</sub> = 4.5 A, T <sub>J</sub> = 175 °C	-	0.066	-	
		$V_{GS} = 10 V$ $V_{GS} = 4.5 V$	$I_D = 4.5 \text{ A}, I_J = 175 \text{ C}$ $I_D = 4 \text{ A}-$	-	0.081	-	
Forward Transconductance <sup>f</sup>	g <sub>fs</sub>		= 15 V, $I_D$ = 4.5 A	-	15	_	s
Dynamic <sup>b</sup>	915	•DS ·	- 10 4, 10 - 4.0 / 1		10	l	
Input Capacitance	C <sub>iss</sub>			_	600	750	Γ
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 25 V, f = 1 MHz	_	110	140	pF
Reverse Transfer Capacitance	C <sub>oss</sub>	VGS - 0 V	$v = v_{DS} = 23 v, i = 1 w_{DZ}$		50	62	
Total Gate Charge <sup>c</sup>				-	11.7	18	
8	Qg		$V_{DS}=30 \text{ V}, \text{ I}_{D}=5.3 \text{ A}$				-
Gate-Source Charge c	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V		-	1.8	2.7	nC
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			- 1.3	2.8	4.2	
Gate Resistance	R <sub>g</sub>		f = 1 MHz		-	6	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	_			7	11	
Rise Time <sup>c</sup>	tr	$\label{eq:VDD} \begin{array}{l} V_{\text{DD}} = 30 \ \text{V}, \ R_{\text{L}} = 6.8 \ \Omega \\ \\ I_{\text{D}} \cong 4.4 \ \text{A}, \ V_{\text{GEN}} = 10 \ \text{V}, \ R_{\text{g}} = 1 \ \Omega \end{array}$		-	3.3	5	- ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	22.4	33.5	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	2.1	3.2	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	28	Α
Forward Voltage	V <sub>SD</sub>	$I_{\rm F} = 2$ A, $V_{\rm GS} = 0$ V		_	0.75	1.1	V

Notes

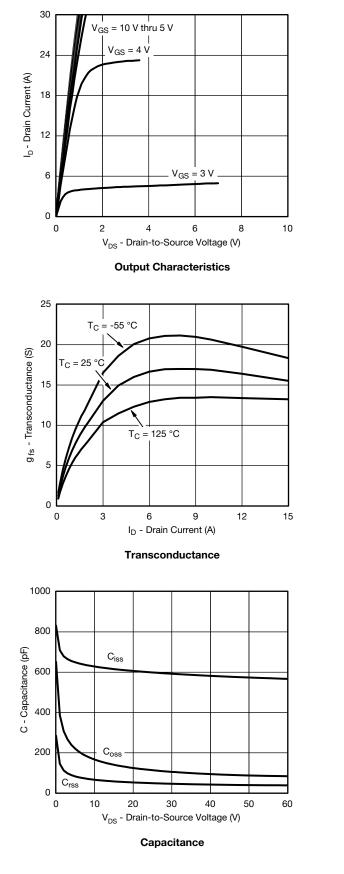
a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.

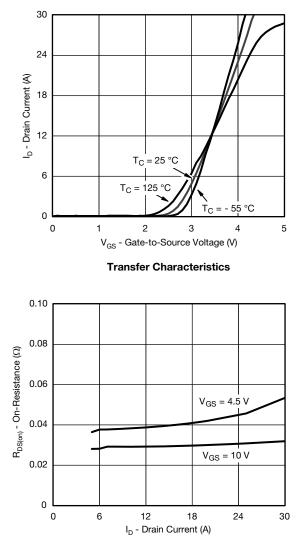
c. Independent of operating temperature.

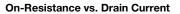
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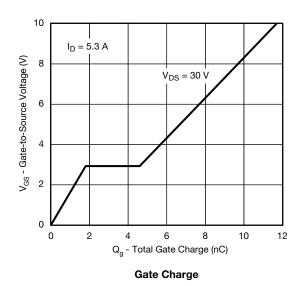


### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



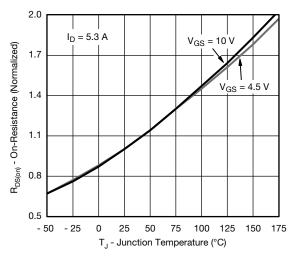




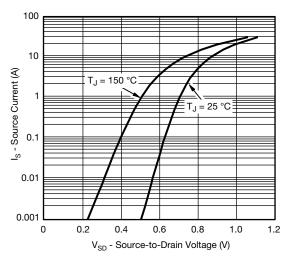




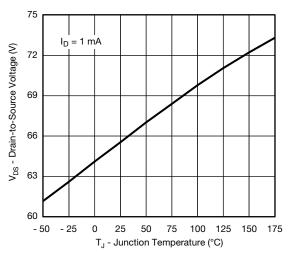
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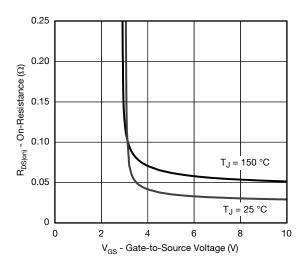
**On-Resistance vs. Junction Temperature** 



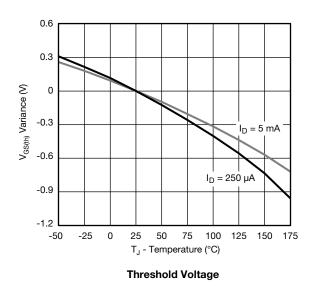
Source Drain Diode Forward Voltage



Drain Source Breakdown vs. Junction Temperature

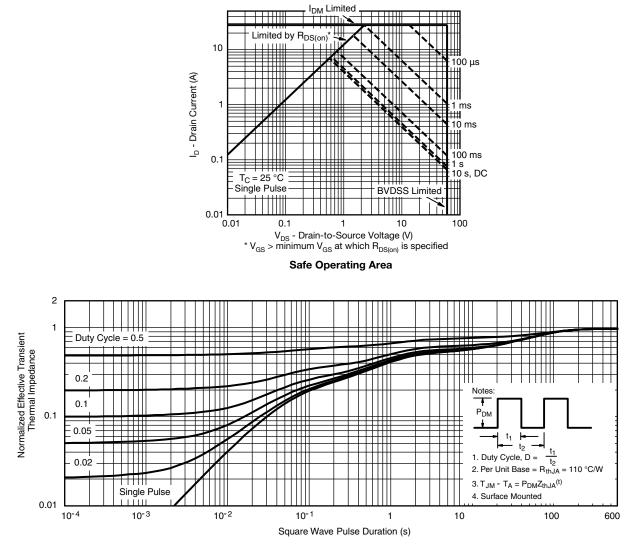


On-Resistance vs. Gate-to-Source Voltage





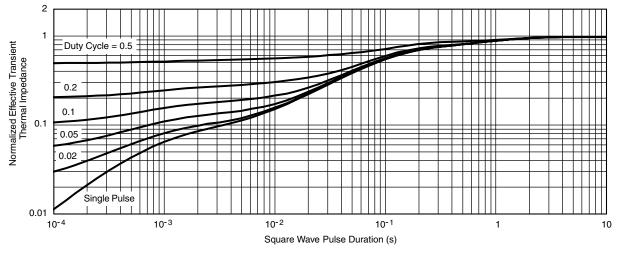
#### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



#### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

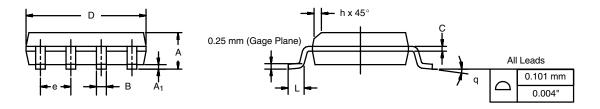


Normalized Thermal Transient Impedance, Junction-to-Foot



# SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012

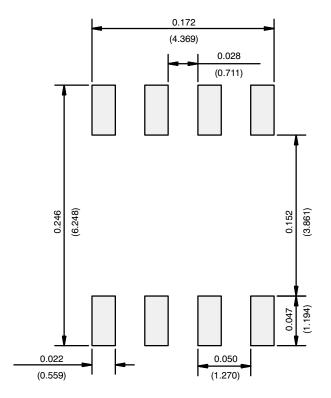




	MILLIM	IETERS	INCHES		
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					



**RECOMMENDED MINIMUM PADS FOR SO-8** 



Recommended Minimum Pads Dimensions in Inches/(mm)



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