

N-Channel 60 V (D-S) MOSFET

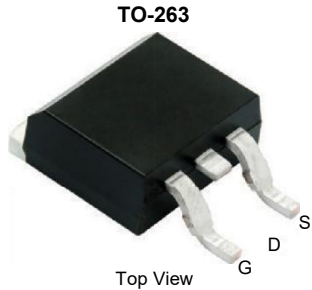
PRODUCT SUMMARY		
V_{DS}	60	V
$R_{DS(on)}$ $V_{GS} = 10$ V	4	m Ω
I_D	150	A
Configuration	Single	

FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R_g and UIS tested



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25$ °C ^a	150
		$T_C = 125$ °C	65
Continuous Source Current (Diode Conduction) ^a	I_S	120	A
Pulsed Drain Current ^b	I_{DM}	350	
Single Pulse Avalanche Current	I_{AS}	65	
Single Pulse Avalanche Energy	E_{AS}	211	mJ
Maximum Power Dissipation ^b	P_D	$T_C = 25$ °C	
		$T_C = 125$ °C	70
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	0.65	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).

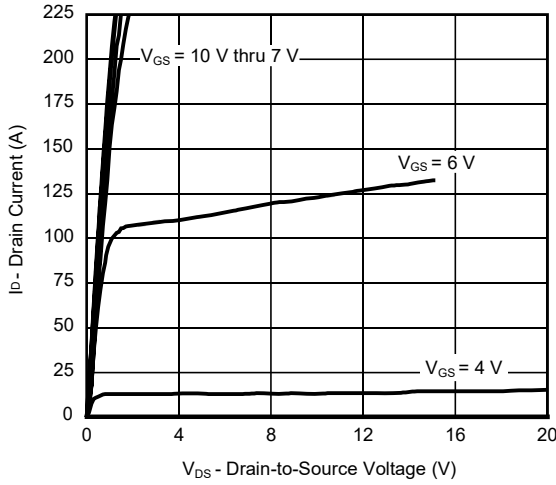
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		60	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 60 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 60 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 60 V, T _J = 175 °C	-	-	250	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	120	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A	-	6	-	mΩ
		V _{GS} = 10 V	I _D = 30 A, T _J = 125 °C	-	12	-	
		V _{GS} = 10 V	I _D = 30 A, T _J = 175 °C	-	15	-	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 30 A		-	94	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	-	7000	pF
Output Capacitance	C _{oss}			-	-	715	
Reverse Transfer Capacitance	C _{rss}			-	-	360	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 30 V, I _D = 75 A	-	96	145	nC
Gate-Source Charge	Q _{gs}			-	24	-	
Gate-Drain Charge ^c	Q _{gd}			-	27	-	
Gate Resistance	R _g	f = 1 MHz		0.3	1	1.7	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 30 V, R _L = 0.4 Ω I _D ≅ 75 A, V _{GEN} = 10 V, R _g = 1 Ω		-	16	24	ns
Rise Time ^c	t _r			-	14	21	
Turn-Off Delay Time ^c	t _{d(off)}			-	34	51	
Fall Time ^c	t _f			-	9	14	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	450	A
Forward Voltage	V _{SD}	I _F = 75 A, V _{GS} = 0		-	0.9	1.5	V

Notes

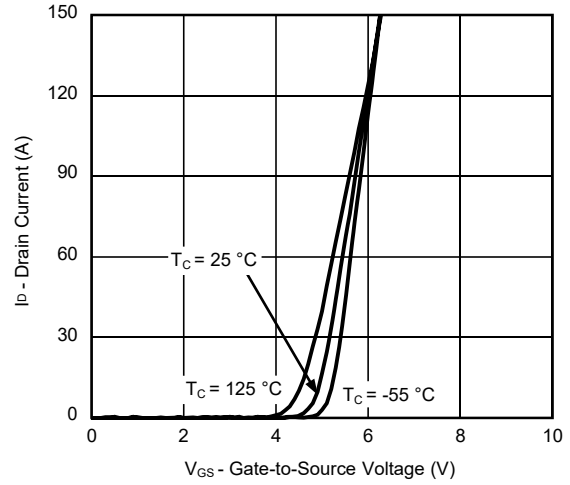
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

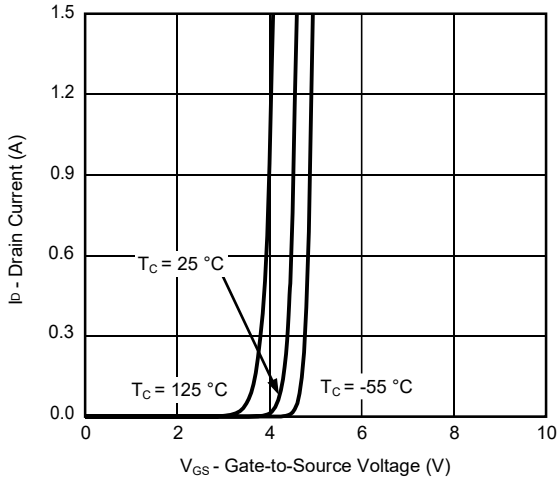
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



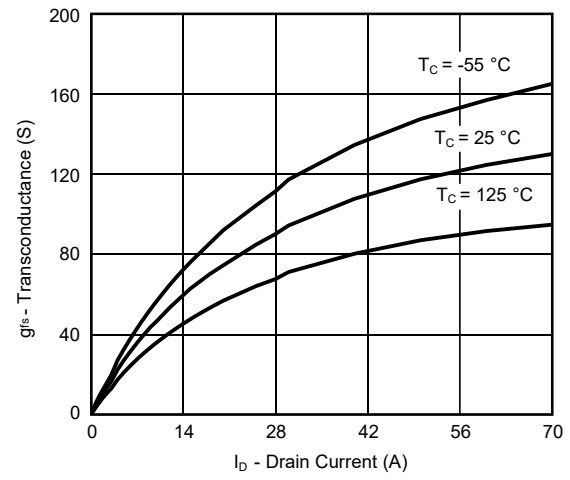
Output Characteristics



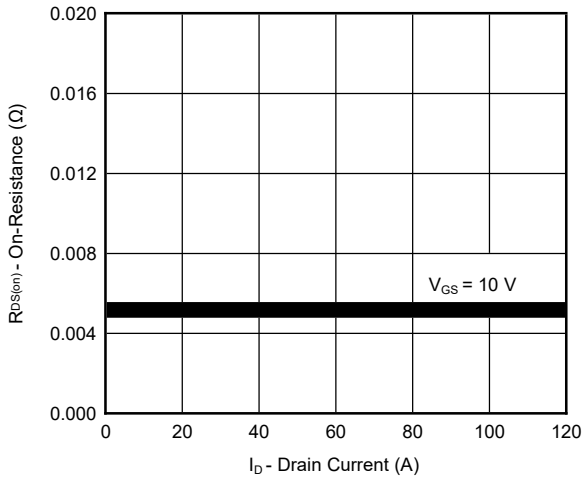
Transfer Characteristics



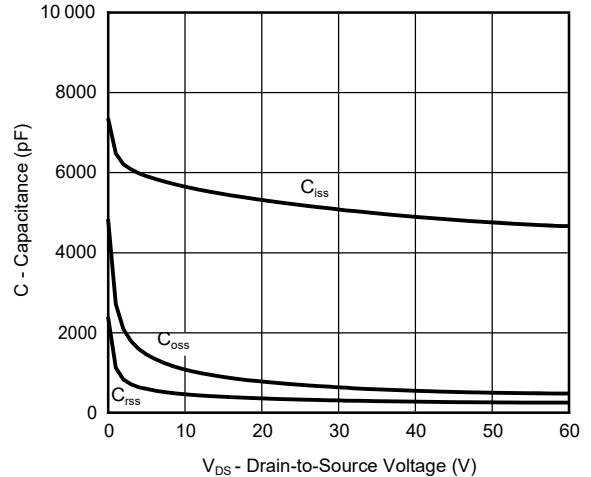
Transfer Characteristics



Transconductance



On-Resistance vs. Drain Current

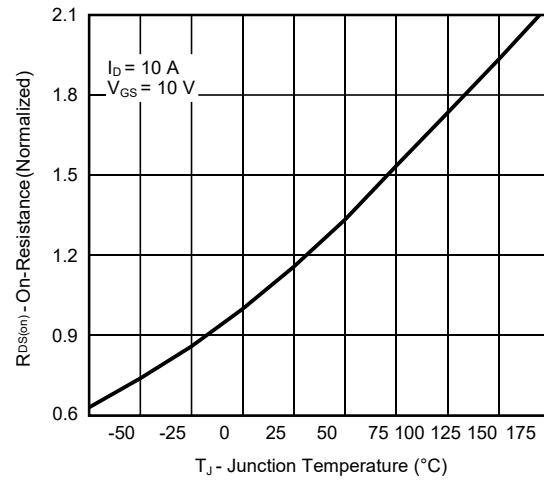


Capacitance

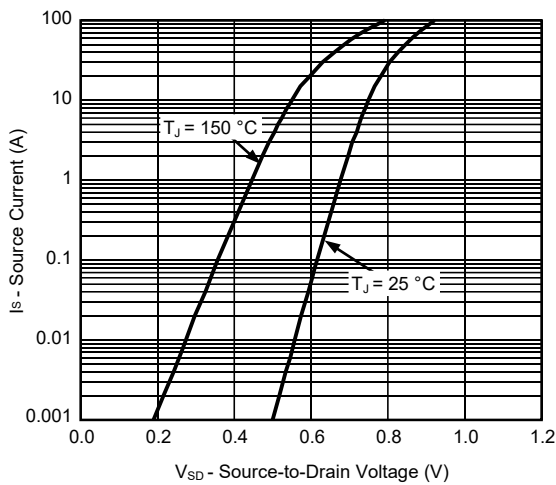
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



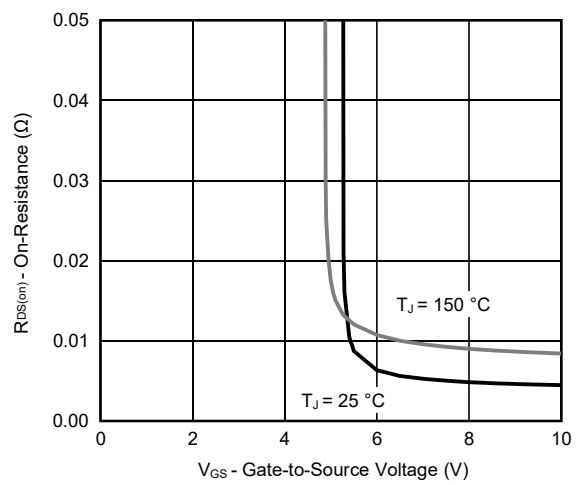
Gate Charge



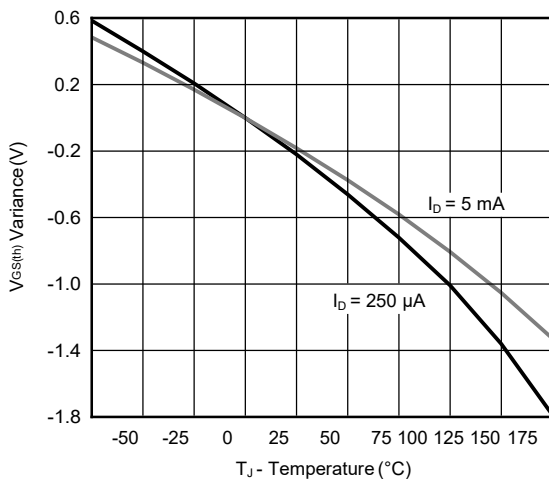
On-Resistance vs. Junction Temperature



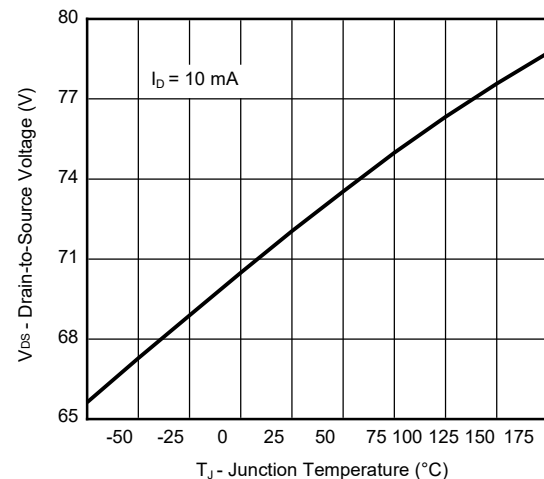
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



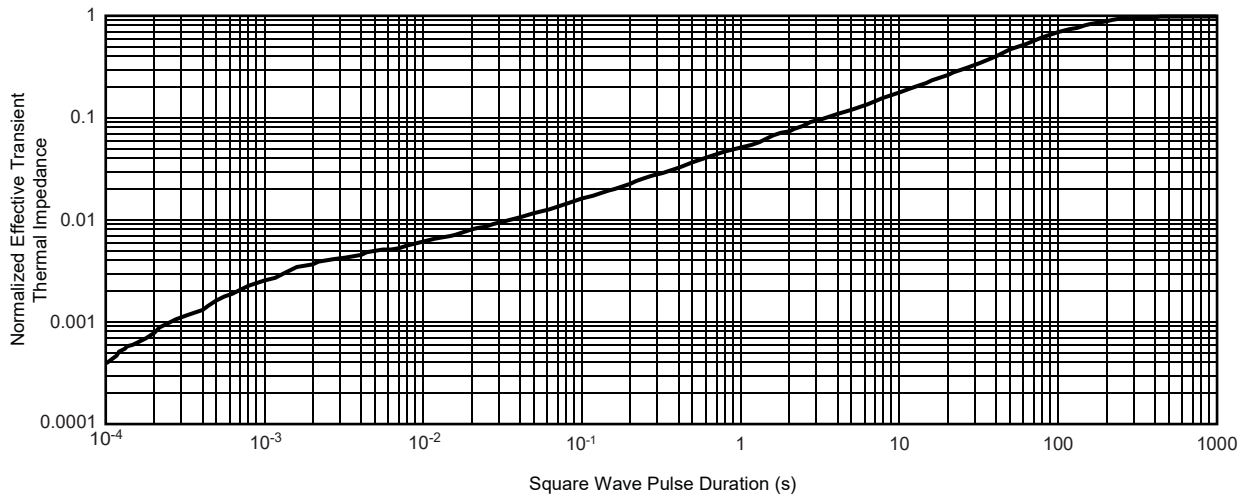
Drain Source Breakdown vs. Junction Temperature

THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



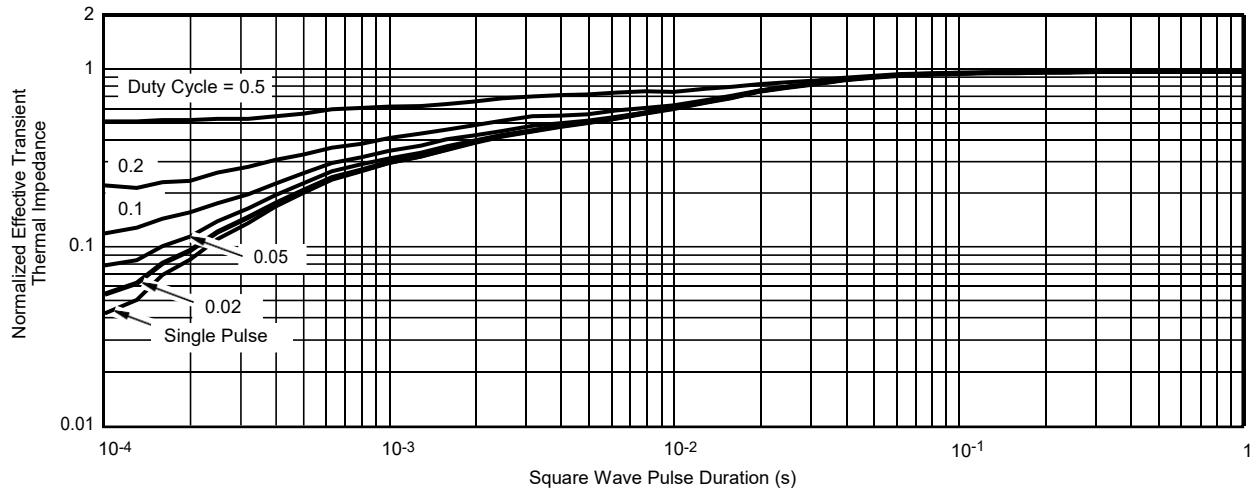
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

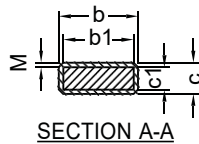
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)
- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

TO-263 (D²PAK): 3-LEAD




DETAIL A (ROTATED 90°)



DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- *: Thin lead is for SUM, SYB.
Thick lead is for SUB, SYM, SQM.
- Use inches as the primary measurement.
-  This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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