

P-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
- 100	0.160 at V _{GS} = - 10 V	- 2.5 ^c	23.2 nC
	0.200 at V _{GS} = - 4.5 V	- 2.3 ^c	

FEATURES

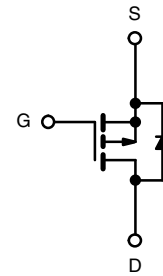
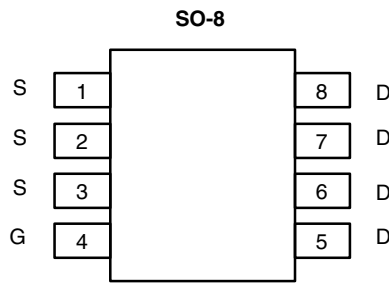
- TrenchFET[®] Power MOSFET
- 100% R_g and UIS Tested



RoHS
COMPLIANT

APPLICATIONS

- Active Clamp in Intermediate DC/DC Power Supplies
- H-Bridge High Side Switch for Lighting Application



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 2.5
		T _C = 70 °C	- 2.3
		T _A = 25 °C	- 2 ^{a, b}
		T _A = 70 °C	- 1.6 ^{a, b}
Pulsed Drain Current	I _{DM}	- 15	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	- 2.5 ^{a, b}
Avalanche Current	I _{AS}	- 15	mJ
Single-Pulse Avalanche Energy	E _{AS}	11.25	
Maximum Power Dissipation	P _D	T _C = 25 °C	5.9
		T _C = 70 °C	3.8
		T _A = 25 °C	3.1 ^{a, b}
		T _A = 70 °C	2 ^{a, b}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

Notes:

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Based on T_C = 25 °C.

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	t ≤ 10 s	R _{thJA}	33	40	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	17	21	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- Maximum under steady state conditions is 80 °C/W.

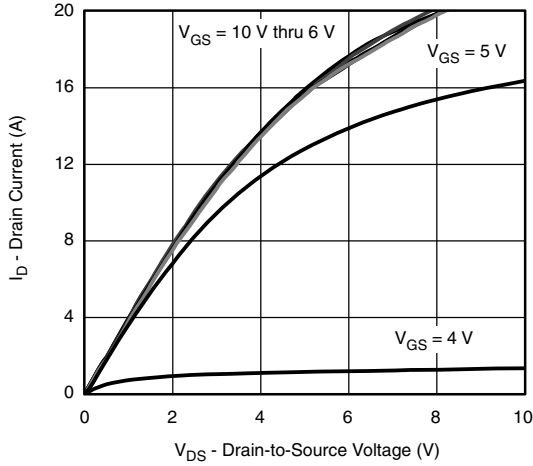
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-165		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6.6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1		-3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5\text{ V}, V_{GS} = -10\text{ V}$	-8			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -2\text{ A}$		0.160		Ω
		$V_{GS} = -4.5\text{ V}, I_D = -1.5\text{ A}$		0.200		
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = 2\text{ A}$		12		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1190		pF
Output Capacitance	C_{oss}			61		
Reverse Transfer Capacitance	C_{rss}			42		
Total Gate Charge	Q_g	$V_{DS} = -50\text{ V}, V_{GS} = -10\text{ V}, I_D = -2\text{ A}$		27.5	42	nC
				23.2	35	
Gate-Source Charge	Q_{gs}	$V_{DS} = -50\text{ V}, V_{GS} = -6\text{ V}, I_D = -2\text{ A}$		5.4		nC
Gate-Drain Charge	Q_{gd}			8.4		
Gate Resistance	R_g		$f = 1\text{ MHz}$		6.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -75\text{ V}, R_L = 25\text{ }\Omega$ $I_D \cong -3\text{ A}, V_{GEN} = -6\text{ V}, R_g = 1\text{ }\Omega$		20	30	ns
Rise Time	t_r			95	145	
Turn-Off Delay Time	$t_{d(off)}$			38	60	
Fall Time	t_f			34	51	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -75\text{ V}, R_L = 25\text{ }\Omega$ $I_D \cong -2\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		11	18	ns
Rise Time	t_r			28	42	
Turn-Off Delay Time	$t_{d(off)}$			52	78	
Fall Time	t_f			35	53	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-13	A
Pulse Diode Forward Current ^a	I_{SM}				-15	
Body Diode Voltage	V_{SD}	$I_S = -2\text{ A}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		65	90	ns
Body Diode Reverse Recovery Charge	Q_{rr}			180	270	nC
Reverse Recovery Fall Time	t_a			45		ns
Reverse Recovery Rise Time	t_b			20		

Notes:

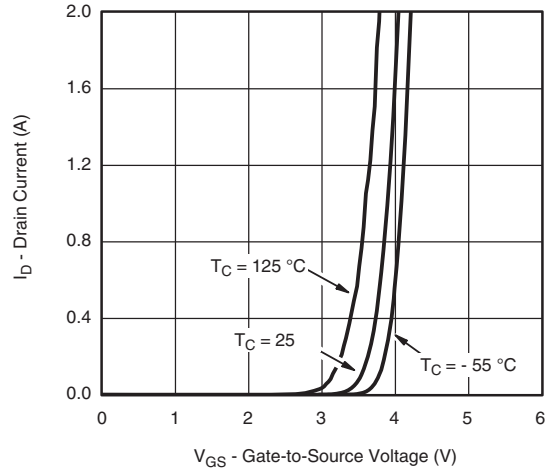
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

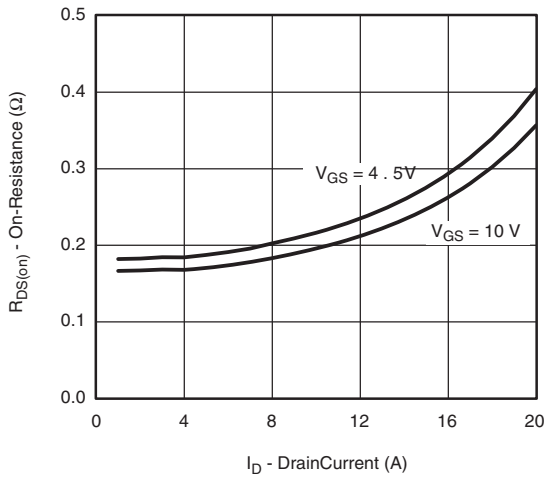
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



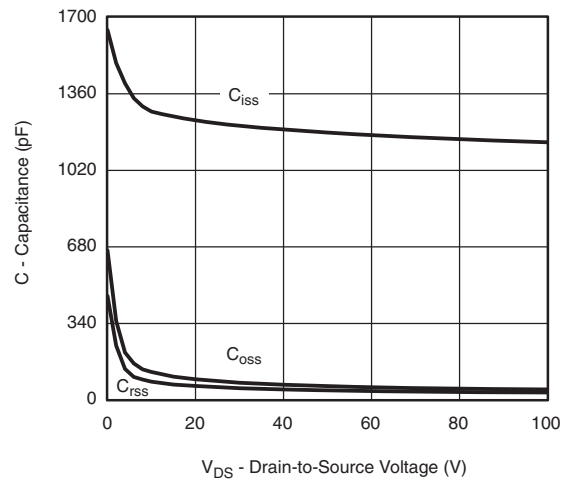
Output Characteristics



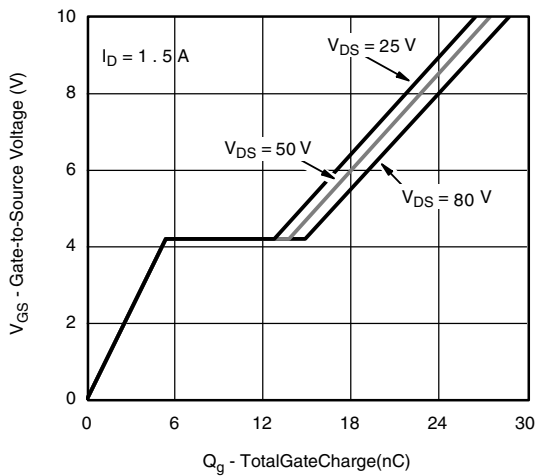
Transfer Characteristics



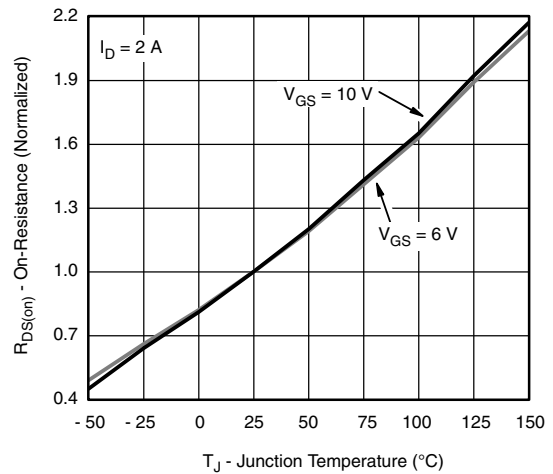
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

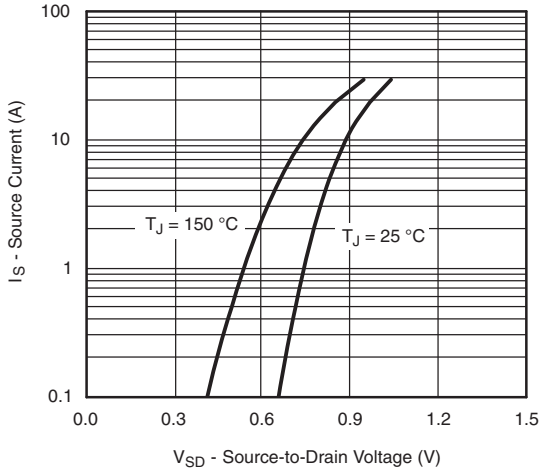


Gate Charge

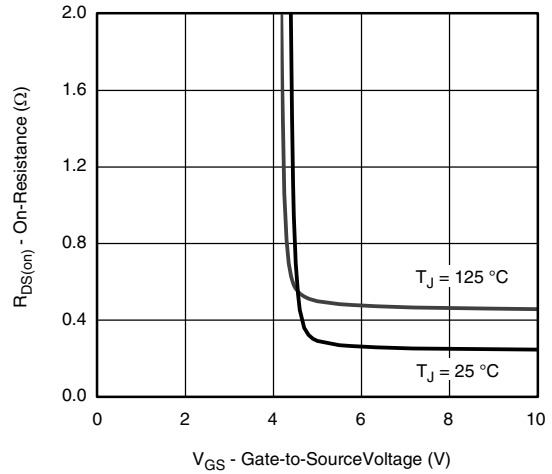


On-Resistance vs. Junction Temperature

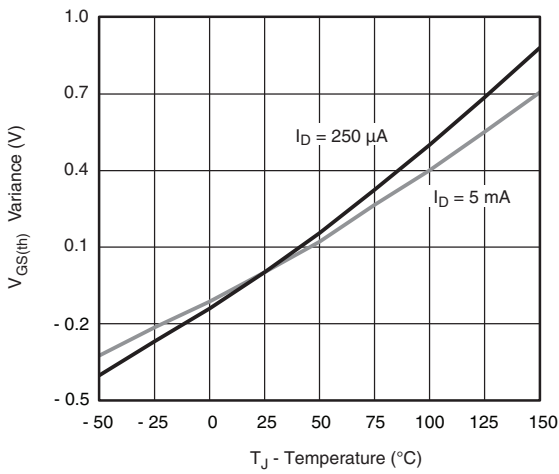
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



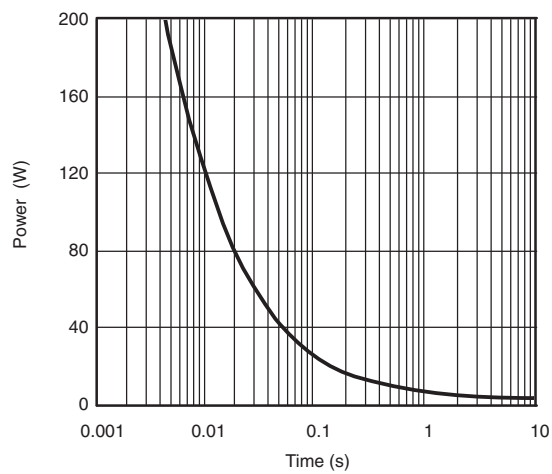
Source-Drain Diode Forward Voltage



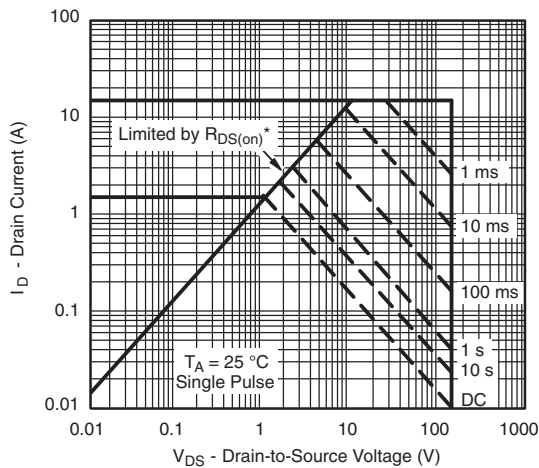
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



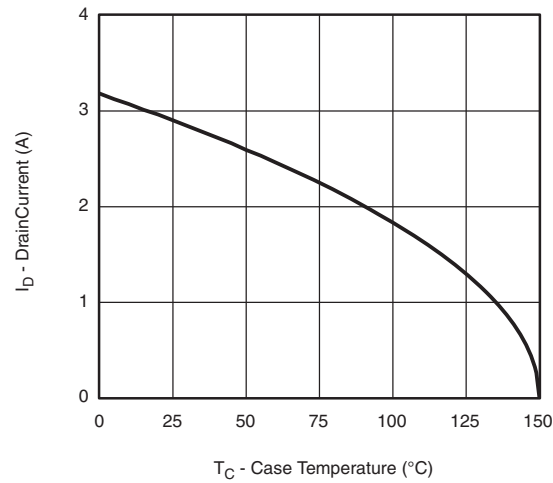
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

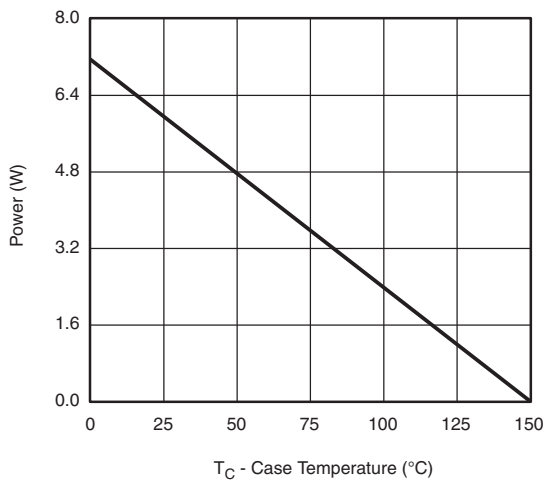
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



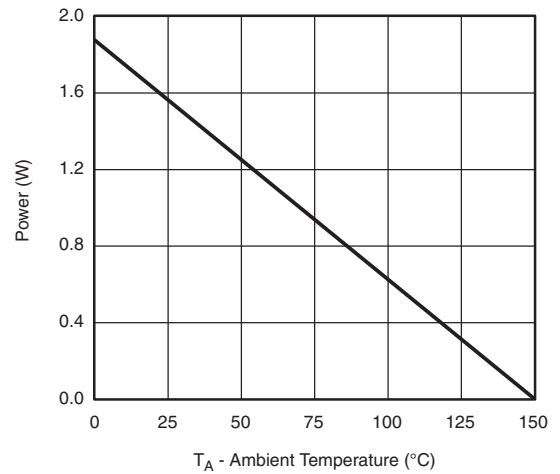
T_C - Case Temperature (°C)

Current Derating*



T_C - Case Temperature (°C)

Power, Junction-to-Foot

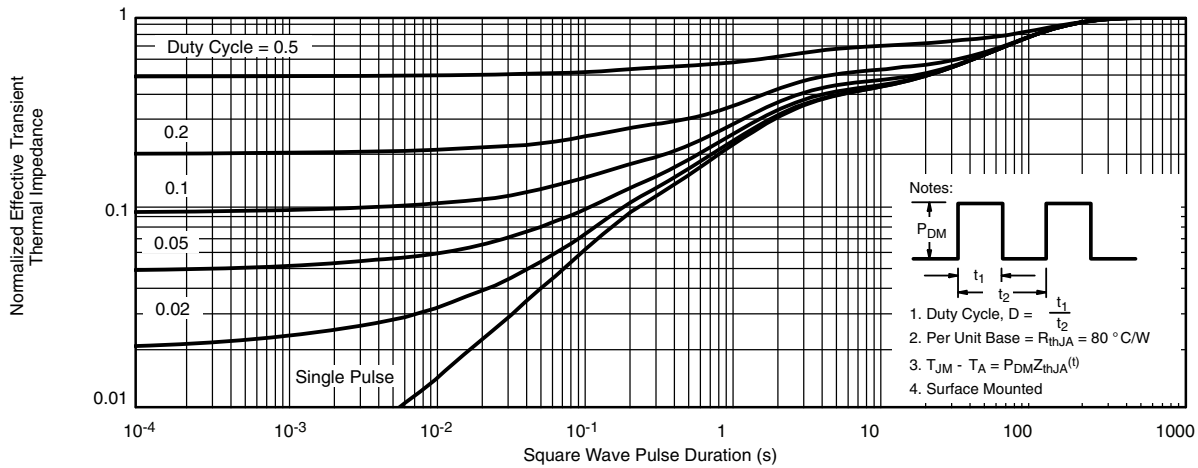


T_A - Ambient Temperature (°C)

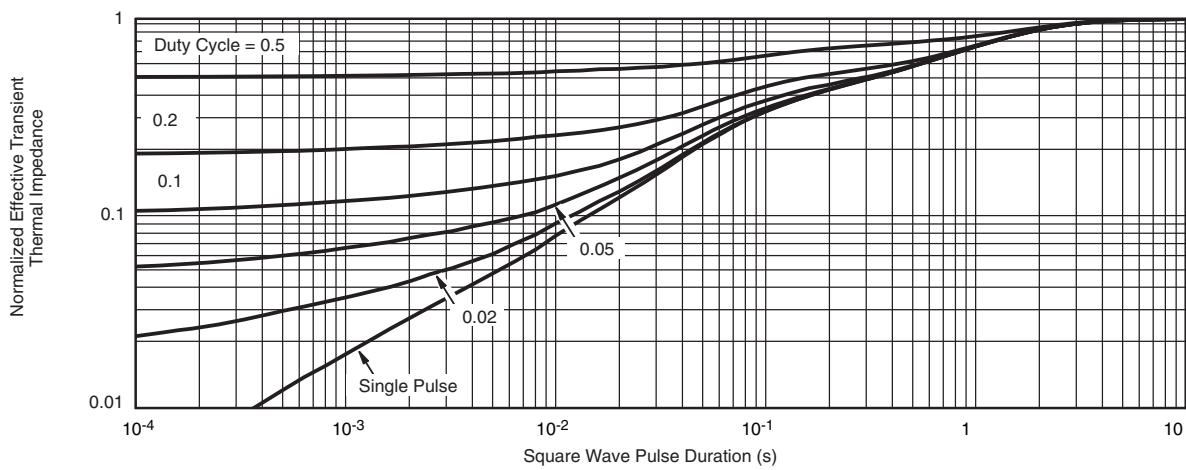
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

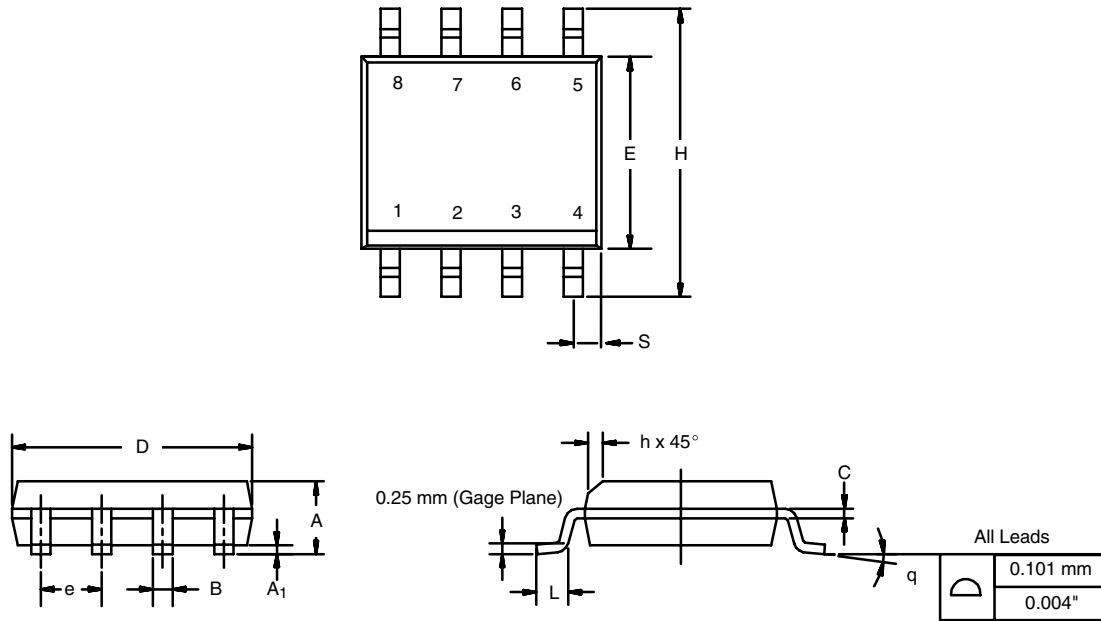


Normalized Thermal Transient Impedance, Junction-to-Ambient



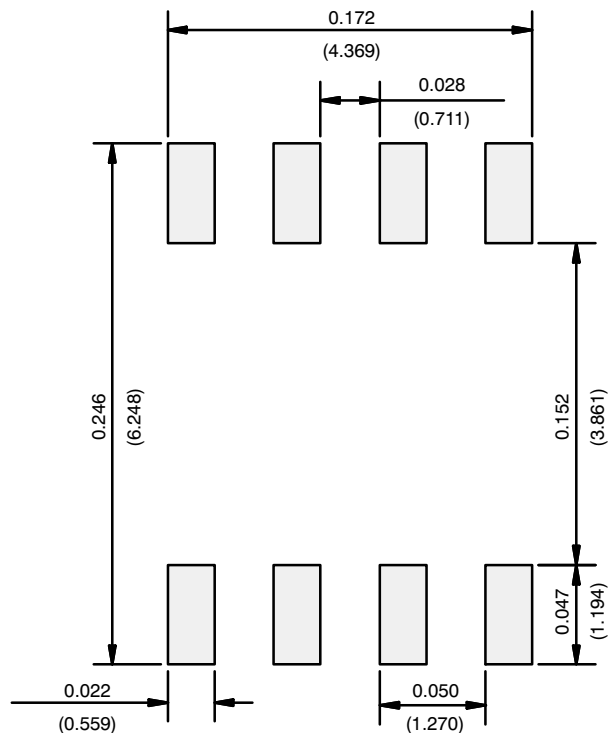
Normalized Thermal Transient Impedance, Junction-to-Foot

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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