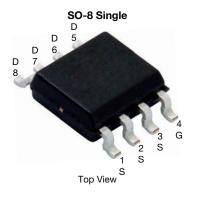
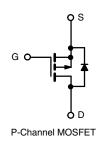
PRODUCT SUMMARY	
V _{DS} (V)	-30
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.0050
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.0080
Q _g typ. (nC)	27
I _D (A)	18





Single

FEATURES

P-Channel 30 V (D-S) MOSFET

- TrenchFET[®] Gen IV p-channel power MOSFET
- · Enables higher power density
- 100 % R_q and UIS tested



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APPLICATIONS

- Battery management in mobile devices
- Adapter and charger switch
- · Battery switch
- · Load switch

ABSOLUTE MAXIMUM RATING	3S (Τ _A = 25 °C, ι	inless otherw	ise noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	-30	V	
Gate-source voltage		V _{GS}	± 20	v	
	T _C = 25 °C		-18		
Continuous drain ourrent (T 150 °C)	T _C = 70 °C	1 , Г	-13		
Continuous drain current ($T_J = 150 \ ^\circ C$)	T _A = 25 °C		-11		
	T _A = 70 °C	T F	-8	Α	
Pulsed drain current (t = 100 μs)		I _{DM}	-145	A	
Continuous source drain diada aurrent	T _C = 25 °C		-5		
Continuous source-drain diode current	T _A = 25 °C	I _S	-2.8 ^{b, c}		
Single pulse avalanche current L = 0.1 mH		I _{AS}	-25		
		E _{AS}	31.2	mJ	
Maximum power dissipation	T _C = 25 °C		5.6		
	T _C = 70 °C	1 , Г	3.6	w	
	T _A = 25 °C	l _P	3.1 ^{b, c}	vv	
	T _A = 70 °C	1 [2 ^{b, c}		
Operating junction and storage temperature range		TJ, T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^c			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient b	t ≤ 10 s	R _{thJA}	34	40	°C/W		
Maximum junction-to-case (drain)	Steady state	R _{thJF}	18	22	-C/W		

Notes

Notes
a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. The SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
a. Powerk conditions: manufacturing is not required to ensure a componente.

Rework conditions: manual soldering with a soldering iron is not recommended for leadless components Maximum under steady state conditions is 85 °C/W e. f.

g. T_C = 25 °C

Configuration

$\begin{array}{ c c c c c } \hline Static & & & & & & & & & & & & & & & & & & &$	SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
$\begin{array}{ c c c c c c } \hline Drain-source breakdown voltage & V_{DS} & V_{GS} = 0 V, I_D = -250 \ \mu A & - & - & - & - & - & - & - & - & - &$	PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
	Static							
$ \begin{array}{ c c c c c } \hline V_{GS(th)} temperature coefficient & AV_{GS(th)} & I_D = -250 \mu A & - & 5.5 & - & I \\ \hline Gate-source threshold voltage & V_{GS(th)} & V_{DS} = V_{GS, I_D} = 250 \mu A & -1 & - & -2.2 \\ \hline Gate-source leakage & I_{GSS} & V_{DS} = 0 V, V_{GS} = +16 / -20 V & - & - & - & 100 \\ \hline Carce gate voltage drain current & I_{DSS} & V_{DS} = 0 V, V_{GS} = 0 V & - & - & - & -15 \\ \hline On-state drain current ^a & I_{D(sn)} & V_{DS} = -30 V, V_{GS} = 0 V & - & - & - & -5 \\ \hline On-state drain current ^a & I_{D(sn)} & V_{DS} = -10 V, V_{DS} = -10 V & -40 & - & - & - \\ \hline Organ - source on-state resistance ^a & P_{DS(on)} & V_{DS} = -10 V, I_D = -15 A & - & 0.0050 & - \\ \hline V_{OS} = -4.5 V, I_D = -10 A & - & 0.0080 & - & \\ \hline V_{OS} = -4.5 V, I_D = -10 A & - & 0.0080 & - & \\ \hline V_{DS} = -15 V, V_{GS} = 0 V, f = 1 \text{MHz} & - & 1420 & - \\ \hline Dupamic ^b & & & & & & \\ \hline Dupta capacitance & C_{ras} & & & & & & & \\ \hline Dupt capacitance & C_{ras} & & & & & & & \\ \hline Total gate charge & Q_{g} & & & & & & & & \\ \hline Total gate charge & Q_{gd} & & & & & & & & \\ \hline Cate resistance & R_{g} & f = 1 \text{MHz} & 1.5 & 3.5 & 6 & \\ \hline Tum-onf delay time & t_{r} & & & \\ \hline Tum-onf delay time & t_{r} & & & \\ \hline Fall time & t_{r} & & & & \\ \hline Tum-onf delay time & t_{d(onf)} & & & & & \\ \hline Fall time & t_{r} & & & & \\ \hline Tum-onf delay time & t_{d(onf)} & & & & & \\ \hline Fall time & t_{r} & & & & & \\ \hline Tum-onf delay time & t_{d(onf)} & & & & & & \\ \hline Fall time & t_{r} & & & & & & \\ \hline Tum-onf delay time & t_{d(onf)} & & & & & & & & \\ \hline Fall time & t_{r} & & & & & & & & & & & & & & \\ \hline Tum-onf delay time & t_{d(onf)} & & & & & & & & & & & & & & & & & & &$	Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-30	-	-	V	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	V _{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I _D = -10 mA	-	-17	-		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	5.5	-	mV/°C	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	-1	-	-2.2	V	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Gate-source leakage		$V_{DS} = 0 V, V_{GS} = +16 / -20 V$	-	-	100	nA	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Zara gata valtaga drain aurrant	1	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	zero gate voltage drain current	IDSS	V_{DS} = -30 V, V_{GS} = 0 V, T_{J} = 70 °C	-	-	-15	μA	
$ \begin{array}{ c c c c c } \hline Prain-source on-state resistance a } \\ \hline Probability Prain Product on the state resistance a } \\ \hline Provem d transconductance a & g_{fs} & V_{DS} = -15 V, I_{D} = -10 A & - & 0.0080 & - & & 0.0080 & - & 0.0080 & - & & 0.0080 & - & 0.$	On-state drain current ^a	I _{D(on)}	$V_{DS} \ge$ -10 V, V_{GS} = -10 V	-40	-	-	А	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Drain acurac on state registeres à		V _{GS} = -10 V, I _D = -15 A	-	0.0050	-	-	
$\begin{tabular}{ c c c c c c } \hline $\mathbf{Dynamic}$ \mathbf{b} \\ \hline $Input capacitance & C_{iss} \\ \hline $Output capacitance & C_{oss} \\ \hline $Output capacitance & C_{rss} \\ \hline $V_{DS} = -15 $ V, $V_{GS} = 0 $ V, $f = 1 $ MHz \\ \hline $-$ $1420 $ $-$ \\ \hline $1420 $ $-$ \\ \hline $-$ $70 $ $-$ $-$ $70 $ $-$ \\ \hline $-$ $70 $ $-$ $70 $ $-$ \\ \hline $-$ $70 $ $-$ $70 $ $-$ \\ \hline $-$ $70 $ $-$ $70 $ $-$ $70 $ $-$ $70 $ $-$ $70 $ $-$ $70 $ $-$ $70 $-$ $70 $ $-$ $70 $ $-$ $70 $ $-$ $70 $-$ $70 $ $-$$	Drain-source on-state resistance "	RDS(on)	$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -10 \text{ A}$	-	0.0080	-	Ω	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Forward transconductance ^a	9 _{fs}	V _{DS} = -15 V, I _D = -15 A	-	81	-	S	
$ \begin{array}{ c c c c c c } \hline \mbox{UDS} & V_{DS} = -15 \ V, \ V_{GS} = 0 \ V, \ f = 1 \ MHz & - & 1420 & - & \\ \hline \mbox{Reverse transfer capacitance} & C_{rss} & & & \\ \hline \mbox{Posser transfer capacitance} & C_{rss} & & & \\ \hline \mbox{Reverse transfer capacitance} & Q_g & & & & \\ \hline \mbox{VDS} = -15 \ V, \ V_{GS} = -10 \ V, \ I_D = -10 \ A & - & 56 & 84 & \\ \hline \mbox{Reverse charge} & Q_{gs} & & & & \\ \hline \mbox{Qg} & & & & & \\ \hline \mbox{Gate-drain charge} & Q_{gd} & & & & & \\ \hline \mbox{Gate resistance} & R_g & f = 1 \ MHz & & 1.5 & 3.5 & 6 & \\ \hline \mbox{Turn-on delay time} & t_{d(on)} & & & & \\ \hline \mbox{Rise time} & t_r & & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & & \\ \hline \mbox{Rise time} & t_r & & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & \\ \hline \mbox{Rise time} & t_r & & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & \\ \hline \mbox{Turn-on delay time} & t_r & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & \\ \hline \mbox{Turn-on delay time} & t_r & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & \\ \hline \mbox{Turn-on delay time} & t_{d(onf)} & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & t_r & & \\ \hline \mbox{Turn-on fleap time} & &$	Dynamic ^b							
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Input capacitance	C _{iss}		-	3490	-		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Output capacitance	C _{oss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	-	1420	-	pF	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Reverse transfer capacitance	C _{rss}		-	70	-		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Total acto charge	0	$V_{DS} = -15 \text{ V}, \text{ V}_{GS} = -10 \text{ V}, \text{ I}_{D} = -10 \text{ A}$	-	56	84		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Total gate charge	Qg		-	27	41	nC	
$ \begin{array}{ c c c c c c } \hline Gate resistance & R_g & f = 1 \ MHz & 1.5 & 3.5 & 6 \\ \hline Turn-on \ delay \ time & t_{d(on)} & & & & & & & & & & & & & & & & & & &$	Gate-source charge	Q _{gs}	V_{DS} = -15 V, V_{GS} = -4.5 V, I_{D} =-10 A	-	9.4	-		
$ \begin{array}{ c c c c c c c } \hline Turn-on \ delay \ time & t_{d(on)} & & & & t_{d(on)} & & & & & t_{d(on)} & & & & & & & & & & & & & & & & & & &$	Gate-drain charge	Q _{gd}		-	8.2	-		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Gate resistance	R _g	f = 1 MHz	1.5	3.5	6	Ω	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Turn-on delay time	t _{d(on)}		-	15	30		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Rise time	t _r	V_{DD} = -15 V, R_L = 1.5 Ω , $I_D \cong$ -10 A,	-	6	12		
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Turn-off delay time	t _{d(off)}	V_{GEN} = -10 V, R_g = 1 Ω	-	39	78		
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Fall time	t _f		-	10	20		
$\begin{tabular}{ c c c c c } \hline Turn-off delay time & $t_{d(off)}$ & $V_{GEN} = -4.5 $ V, $R_g = 1 $ \Omega$ & $-$ & 31 & 62 \\ \hline Fall time & t_f & $-$ & 22 & 44 \\ \hline \end{tabular}$	Turn-on delay time	t _{d(on)}		-	34	68	ns	
Fall time t_f -2244Drain-Source Body Diode CharacteristicsContinuous source-drain diode current I_S $T_C = 25 ^{\circ}C$ 5Pulse diode forward current I_{SM} 150	Rise time	t _r		-	86	172		
Drain-Source Body Diode CharacteristicsContinuous source-drain diode current I_S $T_C = 25 \ ^{\circ}C$ $ -5$ Pulse diode forward current I_{SM} $ -150$	Turn-off delay time	t _{d(off)}	V_{GEN} = -4.5 V, R_g = 1 Ω	-	31	62		
Continuous source-drain diode currentIs $T_C = 25 \ ^{\circ}C$ 5Pulse diode forward currentIsm150	Fall time	t _f		-	22	44		
Pulse diode forward current I _{SM} 150	Drain-Source Body Diode Characteristics							
	Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-5	^	
Body diode voltage V _{SD} I _S = -5 A, V _{GS} = 0 V - -0.73 -1.1	Pulse diode forward current	I _{SM}		-	-	-150	A	
	Body diode voltage	V _{SD}	I _S = -5 A, V _{GS} = 0 V	-	-0.73	-1.1	V	
Body diode reverse recovery time t _{rr} - 44 88	Body diode reverse recovery time	t _{rr}		-	44	88	ns	
Body diode reverse recovery charge Q _{rr} + to the life too to the too to the second se	Body diode reverse recovery charge	Q _{rr}		-	41	82	nC	
Reverse recovery fall time t_a $I_F = -10 \text{ A}$, di/dt = 100 A/µs, $T_J = 25 \text{ °C}$ -19-	Reverse recovery fall time	t _a	$I_F = -10$ A, di/dt = 100 A/µs, $I_J = 25$ °C	-	19	-		
Reverse recovery rise time t _b - 25 -	Reverse recovery rise time			-	25	-	ns	

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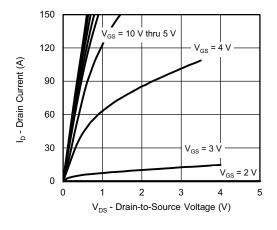
Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$

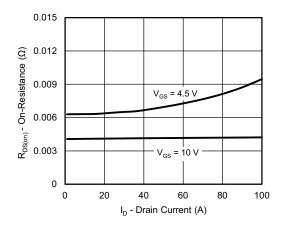
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

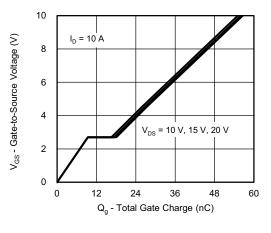




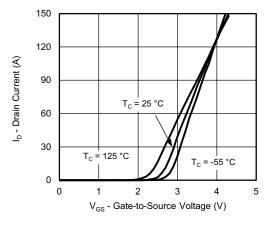
Output Characteristics



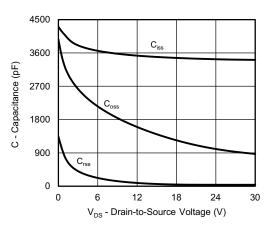
On-Resistance vs. Drain Current and Gate Voltage



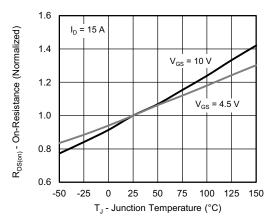
Gate Charge



Transfer Characteristics

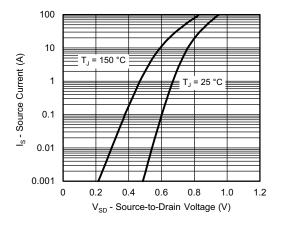


Capacitance

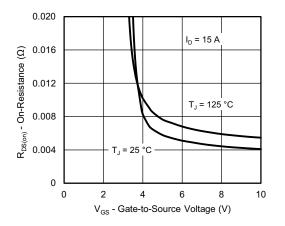


On-Resistance vs. Junction Temperature

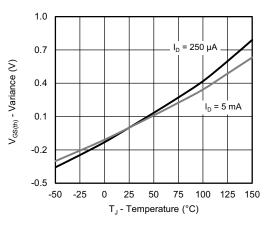




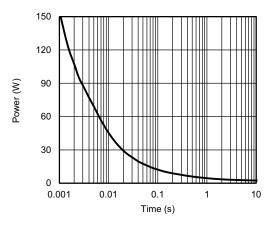
Source-Drain Diode Forward Voltage



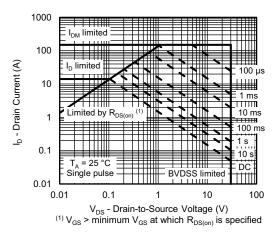
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

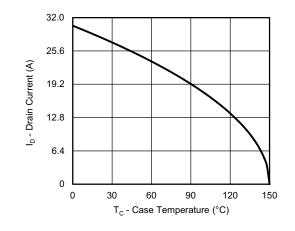


Single Pulse Power, Junction-to-Ambient

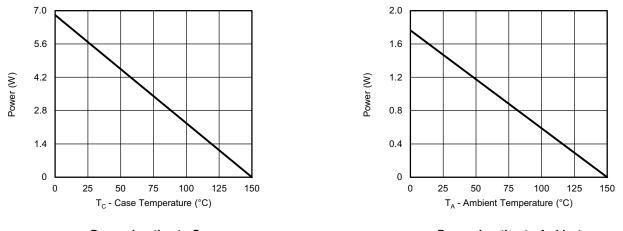


Safe Operating Area, Junction-to-Ambient





Current Derating ^a



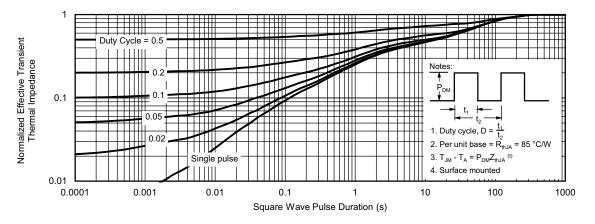
Power, Junction-to-Case

Power, Junction-to-Ambient

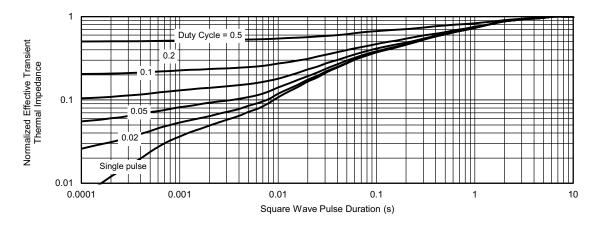
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient

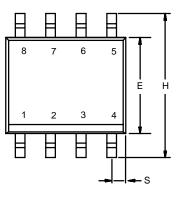


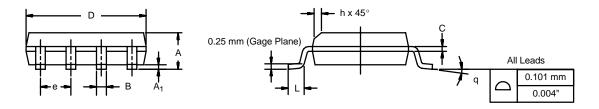
Normalized Thermal Transient Impedance, Junction-to-Case





SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012

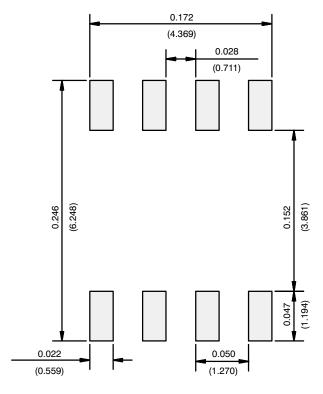




	MILLIN	IETERS	INCHES		
DIM	Min	Max	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



Disclaimer

All products due to improve reliability, function or design or for other reasons, product specifications and data are subject to change without notice.

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