

## Power MOSFET

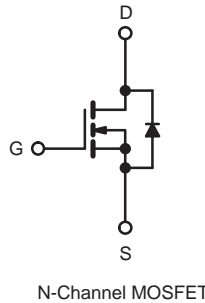
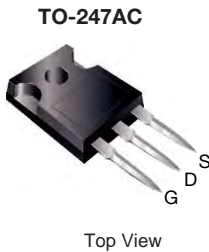
PRODUCT SUMMARY		
$V_{DS}$ (V)	200	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.056
$Q_g$ (Max.) (nC)	70	
$Q_{gs}$ (nC)	13	
$Q_{gd}$ (nC)	39	
Configuration	Single	

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Low-Profile Through-Hole
- Available in Tape and Reel
- Dynamic  $dV/dt$  Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**  
Available



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	200	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	20
			$T_C = 100\text{ }^\circ\text{C}$	13
Pulsed Drain Current <sup>a, e</sup>		$I_{DM}$	72	A
Linear Derating Factor			1.0	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b, e</sup>		$E_{AS}$	580	mJ
Avalanche Current <sup>a</sup>		$I_{AR}$	20	A
Repetitive Avalanche Energy <sup>a</sup>		$E_{AR}$	13	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$ $T_A = 25\text{ }^\circ\text{C}$	$P_D$	3.1	W
			130	
Peak Diode Recovery $dV/dt$ <sup>c, e</sup>		$dV/dt$	5.0	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)		for 10 s	300 <sup>d</sup>	

### Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 2.7\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 18\text{ A}$  (see fig. 12).
- $I_{SD} \leq 20\text{ A}$ ,  $dI/dt \leq 150\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, Steady-State) <sup>a</sup>	R <sub>thJA</sub>	-	40	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	1.0	

**Note**

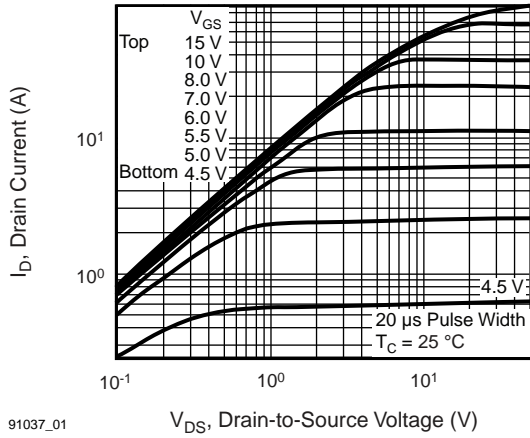
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		200	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA <sup>c</sup>		-	0.29	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 11 A <sup>b</sup>	-	0.09	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 11 A <sup>d</sup>		6.7	-	-	S
<b>Dynamic</b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5 <sup>d</sup>		-	1300	-	pF
Output Capacitance	C <sub>oss</sub>			-	430	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	130	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, V <sub>DS</sub> = 160 V, see fig. 6 and 13 <sup>b, c</sup>	-	-	70	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	13	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	39	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 20 A, R <sub>g</sub> = 9.1 Ω, R <sub>D</sub> = 5.4 Ω, see fig. 10 <sup>b, c</sup>		-	14	-	ns
Rise Time	t <sub>r</sub>			-	51	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	45	-	
Fall Time	t <sub>f</sub>			-	36	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	20	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	72	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 20 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.0	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 20 A, di/dt = 100 A/μs <sup>b, c</sup>		-	300	610	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	3.4	7.1	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

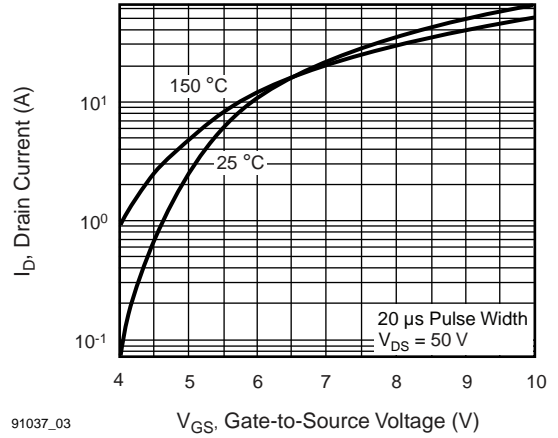
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- c. Uses IRF640/SiHF640 data and test conditions.

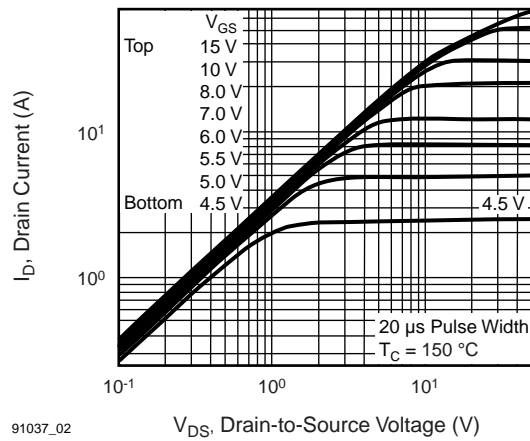
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



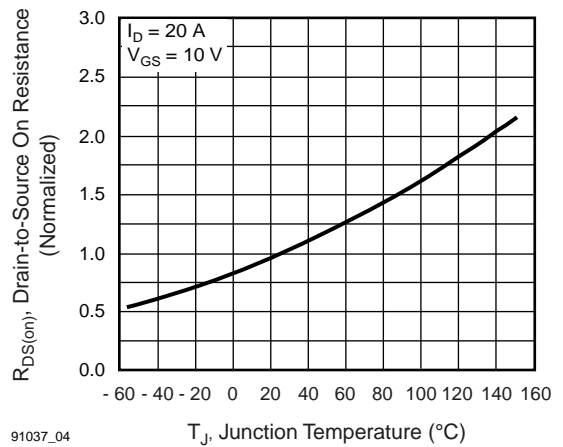
**Fig. 1 - Typical Output Characteristics,  $T_J = 25\text{ °C}$**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics,  $T_J = 175\text{ °C}$**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

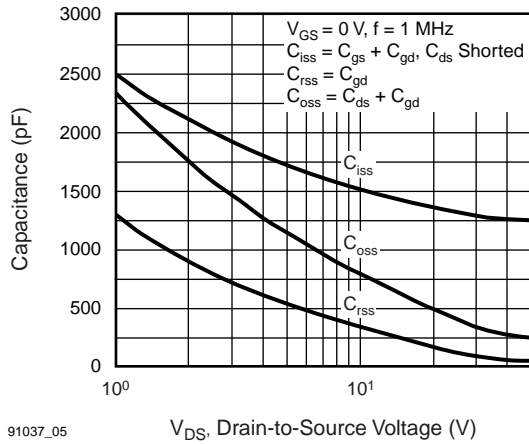


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

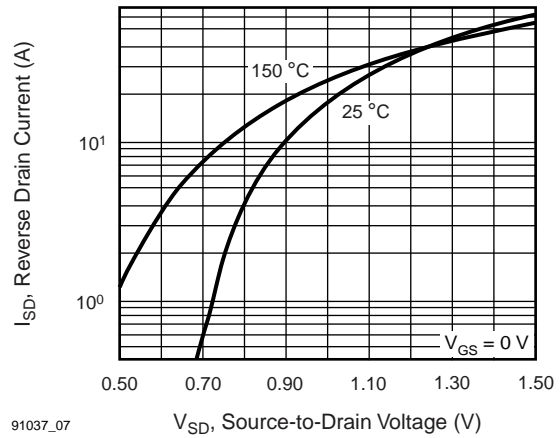


Fig. 7 - Typical Source-Drain Diode Forward Voltage

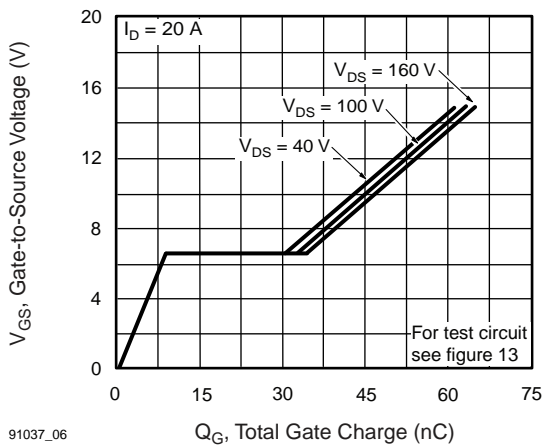


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

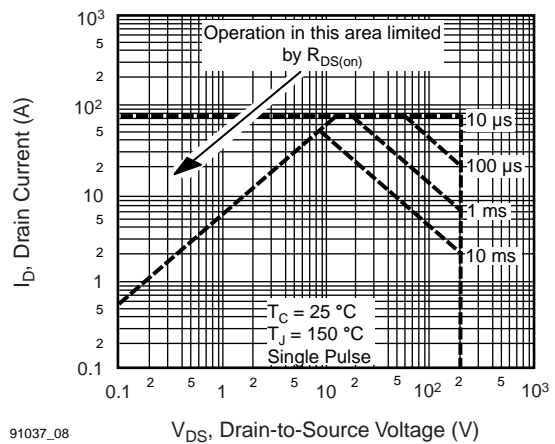


Fig. 8 - Maximum Safe Operating Area

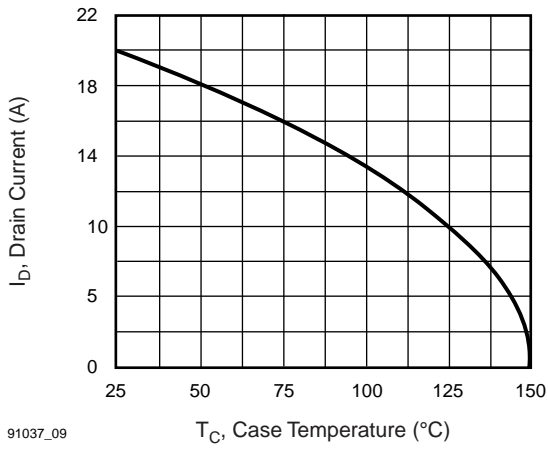


Fig. 9 - Maximum Drain Current vs. Case Temperature

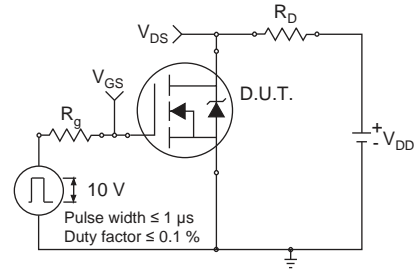


Fig. 10a - Switching Time Test Circuit

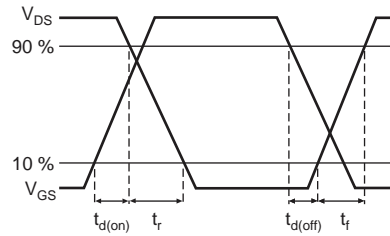


Fig. 10b - Switching Time Waveforms

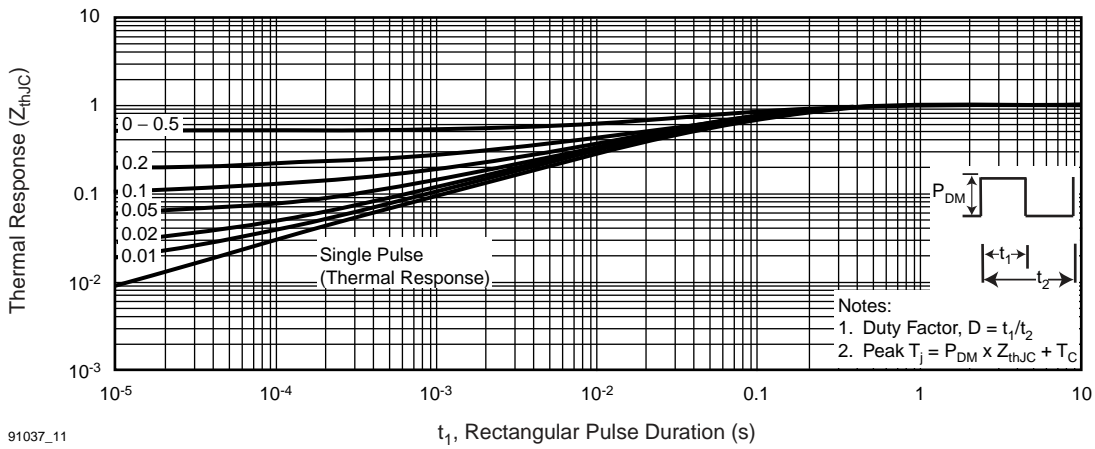


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

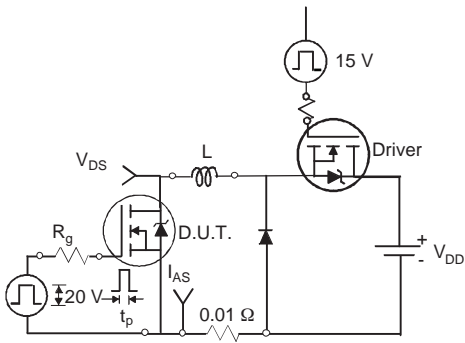
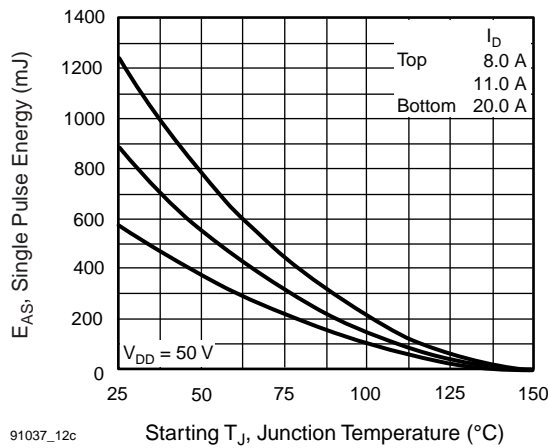


Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms



91037\_12c

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

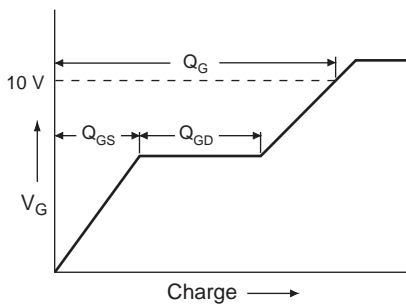


Fig. 13a - Basic Gate Charge Waveform

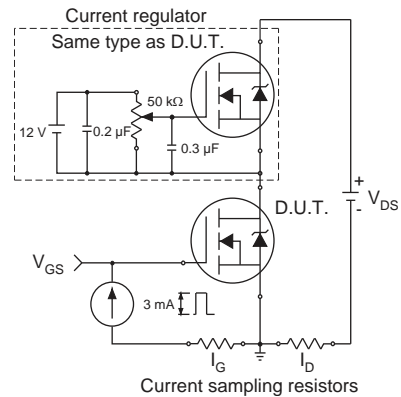
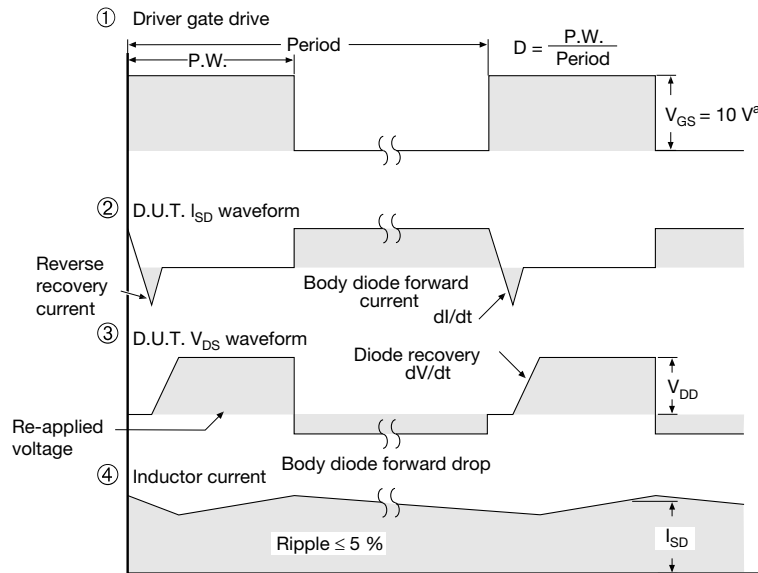


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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