

## N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A) <sup>d</sup>	Q <sub>g</sub> (Typ.)			
40	0.014 at V <sub>GS</sub> = 10 V	10	15 nC			
40	0.016 at V <sub>GS</sub> = 4.5 V	9	13110			

# SO-8 S 1 S 2 G 4 Top View

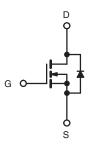
#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested
- Compliant to RoHS directive 2002/95/EC



#### **APPLICATIONS**

- Synchronous Rectification
- POL, IBC
  - Secondary Side



N-Channel MOSFET

Parameter	Symbol	mbol Limit			
Drain-Source Voltage	V <sub>DS</sub>	40			
Gate-Source Voltage		V <sub>GS</sub>	± 20	V	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	I <sub>D</sub>	10 9 9 <sup>a, b</sup> 8 <sup>a, b</sup>	Α	
Pulsed Drain Current  Avalanche Current		I <sub>DM</sub>	50 15		
Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	11	mJ	
Continuous Source-Drain Diode Current	$T_C = 25 ^{\circ}C$ $T_A = 25 ^{\circ}C$	I <sub>S</sub>	5 2.1 <sup>a, b</sup>	Α	
Maximum Power Dissipation	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{\Delta} = 70 ^{\circ}\text{C}$	P <sub>D</sub>	6 3.8 2.5 <sup>a, b</sup> 1.6 <sup>a, b</sup>	w	
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stq</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>a, c</sup>	t ≤ 10 s	$R_{thJA}$	37	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	17	21	C/ VV		

#### Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. Maximum under Steady State conditions is 85 °C/W.
- d. Based on  $T_C = 25$  °C.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static					l	
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V, } I_D = 250  \mu\text{A}$	40			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J I <sub>D</sub> = 250 μA		40		m\//°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 6		mV/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	1		3	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zara Cata Valtaga Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μΑ
Zero Gate Voltage Drain Current		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	50			Α
Drain Course On State Registered	D	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12.4 A	0.014 0.016			0
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 10.8 \text{ A}$				Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 12.4 A		56		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>			2000		pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		260		
Reverse Transfer Capacitance	C <sub>rss</sub>			150		
Total Gate Charge		$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 12.4 \text{ A}$		15		nC
	Q <sub>g</sub>			13		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 12.4 \text{ A}$		6.7		
Gate-Drain Charge	$Q_{gd}$			5.1		
Gate Resistance	$R_g$	f = 1 MHz		1.4	2.1	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			25	40	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 20 V, $R_L$ = 2 $\Omega$		12	20	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		25	40	
Fall Time	t <sub>f</sub>			10	15	] no
Turn-On Delay Time	t <sub>d(on)</sub>			10	15	ns -
Rise Time	t <sub>r</sub>	$V_{DD}$ = 20 V, $R_L$ = 2 $\Omega$		15	25	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		30	45	
Fall Time	t <sub>f</sub>			10	15	
<b>Drain-Source Body Diode Characteristi</b>	cs					
Continuous Source-Drain Diode Current	I <sub>S</sub>	$T_C = 25  ^{\circ}C$			30	Α
Pulse Diode Forward Current	I <sub>SM</sub>				50	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>			30	60	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 10 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C		26	52	nC
Reverse Recovery Fall Time	t <sub>a</sub>	i <sub>F</sub> = 10 Λ, αί/αι = 100 Λ/μ5, 1 <sub>J</sub> = 25 °C		17.5		
Reverse Recovery Rise Time	t <sub>b</sub>	7		12.5		ns

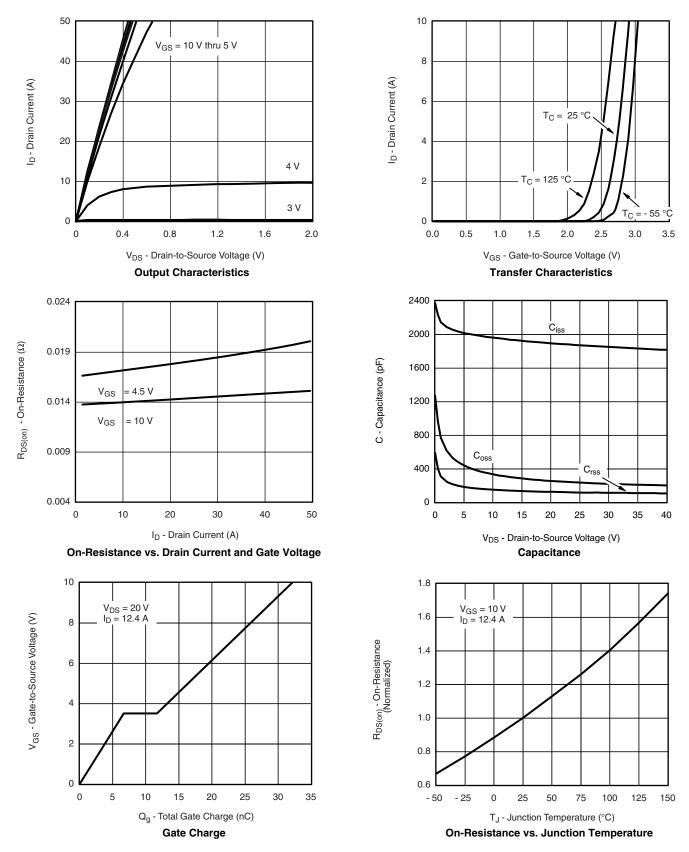
#### Notes

- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



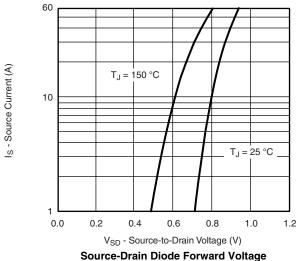
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

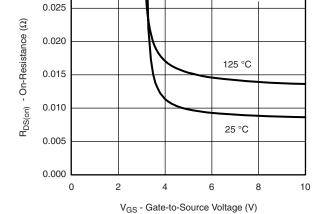




 $I_D = 12.4 A$ 

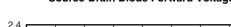
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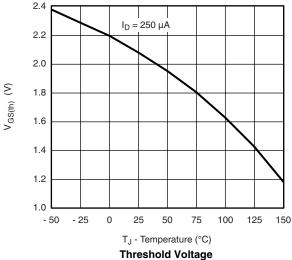


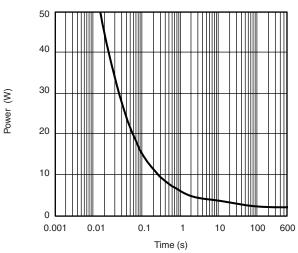


0.030

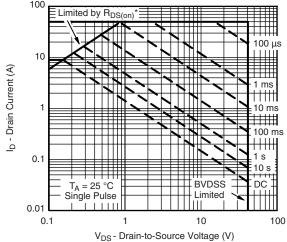
On-Resistance vs. Gate-to-Source Voltage







Single Pulse Power (Junction-to-Ambient)

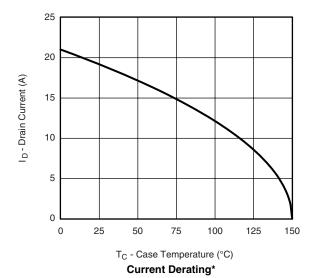


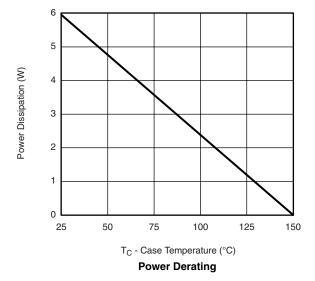
\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient



### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

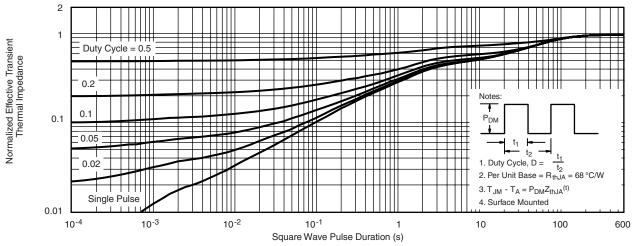




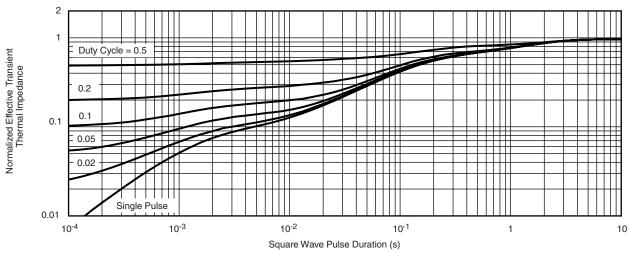
<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



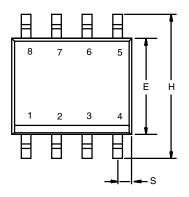
Normalized Thermal Transient Impedance, Junction-to-Ambient



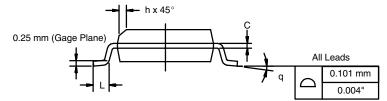
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





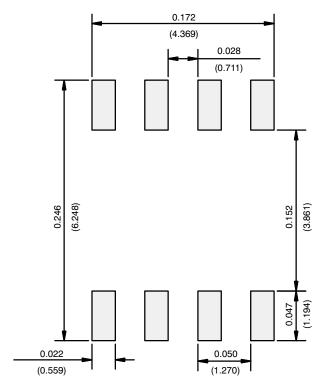


	MILLIM	IETERS	INC	INCHES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I, 11-Sep-06						

DWG: 5498



#### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

VDZA/4/U

www.VBsemi.com

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