

## N-Channel 200 V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$	200	V
$R_{DS(on)} V_{GS} = 10\text{ V}$	48	m $\Omega$
$I_D$	40	A
Configuration	Single	

### FEATURES

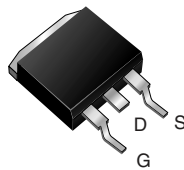
- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- PWM Optimized for Fast Switching
- Compliant to RoHS Directive 2002/95/EC



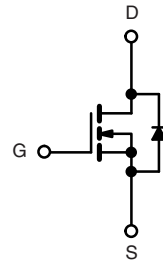
### APPLICATIONS

- Isolated DC/DC Converters  
- Primary-Side Switch

D<sup>2</sup>PAK (TO-263)



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ °C}$ , unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	200	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175\text{ °C}$ )	$T_C = 25\text{ °C}$	$I_D$	40	A
	$T_C = 125\text{ °C}$		25	
Pulsed Drain Current		$I_{DM}$	80	
Avalanche Current		$I_{AR}$	20	
Repetitive Avalanche Energy <sup>a</sup>	L = 0.1 mH	$E_{AR}$	16.2	mJ
Maximum Power Dissipation <sup>a</sup>	$T_C = 25\text{ °C}$	$P_D$	200 <sup>b</sup>	W
	$T_A = 25\text{ °C}^c$		4.5	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263) <sup>c</sup>	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)		$R_{thJC}$	1	

Notes:

- Duty cycle  $\leq 1\%$ .
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

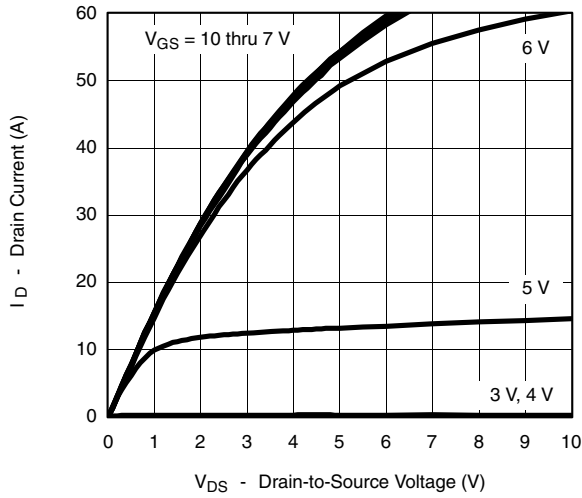
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min .	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	200			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 15\text{ V}, V_{GS} = 10\text{ V}$	60			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		48		m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$		150		
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$		180		
Drain-Source on State Resistance		$V_{GS} = 6.5\text{ V}, I_D = 15\text{ A}$		60		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$	15			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		3300		pF
Output Capacitance	$C_{oss}$			300		
Reverse Transfer Capacitance	$C_{rss}$			120		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		35		nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			11		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			14		
Gate Resistance	$R_G$			2		$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 100\text{ V}, R_L = 5\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\text{ }\Omega$		15	25	ns
Rise Time <sup>c</sup>	$t_r$			35	55	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			40	60	
Fall Time <sup>c</sup>	$t_f$			30	45	
<b>Source-Drain Diode Ratings and Characteristics</b> ( $T_C = 25\text{ }^\circ\text{C}$ ) <sup>b</sup>						
Continuous Current	$I_S$				40	A
Pulsed Current	$I_{SM}$				60	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 20\text{ A}, V_{GS} = 0\text{ V}$		1	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		115	170	ns
Peak Reverse Recovery Charge	$I_{RM(REC)}$			7.5	12	A
Reverse Recovery Charge	$Q_{rr}$			0.43	1.02	$\mu\text{C}$

Notes:

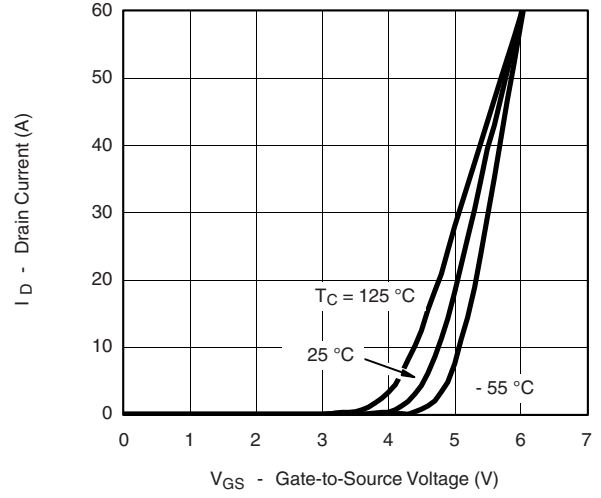
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

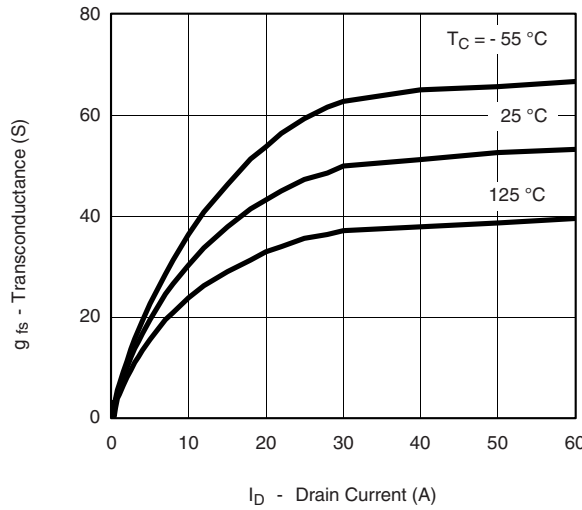
**TYPICAL CHARACTERISTICS** (25 °C unless noted)



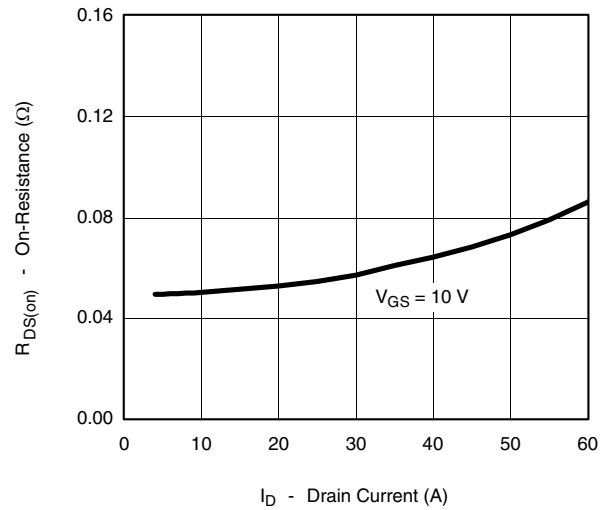
**Output Characteristics**



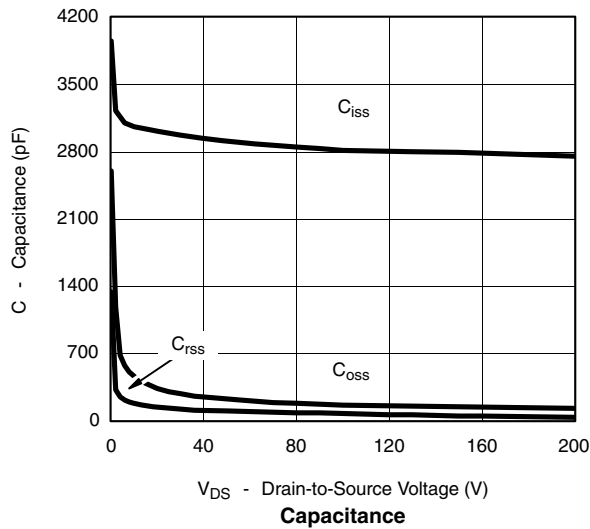
**Transfer Characteristics**



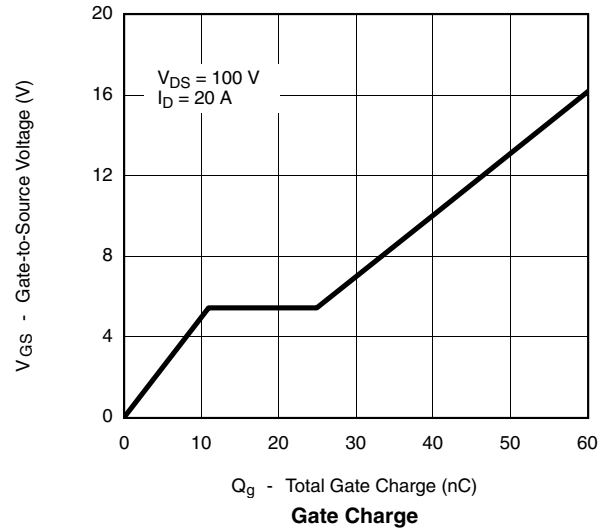
**Transconductance**



**On-Resistance vs. Drain Current**

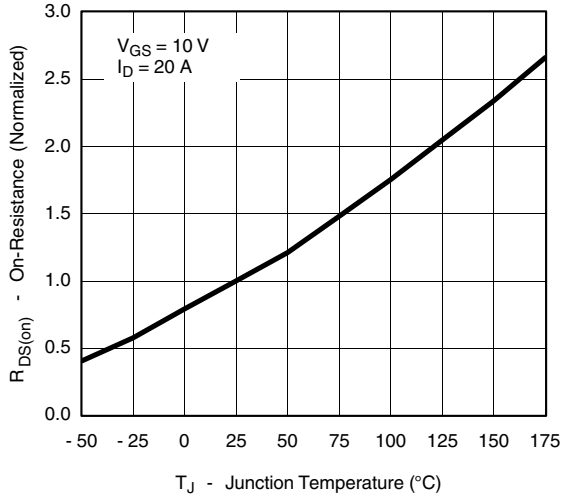


**Capacitance**

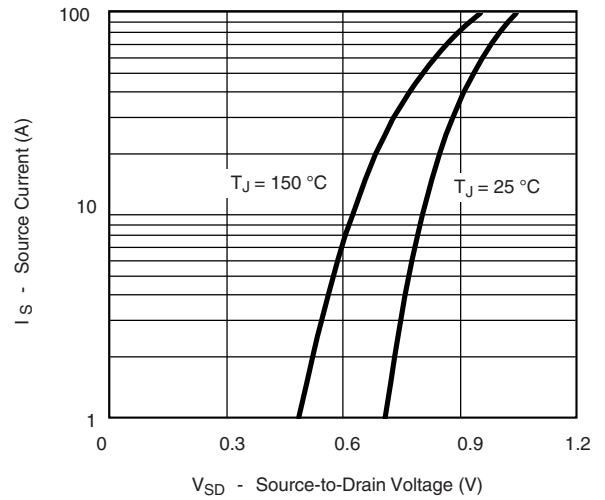


**Gate Charge**

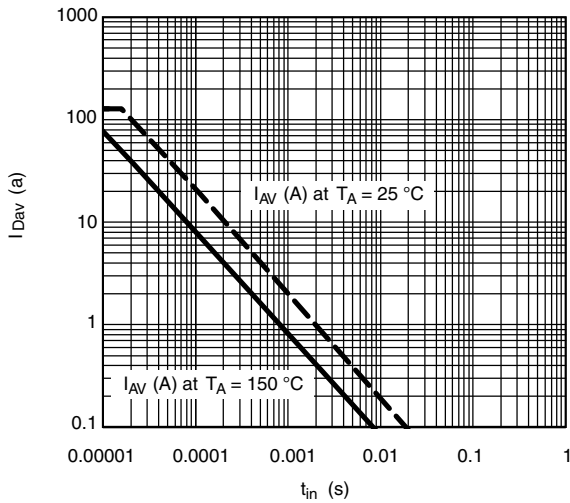
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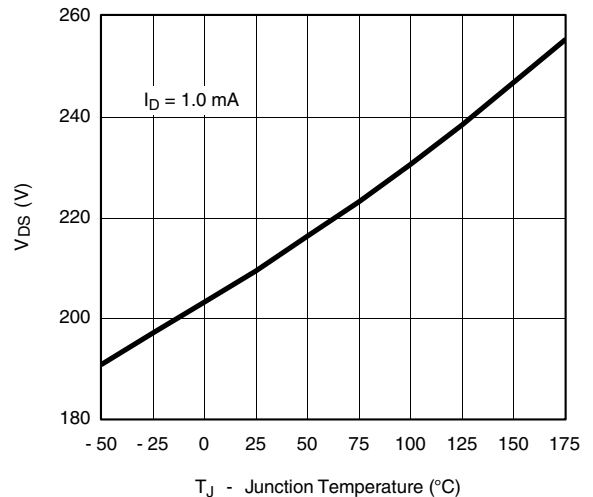
**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**

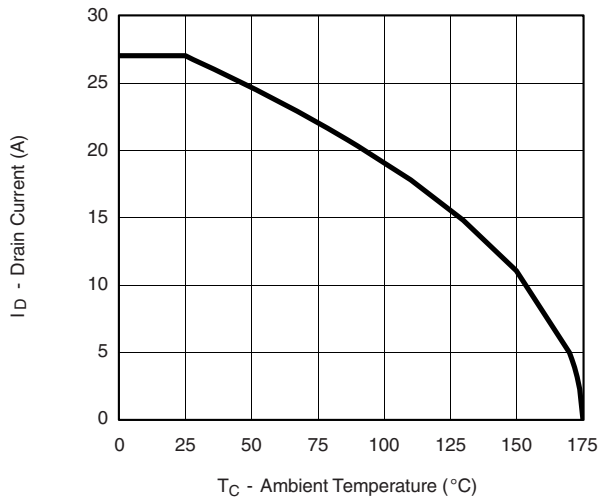


**Avalanche Current vs. Time**

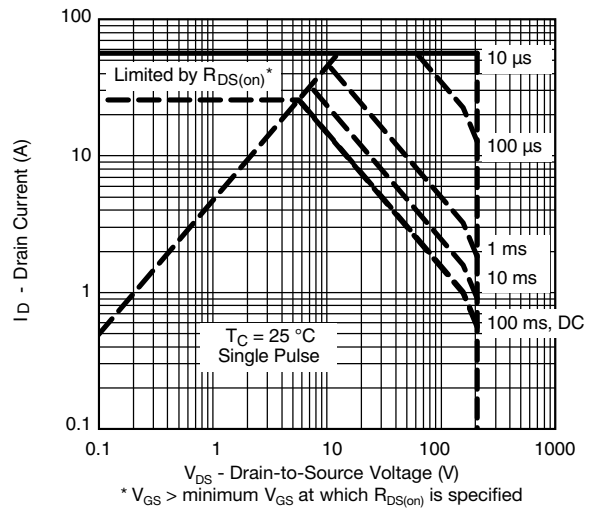


**Drain Source Breakdown vs. Junction Temperature**

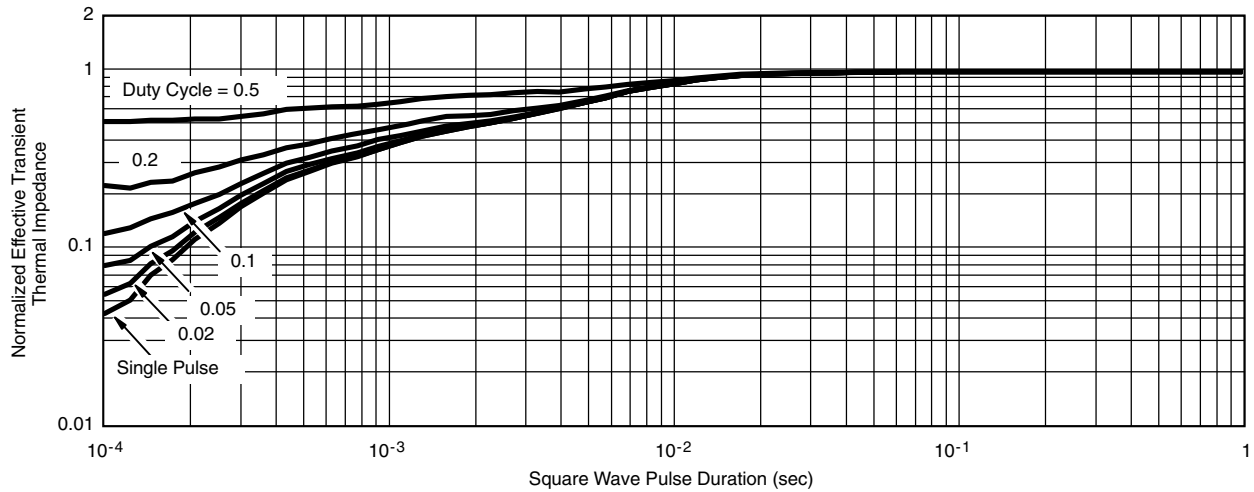
**THERMAL RATINGS**



**Maximum Avalanche and Drain Current vs. Case Temperature**



**Safe Operating Area**  
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**Normalized Thermal Transient Impedance, Junction-to-Case**

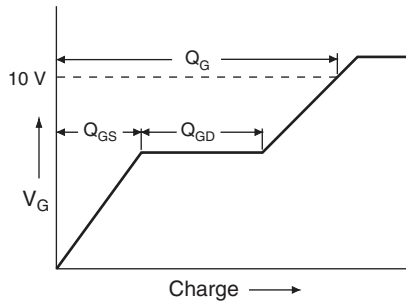


Fig. 13a - Basic Gate Charge Waveform

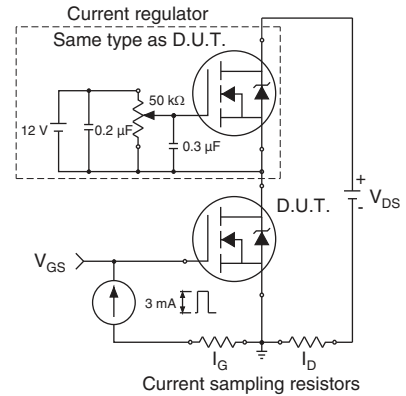
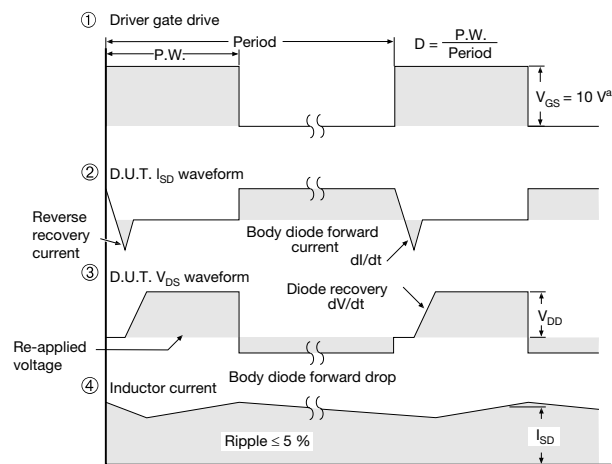
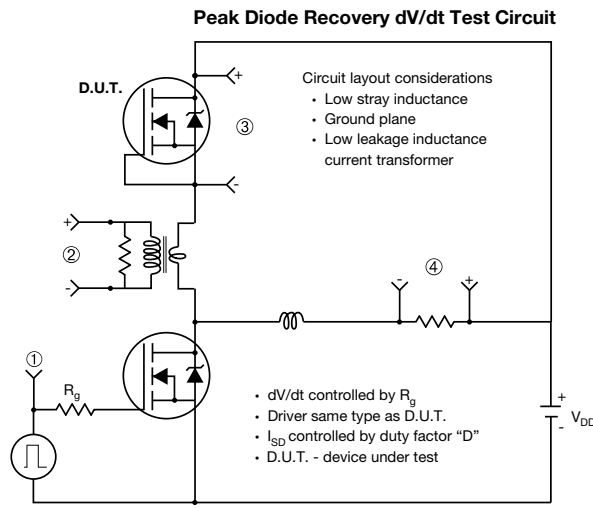


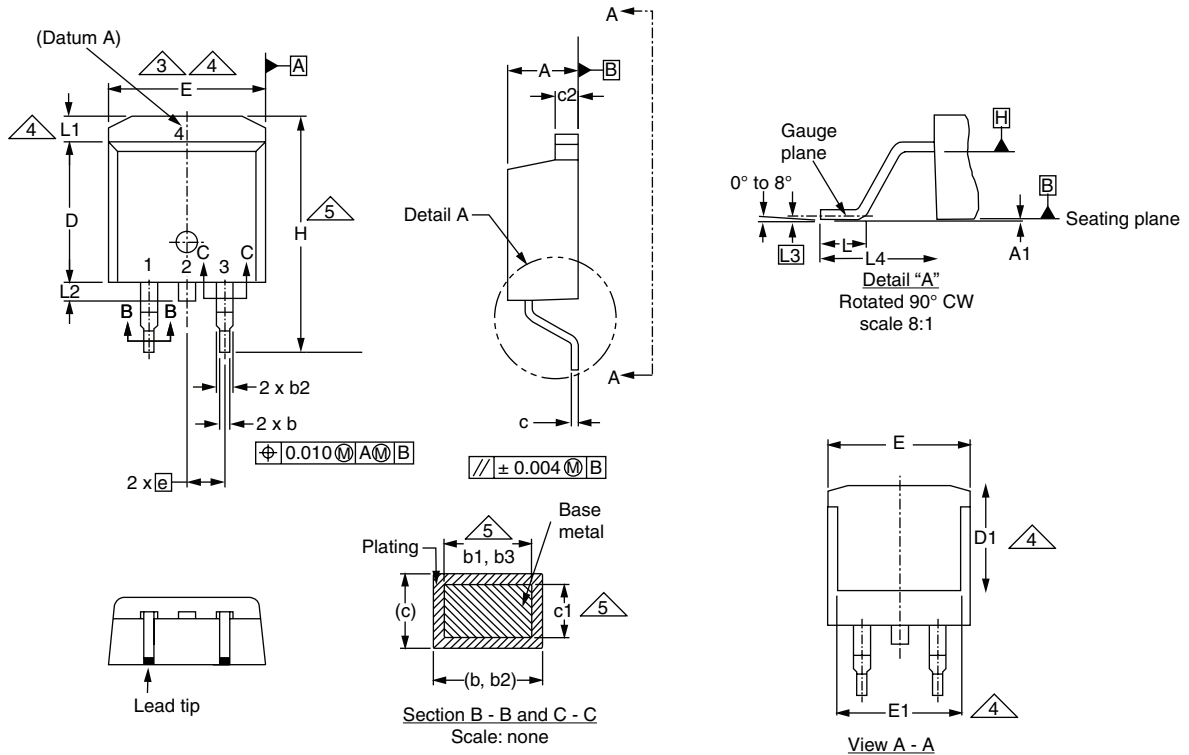
Fig. 13b - Gate Charge Test Circuit



**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 14 - For N-Channel

**TO-263AB (HIGH VOLTAGE)**



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

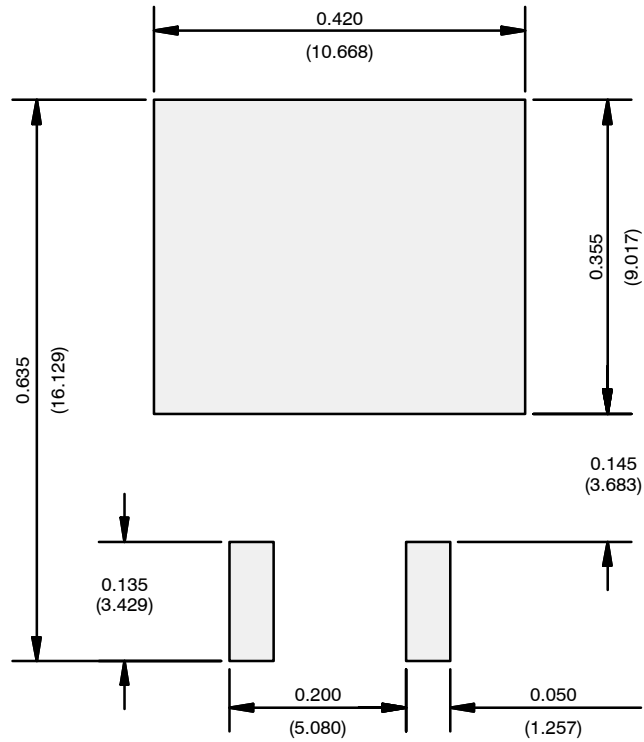
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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