VCC6

LVPECL, LVDS Crystal Oscillator Data Sheet

Description

Vectron's VCC6 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off either a 2.5 or 3.3 volt supply, hermetically sealed 7.0x5.0 mm ceramic package.

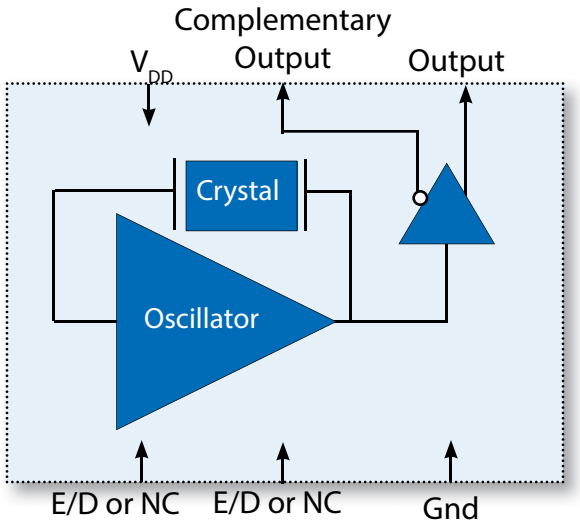
Features

- Ultra Low Jitter Performance, Fundamental or 3rd OT Crystal Design
- Output Frequencies to 275.000MHz
- 0.3 ps typical RMS jitter, 12k-20MHz
- Differential Output
- Enable/Disable
- -10/70°C, -40/85°C or -55/125°C Operation
- Hermetically Sealed 7.0x5.0 mm Ceramic Package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

Applications

- Ethernet, GbE, Synchronous Ethernet
- Fiber Channel
- Enterprise Servers
- Telecom
- Clock source for A/D's, D/A's
- Driving FPGA's
- Test and Measurement
- PON
- Medical
- COTS

Block Diagram



Performance Specifications

Table 1. Electrical Performance, LVPECL Option

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	3.135 2.375	3.3 2.5	3.465 2.625	V V
Current (No Load)	I_{DD}		50	98	mA
Frequency					
Nominal Frequency[2]	f_N	13.500		275.000	MHz
Stability[2,3] (Ordering Option)		±20, ±25, ±50, ±100			ppm
Outputs					
Output Logic Levels[4], -10/70°C Output Logic High Output Logic Low	 V_{OH} V_{OL}	 V_{DD}-1.025 V_{DD}-1.810		 V_{DD}-0.880 V_{DD}-1.620	 V V
Output Logic Levels[4], -40/85°C Output Logic High Output Logic Low	 V_{OH} V_{OL}	 V_{DD}-1.085 V_{DD}-1.830		 V_{DD}-0.880 V_{DD}-1.555	 V V
Output Rise and Fall Time[4]	t_R/t_F			600	ps
Load		50 ohms into V_{DD}-1.3V			
Duty Cycle[5]		45	50	55	%
Jitter (12 kHz - 20 MHz BW)155.52MHz[6]	ϕJ		0.3	0.7	ps
Period Jitter[7] RMS P/P Random Jitter Deterministic Jitter	ϕJ		 2.3 20 2.4 0		 ps ps ps ps
Enable/Disable					
Output Enabled[8] Output Disabled	V_{IH} V_{IL}	0.7*V_{DD}		 0.3*V_{DD}	V V
Disable Time	t_D			200	ns
Enable/Disable Leakage Current				±200	uA
Enable Pull-Up Resistor Output Enabled Output Disabled			 33 1		 KOhm MOhm
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70, -40/85 or -55/125			°C

1. The VCC6 power supply pin should be filtered, eg, a 0.1 and 0.01uf capacitor.
2. See Standard Frequencies and Ordering Information for more information.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Figure 1 defines the test circuit and Figure 2 defines these parameters.
5. Duty Cycle is defined as the On/Time Period.
6. Measured using an Agilent E5052, 155.520MHz. Please see "Typical Phase Noise and Jitter Report for the VCC6 series".
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

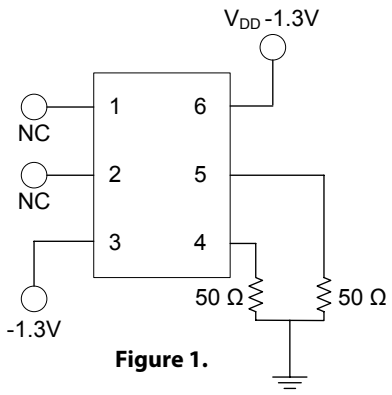


Figure 1.

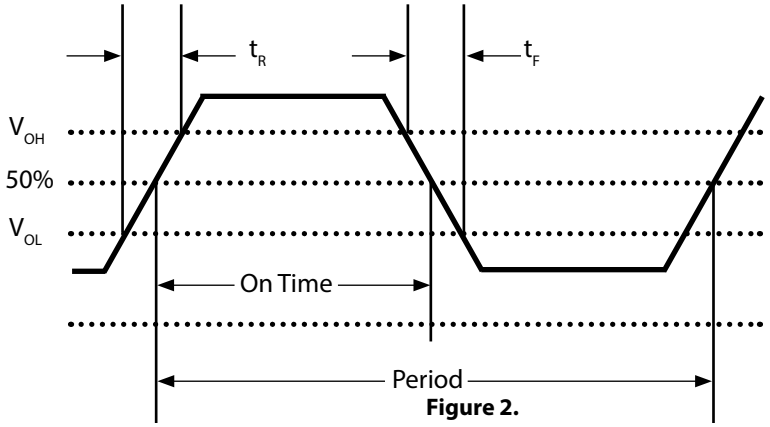


Figure 2.

Performance Specifications

Table 2. Electrical Performance, LVDS Option

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	3.135 2.375	3.3 2.5	3.465 2.625	V V
Current (No Load)	I_{DD}			60	mA
Frequency					
Nominal Frequency[2]	f_N	13.500		275.000	MHz
Stability[2,3,] (Ordering Option)		±20, ±25, ±50, ±100			ppm
Outputs					
Output Logic Levels[4] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 0.9	 1.43 1.10	 1.6	 V V
Differential Output Amplitude		247	330	454	mV
Differential Output Error				50	mV
Offset Voltage		1.125	1.25	1.375	V
Offset Voltage Error				50	mV
Output Leakage Current				10	uA
Output Rise and Fall Time[4]	t_R/t_F			600	ps
Load		100 ohms differential			
Duty Cycle[5]		45	50	55	%
Jitter (12 kHz - 20 MHz BW)155.52MHz[6]	ϕJ		0.3	0.7	ps
Period Jitter[7] RMS P/P Random Jitter Deterministic Jitter	ϕJ		 2.5 22 2.6 0		 ps ps ps ps
Enable/Disable					
Output Enabled[8] Output Disabled	V_{IH} V_{IL}	0.7*V_{DD}		 0.3*V_{DD}	V V
Disable Time	t_D			200	ns
Enable/Disable Leakage Current				±200	uA
Enable Pull-Up Resistor Output Enabled Output Disabled			 33 1		 KOhm MOhm
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70, -40/85 or -55/125			°C

1. The VCC6 power supply pin should be filtered, eg, a 0.1 and 0.01uf capacitor.
2. See Standard Frequencies and Ordering Information for more information.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Figure 2 defines these parameters and Figure 3 defines the test circuit.
5. Duty Cycle is defined as the On/Time Period.
6. Measured using an Agilent E5052, 155.520MHz. Please see "Typical Phase Noise and Jitter Report for the VCC6 series".
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

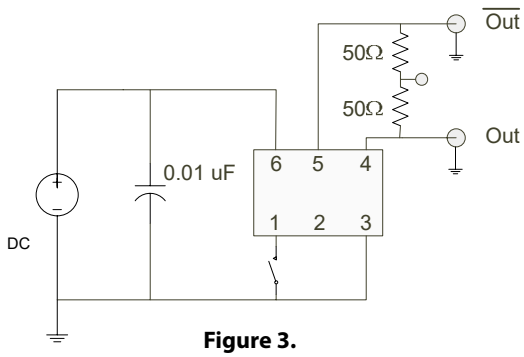


Figure 3.

LVPECL Application Diagrams

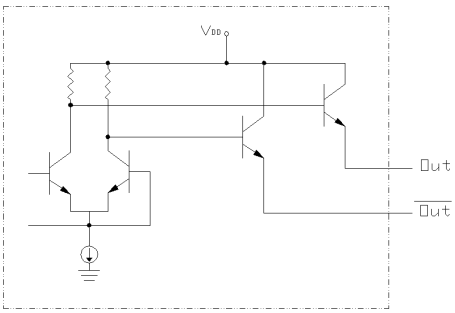


Figure 6. Standard PECL Output Configuration

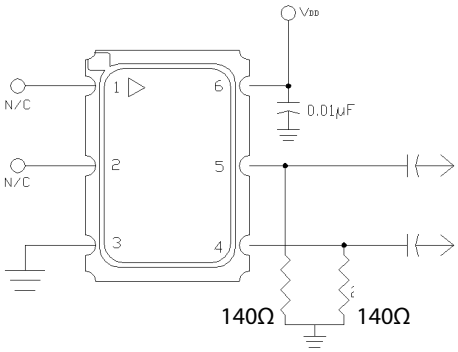


Figure 7. Single Resistor Termination Scheme
Resistor values are typically 140 ohms for 3.3V operation and 84 ohms for 2.5V operation.

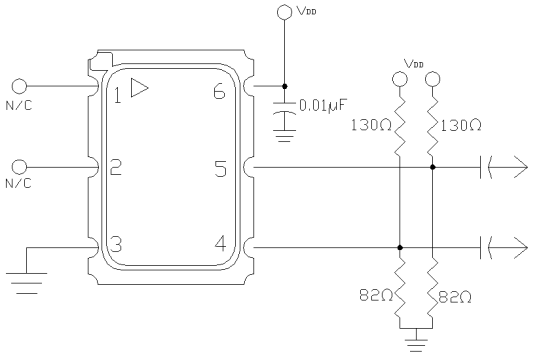


Figure 8. Pull-Up Pull Down Termination

Resistor values are typically for 3.3V operation For 2.5V operation, the resistor to ground is 62

The VCC6 incorporates a standard PECL output scheme, which are un-terminated emitters as shown in Figure 6. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 7, and a pull-up/pull-down scheme as shown in Figure 8. An AC coupling capacitor is optional, depending on the application and the input logic requirements of the next stage.

LVDS Application Diagrams

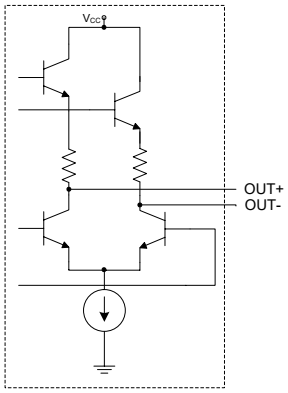


Figure 9. Standard LVDS Output Configuration

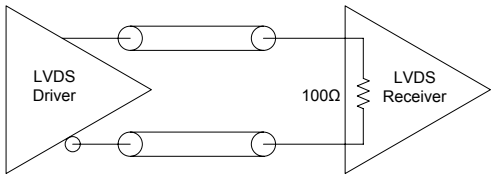


Figure 10. LVDS to LVDS Connection, Internal 100ohm

Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components.

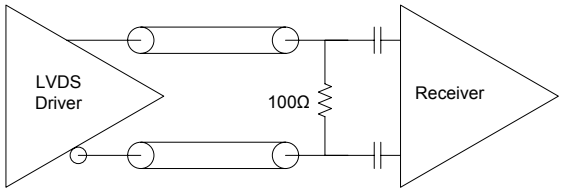


Figure 11. LVDS to LVDS Connection External 100ohm and AC blocking caps

Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

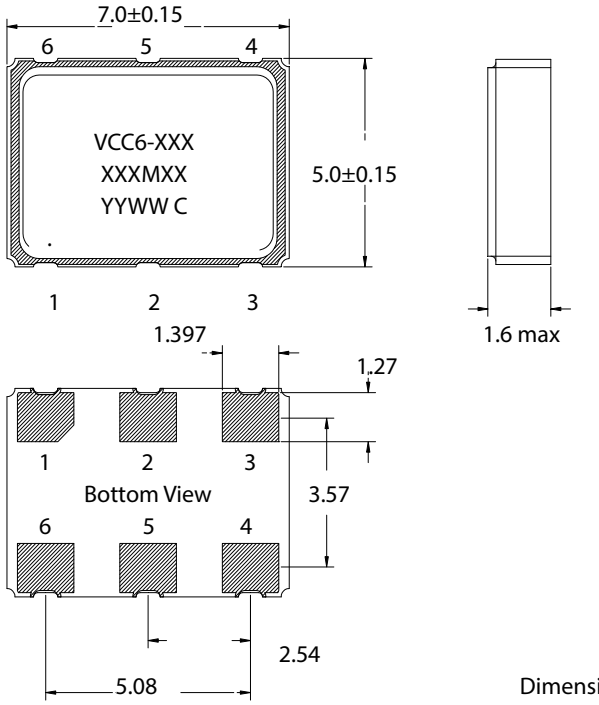
Package and Pinout

Table 3. Pinout

Pin #	Symbol	Function
1	E/D or NC	Enable Disable or No Connection
2	E/D or NC	Enable Disable or No Connection
3	GND	Electrical and Lid Ground
4	f_O	Output Frequency
5	Cf_O	Complementary Output Frequency
6	V_{DD}	Supply Voltage

Table 4. Enable Disable Function (optional on pin 1 or pin2)

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance



Dimensions are in mm

Figure 4. Package Outline Drawing

Marking Information

VCC6-XXX = VCC6 Product family and ordering options
XXXMXX = Frequency (example 100M00)
YY= Year of Manufacture
WW = Week of the Year
C = Manufacturing Location
. = Pin 1

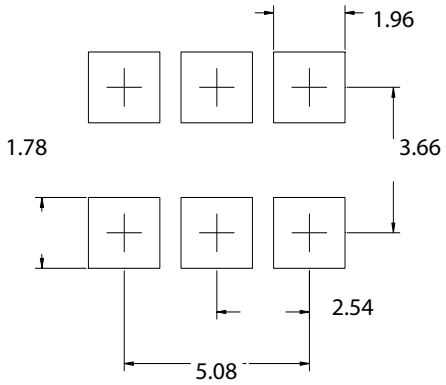
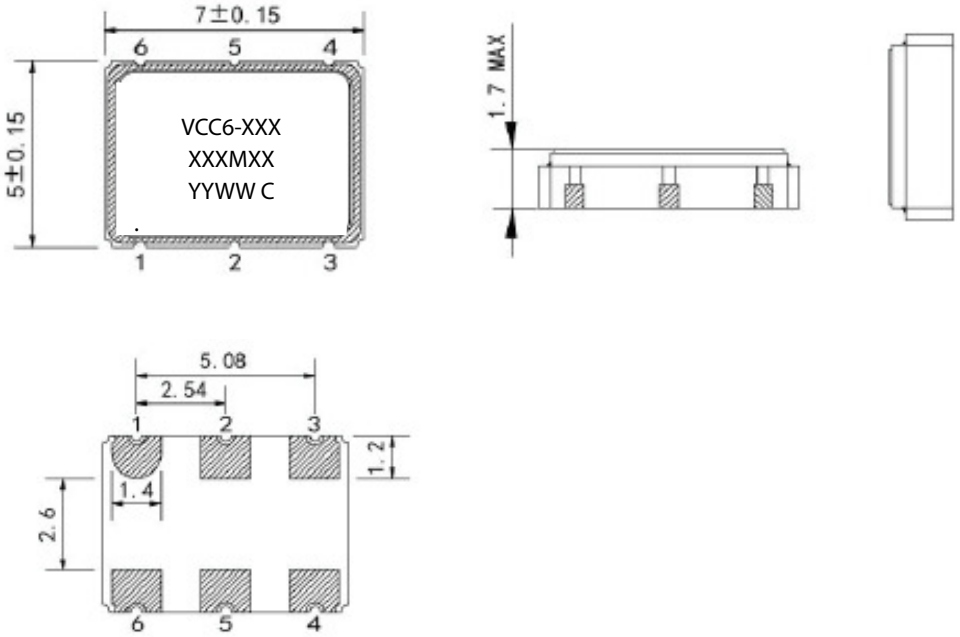


Figure 5. Pad Layout

Alternative Package



Environmental and IR Compliance

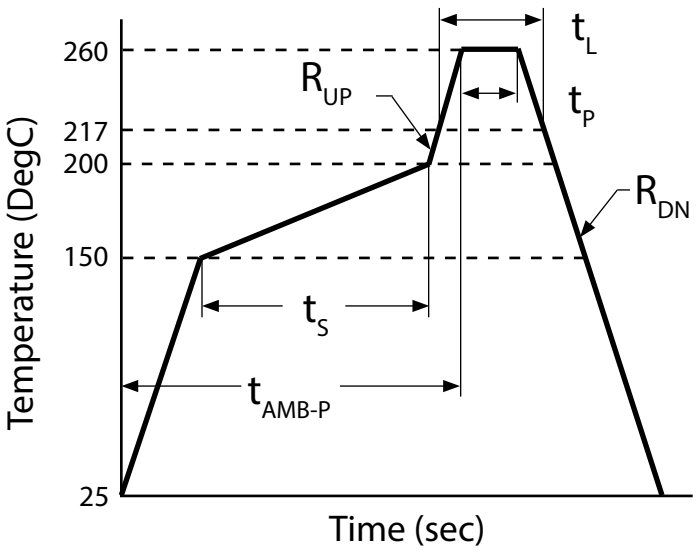
Table 5. Environmental Compliance	
Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold (0.3 um min - 1.0 um max) over Nickel
ThetaJC (bottom of package)	13 °C/W
Weight	170 mg

IR Compliance

Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 5. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Table 6. Reflow Profile		
Parameter	Symbol	Value
PreHeat Time	ts	200 sec Max
Ramp Up	R_{UP}	3°C/sec Max
Time above 217°C	tL	150 sec Max
Time to Peak Temperature	tAMB-P	480 sec Max
Time at 260°C	tP	30 sec Max
Time at 240°C	tP2	60 sec Max
Ramp down	R_{DN}	6°C/sec Max



Maximum Ratings, Tape & Reel

Absolute Maximum Ratings and Handling Precautions

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Although ESD protection circuitry has been designed into the VCC6, proper precautions should be taken when handling and mounting. Vectron employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation.
ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

Table 7. Maximum Ratings

Parameter	Symbol	Rating	Unit
Storage Temperature	T_{STORE}	-55/125	°C
Supply Voltage		-0.5 to 5.0	V
Enable/Disable Voltage		-0.5 to V_{DD}+0.5	V
ESD, Human Body Model		1500	V
ESD, Charged Device Model		1000	V

Table 8. Tape and Reel Information

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	180	2	13	21	55	17	21	1000

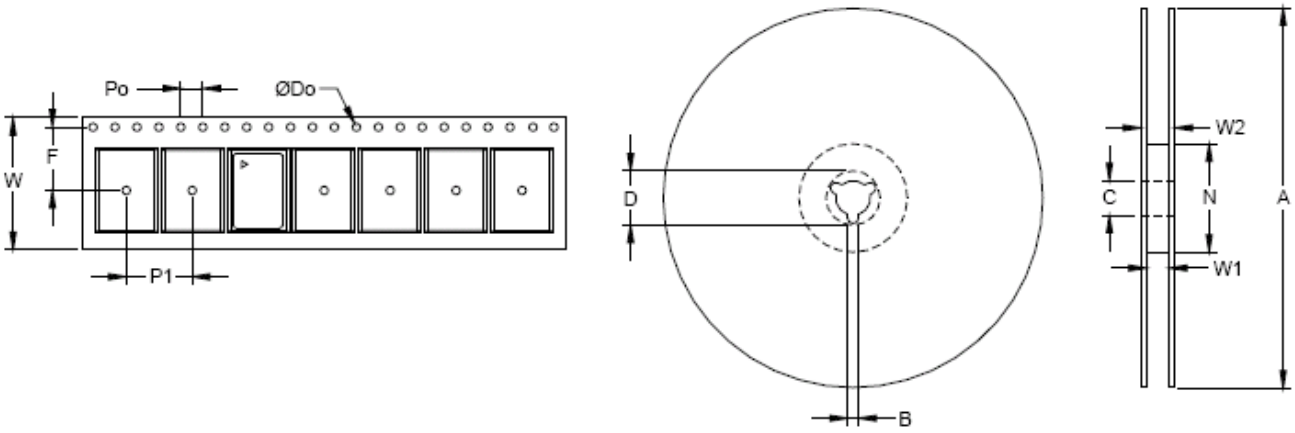


Table 9. Standard Frequencies (MHz)										
19.4400	25.0000	27.1200	30.7200	33.0000	33.3330	35.0000	35.5000	38.8800	40.0000	40.6800
43.7500	48.0000	50.0000	53.1250	56.0000	61.440	62.2080	62.5000	66.0000	68.0000	70.0000
71.5000	74.1758	74.2500	75.0000	75.4000	77.7600	78.1250	80.0000	81.2500	83.3330	84.0000
86.0000	87.5000	90.0000	95.0000	99.1440	100.0000	105.0000	106.2500	110.0000	112.0000	112.5000
114.2850	120.0000	122.8800	124.4160	125.0000	125.0093	128.0000	130.0000	130.5882	132.8125	133.0000
135.0000	136.0000	140.0000	142.5408	143.0000	148.7500	150.0000	153.6000	153.8500	155.5200	156.1734
156.2500	156.253906	156.261718	156.2740	156.2930	159.3750	160.0000	161.1300	161.1328	162.3250	164.3555
165.0000	166.0000	166.5600	166.6286	166.6667	167.3300	167.3317	167.328125	167.4100	168.2009	168.6997
172.6423	173.3700	173.3708	173.4380	175.000	176.0950	176.8382	177.3437	178.018970	178.1250	178.5000
180.0000	187.0177	187.5000	190.0000	192.4560	195.3125	200.0000	210.0000	212.4840	212.5000	218.7500
225.0000	250.0000	260.0000	266.0000	275.0000						

Ordering Information

VCC6 - X X X - xxMxxxxxxxXX

Product
XO, 7.0x5.0 mm Ceramic Package

Output and Voltage
Q: +3.3 Vdc ±5%, LVPECL
R: +2.5 Vdc ±5%, LVPECL
L: +3.3 Vdc ±5%, LVDS
V: +2.5 Vdc ±5%, LVDS

Enable/Disable
A: E/D is on Pin 2
C: E/D is on Pin 1

Packaging
TR: Tape and Reel
blank: Cut Tape / non Tape and Reel quantities
_SNPB: Tin lead solder dipped

Frequency in MHz

Stability/Temp Range
A: ±100 ppm over -10/70°C
B: ±50 ppm over -10/70°C
C: ±100 ppm over -40/85°C
D: ±50 ppm over -40/85°C
E: ±25 ppm over -10/70°C
F: ±25 ppm over -40/85°C
G: ±20 ppm over -10/70°C, excludes aging
P: ±100 ppm over -55/125°C
R: ±50 ppm over -55/125°C

**Note: not all combination of options are available.*
P code is available ≤ 156M250, R code is avaiable ≤ 125M000
Other specifications may be available upon request.

±20ppm Options

VCC6-107-frequency	LVPECL	+3.3V	±20ppm over -10/70°C, includes 10 years aging, E/D on Pin1
VCC6-109-frequency	LVDS	+3.3V	±20ppm over -10/70°C, includes 10 years aging, E/D on Pin1
VCC6-110-frequency	LVPECL	+2.5V	±20ppm over -10/70°C, includes 10 years aging, E/D on Pin1
VCC6-111-frequency	LVDS	+2.5V	±20ppm over -10/70°C, includes 10 years aging, E/D on Pin1
VCC6-119-frequency	LVPECL	+3.3V	±20ppm over -40/85°C, includes 10 years aging, E/D on Pin1
VCC6-120-frequency	LVPECL	+2.5V	±20ppm over -40/85°C, includes 10 years aging, E/D on Pin1
VCC6-121-frequency	LVDS	+3.3V	±20ppm over -40/85°C, includes 10 years aging, E/D on Pin1
VCC6-122-frequency	LVDS	+2.5V	±20ppm over -40/85°C, includes 10 years aging, E/D on Pin1

Example:

VCC6-QCD-156M250000TR	**Tape and Reel**
VCC6-QCD-156M250000	**Cut Tape**
VCC6-QCD-156M250000_SNPB	**Tin lead solder dipped**

Revision History

Revision Date	Approved	Description
Feb 12, 2014	TG	Updated Vectron Logo, Hudson & Asia Contact Address
Aug 04, 2014	VN	Frequency range Limited to 275MHz. Removed Optional 7.5x5.08mm package.
Aug 10, 2018	FB	Update logo and contact information, added SNPBDIP ordering option
March 19,2019	FB	Update logo and contact ifnoromation, change SNPBDIP to SNPB, add E/D logic Table 4, weight, thetaJC and R ordering option
April 30, 2020	FB	Add tape and reel ordering option, update min frequency to 13.500MHz, updates and corrections as needed

Contact Information

USA:
100 Watts Street
Mt Holly Springs, PA 17065
Tel: 1.717.486.3411
Fax: 1.717.486.5920

Europe:
Landstrasse
74924 Neckarbischofsheim
Germany
Tel: +49 (0) 7268.801.0
Fax: +49 (0) 7268.801.281

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