GENERAL DESCRIPTION

The VM3011 is a high performance, low noise digital MEMS microphone. It features Vesper's Adaptive ZeroPower Listening™ that dramatically extends the battery life of always-on, always listening systems. Adaptive Intelligence constantly monitors the ambient level to activate the system only when a sound is detected above the background noise level. The entire signal chain of always-listening system is in hibernate mode while listening for an event or a wake word. When an event is detected, the microphone switches to a Normal Mode where it will operate as any standard PDM multi-mode microphone.

The VM3011 has an industry standard 3.76 x 2.95 x 1.3mm package. The microphone is solder reflow compatible with no sensitivity degradation. Vesper's Piezoelectric MEMS construction also enables operation in in environmentally harsh surroundings due to IP57 dust and moisture resistance rating. It is ideal for applications requiring voice activation in battery powered consumer devices.

FEATURES

- Adaptive ZeroPower Listening™ (ZPL) Microphone with ultra-low power acoustic activity detection
- Ambient Sound Engine using I2C register readback
- Dust and moisture resistant
- Digital Output, Pulse Density Modulation (PDM)
- Mode switching using Clock Speed
- Adaptive ZPL mode configurable through I2C
- Ultra-fast startup in all modes including ZPL to Normal mode, 200 µSec
- RFI and EMI robust
- Wide Temperature Range: -40C to 85C
- Industry standard 3.76 x 2.95mm LGA package footprint

APPLICATIONS

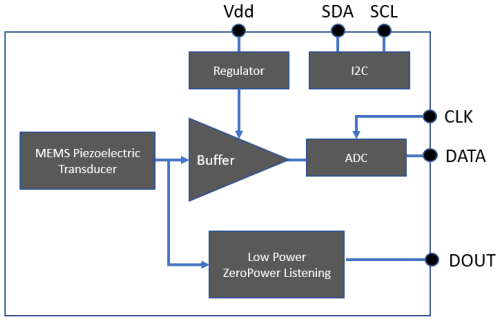
- Smart Home Devices
- TV Remotes
- Smart Watches and other Wearables
- IP Security Cameras
- Hearables
- Any battery-operated application with wakeup on sound

ORDERING INFORMATION

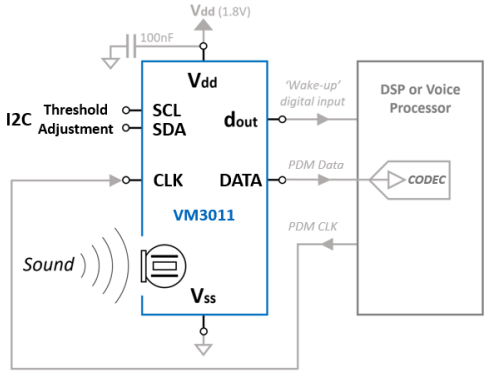
Product	Package Description	Quantity
VM3011AA	13" Tape and Reel	5,000

See Lid Marking Section for actual product marking

BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



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SPECIFICATIONS

The table below shows **General Acoustic and Electrical specifications** at 25°C, VDD = 1.8 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	VDD		1.6	1.8	3.6	V
Sensitivity	SENS	1 kHz, 94 dB SPL	-27	-26	-25	dBFS
Output DC Offset				0		% FS
Roll Off Frequency		-3dB at 1KHz		100		Hz
Directivity			Omni			
Polarity		Increase in sound pressure	Increase in density of 1's			
Supply Current- ZeroPower Listening Mode[1]		VDD On, CLK Off (CLK must be logic LOW)		10		µA
Supply Current- Standby Mode		VDD On, 200kHz < CLK < 250 kHz No Audio Output, DATA line outputs CLK at 50% Duty Cycle		98		µA
Time to First Data Bit		Time from valid Vdd and CLK until the first valid bit is driven on the DATA line. Output is Hi-Z until then.		0.1		mS
Startup Time		(Powered Down, Standby or ZPL) → Active (Low Power or Normal Mode) Within ±0.5dB of actual sensitivity		0.2		mS
Mode-Change Time		Between any modes (ZPL, Standby, Low Power, Full Power)		0.2		mS

Note 1: In very quiet environments where SPL < 50 dB, the current consumption in ZPL mode will increase from 10 µA to 16 µA

The table below shows specifications for **ZeroPower Listening Mode** (CLK OFF, LOGIC LOW) at 25°C, VDD = 1.8 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Max Acoustic Threshold		Read-only Register 0x01 = 0x1F, 1kHz signal		91.5		dB SPL
Min Acoustic Threshold		Read-only Register 0x01 = 0x00, 1kHz signal		45		dB SPL

Table below shows specifications for **Normal Mode** (1.1MHZ < CLK < 4MHZ) at 25°C, VDD = 1.8 V, CLK = 2.4MHz, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Signal-to-Noise Ratio	SNR	94 dB SPL at 1 kHz signal, 20Hz-20kHz, A-weighted Noise		64		dB(A)
Signal-to-Noise Ratio, Voice Band	SNR	94 dB SPL at 1 kHz signal, 20Hz-8kHz, A-weighted Noise		66		dB(A)
Total Harmonic Distortion	THD	94 dB SPL		0.1		%
		120dB SPL		1		
Acoustic Overload Point	AOP	10.0% THD		122		dB SPL
Power Supply Rejection Ratio	PSRR	VDD = 1.8V, 1kHz, 100mV$_{PP}$ Sine Wave (1)		-57		dBFS/dBV
Power Supply Rejection	PSR	VDD = 1.8V, 217Hz, 100mV$_{PP}$ square wave, 20 Hz – 20kHz, A-weighted		-87		dB(A)
Supply Current		CLK = 1.536MHz		525		µA
		CLK = 2.4MHz		635		µA
		CLK = 3.072MHz		725		µA

(1) PSRR will be -67dBFS/dBV if I2C uses a separate power supply that is not Vdd

Table below shows specifications for **Low Power Mode** (350kHZ < CLK < 900kHz) at 25°C, VDD = 1.8 V, CLK = 768kHz, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Signal-to-Noise Ratio, Voice Band	SNR	94 dB SPL at 1 kHz signal, 20Hz-8kHz, A-weighted Noise		64		dB(A)
Total Harmonic Distortion	THD	94 dB SPL		0.1		%
		120dB SPL		1		
Acoustic Overload Point	AOP	10.0% THD		122		dB SPL
Power Supply Rejection Ratio	PSRR	VDD = 1.8, 1kHz, 100mV$_{PP}$ Sine Wave(2)		-57		dBFS/dBV
Power Supply Rejection	PSR	VDD = 1.8, 217Hz, 100mV$_{PP}$ square wave, 20 Hz – 8kHz, A-weighted		-87		dB(A)
Supply Current		CLK = 768kHz		350		µA

(2) PSRR will be -67dBFS/dBV if I2C uses a separate power supply than Vdd

DEVICE MODES

MODE	Conditions	DATA Output	DOUT Output	Mode Transition Time	Supply Current
OFF	VDD OFF	NA	NA	NA	NA
ZPL	VDD ON, CLK OFF (LOGIC LOW)	NA	ZPL FLAG	200 µSec	10 µA
STANDBY	VDD ON, CLK ON (< 250 kHz)	PDM CLK, No Audio Output	NA	200 µSec	88 µA
LOW POWER	VDD ON, 350 kHz < CLK ON < 900 kHz	PDM	ZPL FLAG	200 µSec	400 µA
Full POWER	VDD ON, CLK ON > 1.1 MHz	PDM	ZPL FLAG	NA	700 µA

Note: 1) The first time Vdd is applied, it will take 1sec for the ZPL mode to adapt to the environment and be ready to trigger on external sounds.
2) In very quiet environments where SPL < 50 dB, the current consumption in ZPL mode will increase from 10 µA to 16 µA

CHANNEL SELECTION

Channel	Select	Asserts DATA on	Latch DATA on
Left	GND	Falling Edge of CLK	Rising Edge of CLK
Right	VDD	Rising Edge of CLK	Falling Edge of CLK

PDM DIGITAL SPECIFICATIONS

Parameter	Conditions	Min.	Typ.	Max.	Units
Logic Input High		0.65*VDD		VDD	V
Logic Input Low		-0.3		0.35*VDD	V
Logic Output High	I_{Load} = 0.5mA	0.7*VDD	VDD		V
Logic Output Low	I_{Load} = 0.5mA		0	0.3*VDD	V
Driving Capability				100	pF

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Supply Voltage	-0.3 to +3.6	V
Sound Pressure Level	160	dB re 20 µPa
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-55 to +150	°C

ENVIRONMENTAL ROBUSTNESS

IP adherence is evaluated by 1kHz Sensitivity spec post-stress

Ingress Protection Type	Description
Dust Resistance	IP5X;
Water Immersion	IPX7; 2 hours drying time, dry environment

RELIABILITY SPECIFICATIONS

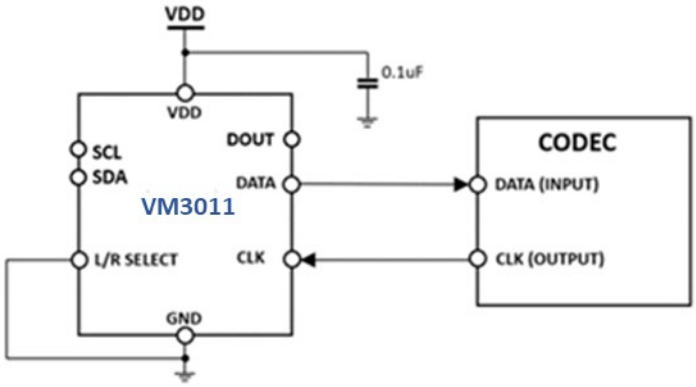
Stress Test	Description
Temperature Cycling Test	-40°C to +125°C, 850 cycles
High-Temperature Operating Life	+125°C, 1000 hours, biased
High-Temperature Storage	+125°C, 1000 hours, unbiased
Temperature Humidity Bias	+85°C, 85% RH, 1000 hours, biased
Reflow	3 reflow cycles with peak temperature of +260°C
ESD-HBM	3 discharge, all pins, ± 2kV
ESD-CDM	3 discharges, all pins, ± 750V
Mechanical Shock	10,000g per MIL-STD-883 M2002

MICROPHONE OPERATION

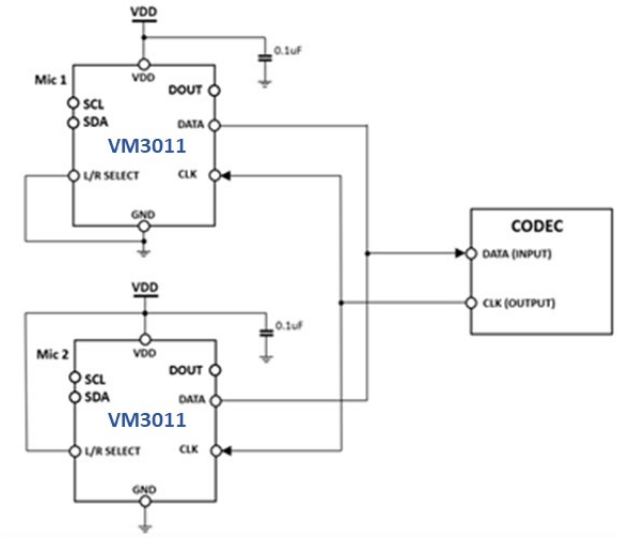
NORMAL MODE

The VM3011 is a Pulse Density Modulated (PDM) digital output microphone. It takes the audio signal from the Piezo MEMS element, amplifies it, and samples at a very high rate, converting it to a single-bit stream PDM using a fourth-order sigma-delta modulator. This PDM data (DATA) is ready to be interfaced directly to a codec, applications processor, or other compatible hardware. The master system (codec, etc.) provides the master clock, CLK, which defines the rate at which the bits are transmitted on the DATA line. The data is set on the rising or falling edge of the CLK, defined by the L/R Select pin, with L/R Select=GND (left) setting data on the falling edge, and L/R Select=Vdd (right) setting data on the rising edge. This allows two microphones to be connected to form a stereo configuration over a single DATA line. The CODEC or processor can then separate the bitstreams based on their alignment with the CLK edges

In *Normal* mode, the microphone streams the incoming audio signal, amplifies it, and samples at a very high rate, outputting Pulse Density Modulated (PDM) data using a fourth-order sigma-delta modulator. This PDM data is ready to be interfaced directly to a DSP/SOC/MCU. The codec provides the master CLK signal that controls the microphone CLK signal.



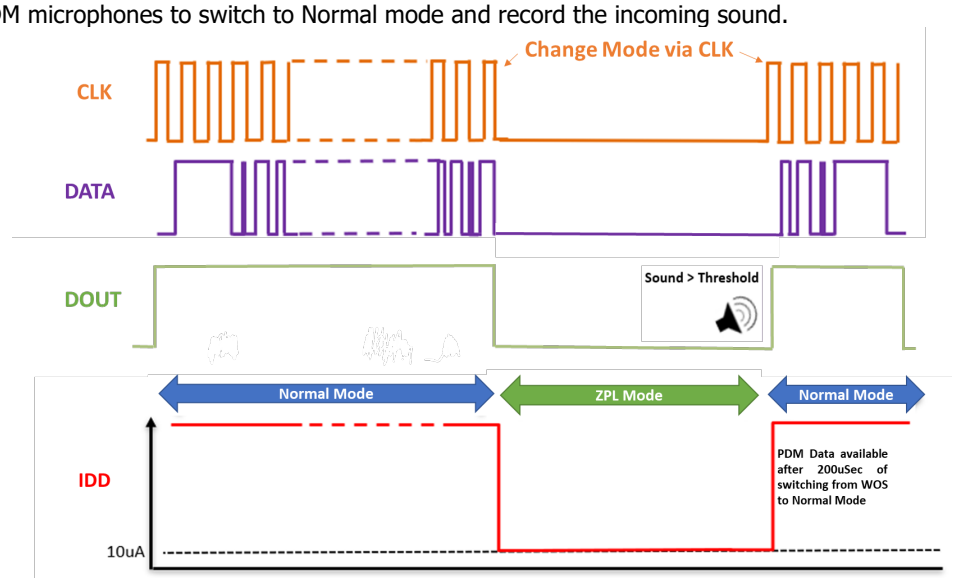
Typical Application Circuit for Mono Microphone Configuration (Left Channel Selected)



Typical Application Circuit for Stereo Microphone Configuration

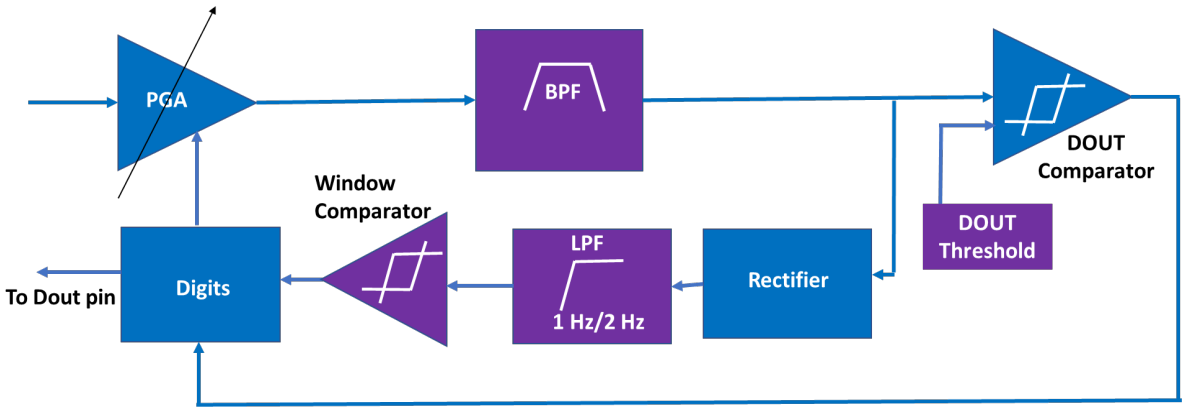
ADAPTIVE ZERO POWER LISTENING™ MODE

VM3011 uses the clock speed to change device modes. The DATA pin outputs PDM output in normal mode operation. When no clock is applied, the device enters ZPL mode by default. In ZPL mode, DOUT outputs a single bit "Threshold Exceeded" Flag when the acoustic input is greater than the set threshold. The typical application circuit for the VM3011 is shown below on the left. Usage of the DATA pin for PDM output and the DOUT pin for Wake on Sound (WoS) digital trigger is shown below. VM3011 automatically adapts to the background noise level present in the environment. ZPL threshold will be automatically set by the microphone to ensure that the microphone does not trigger too often with high background noise level. Similarly, it also makes sure that it does not easily trigger in a quiet environment. When the incoming sound exceeds the ZPL threshold, the microphone sends an interrupt signal to the external codec or voice processor using a Digital Output pin. The processor then sends a clock signal to the PDM microphones to switch to Normal mode and record the incoming sound.



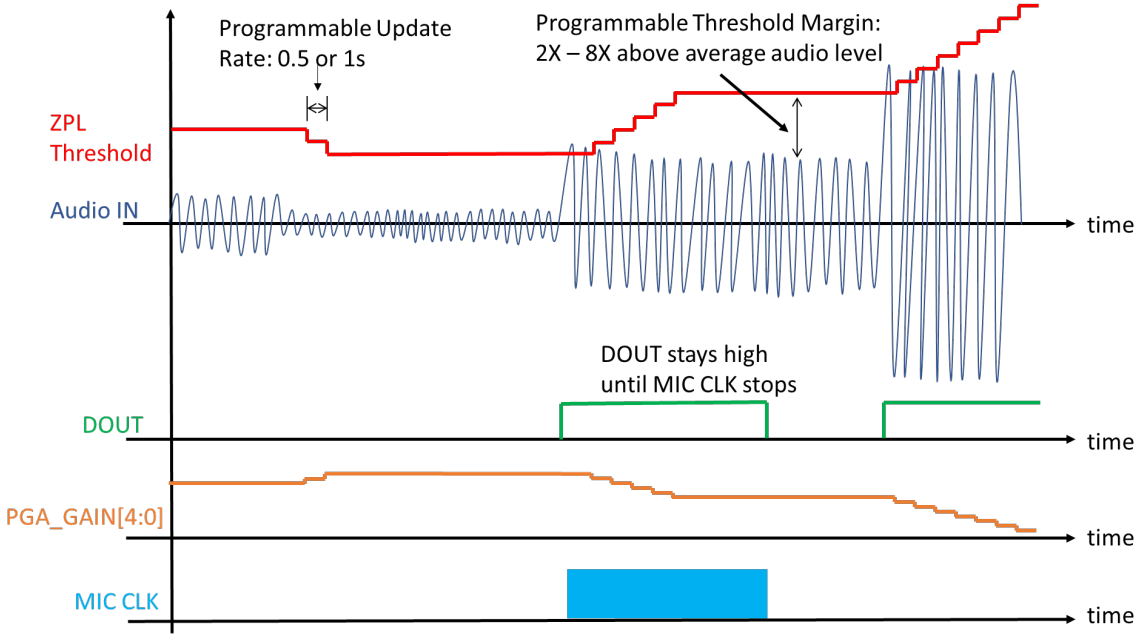
Switching between different microphone modes using PDM CLK

VM3011 block diagram with user-programmable blocks is shown below. Blocks shown in Purple indicate I2C R/W programmable registers.



Block Diagram of VM3011 with I2C programmable blocks shown in purple

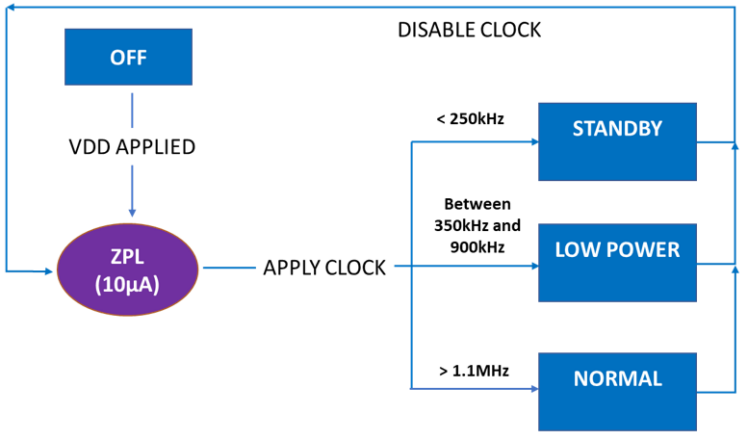
Adaptive Mode automatically senses the average sound level of the environment, and adjusts the gain parameter, PGA_GAIN of the programmable gain amplifier (PGA) over time. This is accomplished using a rectifier, low-pass filter (LPF), and window comparator in the feedback path of the ZPL mode. This feedback path tries to keep the input of the DOUT comparator near a fixed amplitude by rectifying the signal and filtering it with a very low corner low-pass filter (1Hz or 2Hz). Filtering with a 1Hz or 2Hz filter gives a slow-moving, long term average representation of the input sound level. The adaptive loop converges to the average acoustic input level within 1sec after power up and then slows back down to either 1 Hz to 2 Hz depending on how WOS_RMS bit is set. A visual description of the VM3011 Adaptive ZPL mode is shown below



VM3011 Functional Description

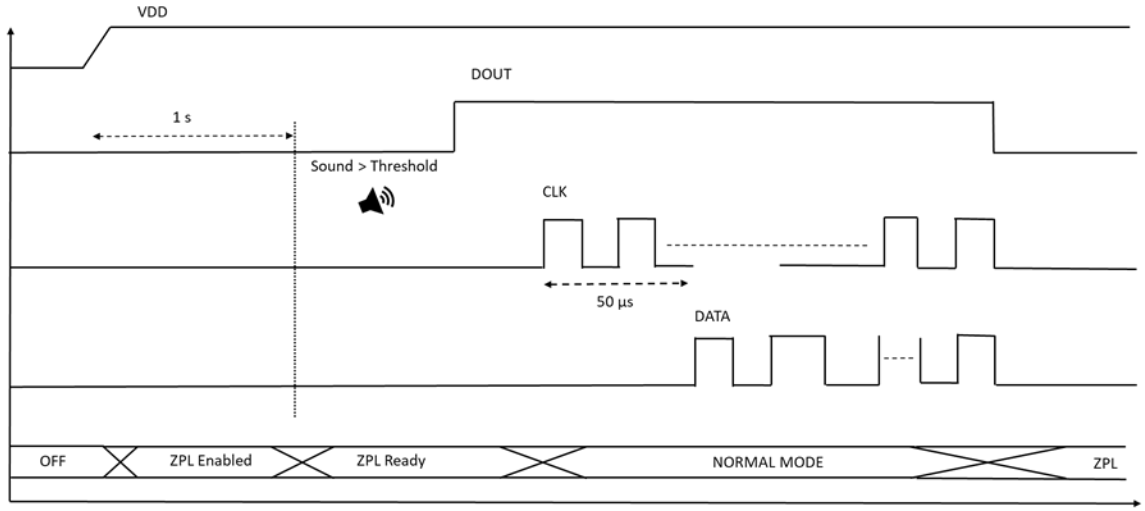
MICROPHONE STATE DIAGRAM

The state diagram below shows the different modes and the associated current consumption.



VM3011 State Diagram

POWER UP SEQUENCE



VM3011 Power-up Sequence

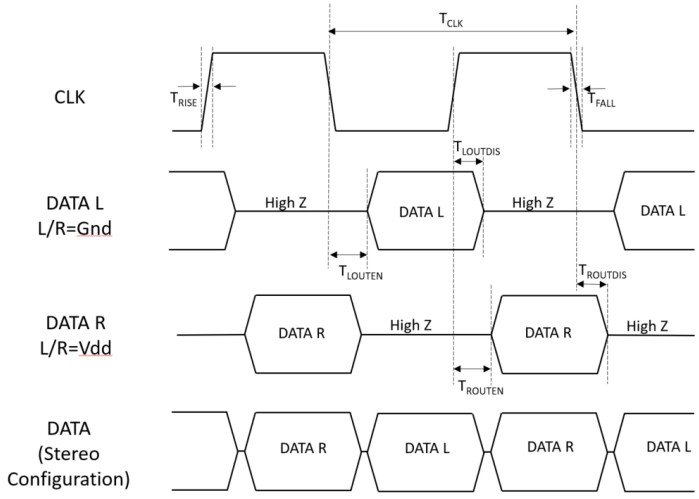
The power-up sequence of VM3011 is shown above. Upon chip power-up, Wake-on-sound mode will be entered if no MIC Clock is present. For the first 1s after power-up, the DOUT output will be blanked to allow the ZPL circuitry to power up correctly and settle. After this initial 1s, the DOUT pin will be free to toggle.

When MIC Clock is applied at a frequency great enough to enter a valid microphone mode, the microphone will power up into that mode. The ZPL lineup will continue to function during normal mode.

A DOUT pin event is not required to enter one of the microphone modes, anytime the MIC clock is applied, at a valid frequency, the part will transition into that mode.

When the incoming sound exceeds the ZPL threshold, the microphone wakes up the rest of the system, and the voice processor will send a CLK signal to switch the microphone to normal mode. By default, when the DMIC Clock first starts up in normal mode, PDM output will toggle high and low with a 50% duty cycle within 50us after the clock is applied. This mechanism will prevent any pop noises in the PDM audio stream during startup. The microphone will then seamlessly switch over to a PDM stream. The PDM data will reach +/- 0.5 dB Sensitivity within 200µs.

TIMING SPECIFICATIONS



Timing Diagram for CLK, DATA L, DATA R in Stereo Configuration

Parameter	Conditions	Min.	Typ.	Max.	Units
T_{CLK}	CLK period	303		3636	nS
T_{RISE}	CLK Rise Time (10%-90% level)			25	nS
T_{FALL}	CLK Fall Time (90%-10% level)			25	nS
T_{LOUTEN}	DATA L driven after falling CLK edge	31	48	80	nS
$T_{LOUTDIS}$	DATA L disabled after rising CLK edge	9	17	30	nS
T_{ROUTEN}	DATA R driven after rising CLK edge	31	48	80	nS
$T_{ROUTDIS}$	DATA R disabled after falling CLK edge	9	17	30	nS

Timing Data for CLK, DATA L, DATA R in Stereo Configuration

ELECTRICAL SPECIFICATION FOR I/O STAGES AND BUS LINES

Parameter	Symbol	Conditions	Standard mode		Fast mode		Fast mode plus		Units
			Min	Max	Min	Max	Min	Max	
LOW-level input voltage [1]	V_{IL}		-0.5	0.3 V_{DD}	-0.5	0.3 V_{DD}	-0.5	0.3 V_{DD}	V
LOW-level input voltage [1]	V_{IH}		0.7 V_{DD}	[2]	0.7 V_{DD}	[2]	0.7 V_{DD} [1]	[2]	V
Hysteresis of Schmitt trigger inputs	V_{hys}				0.05 V_{DD}		0.05 V_{DD}		V
LOW-level output voltage 1	V_{OL1}	(open-drain or open-collector) at 3mA sink current; V_{DD}>2V	0	0.4	0	0.4	0	0.4	V
LOW-level output voltage 2	V_{OL2}	(open-drain or open-collector) at 2mA sink current [3]; V_{DD}<=2V			0	0.2 V_{DD}	0	0.2 V_{DD}	V
LOW-level output current	I_{OL}	V_{OL} = 0.4 V	3		3		20		mA
		V_{OL} = 0.6 V [4]			6				mA
Output fall time from V_{IHmin} to V_{ILmax}	t_{Of}			250 [5]	20 x (V_{DD} / 5.5 V) [6]	250 [5]	20 x (V_{DD} / 5.5 V) [6]	120 [7]	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}				0	50 [8]	0	50 [8]	ns
Input current each I/O pin	I_i	0.1V_{DD} < V_I < 0.9V_{DDmax}	-10	+10	-10[9]	+10 [9]	-10[9]	+10 [9]	µA
Capacitance for each I/O pin [10]	C_i			10		10		10	pF

Characteristics of the SDA and SCL I/O Stages

[1] Some legacy Standard-mode devices had fixed input levels of V_{IL} = 1.5 V and V_{IH} = 3.0 V. Refer to component datasheets.
[2] Maximum V_{IH} = $V_{DD(max)}$ + 0.5 V or 5.5 V, whichever is lower. See component datasheets.
[3] The same resistor value to drive 3 mA at 3.0 V V_{DD} provides the same RC time constant when using <2 V V_{DD} with a smaller current draw.
[4] To drive a full bus load at 400 kHz, 6 mA I_{OL} is required at 0.6 V V_{OL}. Parts not meeting this specification can still function, but not at 400 kHz and 400 pF.
[5] The maximum t_f for the SDA and SCL bus lines quoted in the table below (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_s) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
[6] Necessary to be backward compatible with Fast mode.
[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
[8] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
[9] If V_{DD} is switched off, I/O pins of Fast-mode and Fast-mode Plus devices must not obstruct the SDA and SCL lines.
[10] Special purpose devices such as multiplexers and switches may exceed this capacitance because they connect multiple paths together.

Parameter	Symbol	Conditions	Standard mode		Fast mode		Fast mode plus		Units
			Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		0	100	0	400	0	1000	kHz
hold time (repeated) START condition	$t_{HD;STA}$	After this period, the first clock pulse is generated	4.0		0.6		0.26		µS
LOW period of the SCL clock	t_{LOW}		4.7		1.3		0.5		µS
HIGH period of the SCL clock	t_{HIGH}		4.0		0.6		0.26		µS
set-up time for a repeated START	$t_{SU;STA}$		4.7		0.6		0.26		µS
data hold time [2]	$t_{HD;DAT}$	CBUS compatible masters	5.0						µS
		I2C bus devices	0 [3]	[4]	0 [3]	[4]	0		µS
data set-up time	$t_{SU;DAT}$		250		100 [5]		50		ns
Rise time of both SDA and SCL signals	t_r			1000	20	300		120	ns
Fall time of both SDA and SCL Signals [3][6][7][8]	t_f			300	20 x (V_{DD} / 5.5V)	300	20 x (V_{DD} / 5.5V) [9]	120 [8]	ns
Set-up time for STOP condition	$t_{SU;STO}$		4.0		0.6		0.26		µS
Bus free time between a STOP and START condition	t_{BUF}		4.7		1.3		0.5		µS
Capacitive load for each bus line [10]	C_b			400		400		550	pF
Data valid time [11]	$t_{VD;DAT}$			3.45 [4]		0.9 [4]		0.45 [4]	µS
Data valid acknowledge time [12]	$t_{VD;ACK}$			3.45 [4]		0.9 [4]		0.45 [4]	µS
Noise margin at the LOW level	V_{nL}	For each connected device (including hysteresis)	0.1 V_{DD}		0.1 V_{DD}		0.1 V_{DD}		V
Noise margin at the HIGH level	V_{nH}	For each connected device (including hysteresis)	0.2 V_{DD}		0.2 V_{DD}		0.2 V_{DD}		V

Characteristics of the SDA and SCL bus lines for Standard, Fast, Fast mode plus I2C bus devices

[1] All values referred to $V_{IH(min)}$ (0.3V_{DD}) and $V_{IL(max)}$ (0.7V_{DD}) levels (see Table: Characteristics of SDA and SCL).
[2] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission, and the acknowledge.
[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[4] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
[5] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also, the acknowledge timing must meet this set-up time.
[6] If mixed with Hs-mode devices, faster fall times according to the table are allowed.
[7] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
[8] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
[9] Necessary to be backward compatible to Fast mode.

[10] The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application.
[11] $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
[12] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse)

I2C Operation

The following recommendations should be followed for using I2C to communicate with the VM3011.

1. All I2C communication should take place when the device is in ZPL mode. I2C access in normal PDM mode could lead to coupling from I2C pins to the PDM output. This could show up in the audio output as clicks when the I2C transactions are taking place.

2. If possible, a dedicated I2C port should be used for the VM3011. Sharing I2C ports with other I2C devices could results in interference in the audio output path in the normal mode when I2C communication is happening with other devices.

I2C Addresses

The VM3011 has two selectable I2C addresses. When LR Select is connected to GND, the I2C address is 0x60. When LR Select is connected to Vdd, the I2C address is 0x61.

I2C Registers

The I2C Registers below are user-programmable by setting the appropriate register settings.

Values in parenthesis indicate the default settings for I2C registers shipped with the device. These default values can be read back from the device using I2C readback.

Feature	Address	B7	B6	B5	B4	B3	B2	B1	B0	Read/Write
I2C_Cntrl	0x0				DOUT_CLEAR (0x0)	RESERVED (0x0)	WDT_DLY (0x0)		WDT_ENABLE (0x0)	R/W
WOS_PGA_GAIN	0x1				WOS_PGA_GAIN (0x10)					R
WOS Filter	0x2					WOS_HPF (0x3)		WOS_LPF (0x0)		R/W
WOS PGA MIN THR	0x3		FAST_MODE_CNT (0x2)		WOS_PGA_MIN_THR (0x0)					R/W
WOS PGA MAX THR	0x4			WOS_RMS (0x0)	WOS_PGA_MAX_THR (0x1B)					R/W
WOS THRESH	0x5						WOS_THRESH (0x7)			R/W

User Programmable I2C Registers

I2C User Programmable Registers in VM3011

DOUT_CLEAR: when set to 1, DOUT pin will be reset to LOW. This is another way to reset the ZPL mode to look for acoustic trigger without toggling the PDM clock.

WDT_Delay: In the rare case when the host stops toggling the SCL clock in the middle of an I2C transaction, I2C interface has a Watch Dog Timer to reset the I2C logic. By default, the timer is reset and disabled upon detection of an end of an I2C transaction. If the timer exceeds the time controlled by the WDT_DLY bits, then the entire I2C logic is reset (the registers and all other logic on VM3011 are not affected). **WDT_Delay** register Sets the watchdog time delay.

WDT_DLY	Watchdog Timer Delay (ms)
00	8
01	16
10	32
11	64

WDT_Enable: The Watchdog Timer can be disabled by setting the WDT_ENABLE bit low.

Programmable Gain Amplifier gain (WOS_PGA_GAIN) is automatically adjusted by the feedback loop, as described above. Gain value can be read back using I2C register to monitor the ambient sound level while in Adaptive ZPL mode. The table below shows the translation between SPL levels and PGA gain.

Ambient Sound Engine enables ambient noise level detection in applications such as Smartwatch, hearables, etc. where the background noise has to be monitored constantly to identify safe hearing levels. The device can get the PGA_GAIN register value from I2C and use the lookup table below to measure the ambient noise level. The microphone can still operate in ZPL mode during this readback process.

Threshold (dB-SPL)	PGA_GAIN [4:0]	Threshold (dB-SPL)	PGA_GAIN [4:0]
91.5	00000	**67.5**	10000
90	00001	**66**	10001
88.5	00010	**64.5**	10010
87	00011	**63**	10011
85.5	00100	**61.5**	10100
84	00101	**60**	10101
82.5	00110	**58.5**	10110
81	00111	**57**	10111
79.5	01000	**55.5**	11000
78	01001	**54**	11001
76.5	01010	**52.5**	11010
75	01011	**51**	11011
73.5	01100	**49.5**	11100
72	01101	**48**	11101
70.5	01110	**46.5**	11110
68	01111	**45**	11111

Acoustic Threshold / Gain Correlation (Address 0x0, Bitfield: [4:0])

Band Pass Filter (BPF) can be programmed via I2C to adjust the lower and upper frequency between which the device will wake up. The corner frequency settings supported by WOS_LPF and WOS_HPF register bits are below

WOS_LPF	Corner Frequency (kHz)
00	2
01	4
10	6
11	8

Low-pass Filter Corners (Address 0x2, Bitfield: [1:0])

WOS_HPF	Corner Frequency (Hz)
00	200
01	300
10	400
11	800

High-pass Filter Corners (Address 0x2, Bitfield: [3:2])

FAST_MODE_COUNT can be programmed to increase the speed at which the ZPL feedback loop adapts to a large change in background noise. The FAST MODE is triggered according to the FAST_MODE_CNT setting described in the table below. For example, when FAST_MODE_CNT[1:0]=01, if the PGA Gain is incremented two times in a row or decremented two times in a row, the FAST MODE will engage.

FAST_MODE_CNT[1:0]	Description
00	Fast mode disabled
01	If two window comparator trips in a row in the same direction, the clocks are sped up 16x
10	If four window comparator trips in a row in the same direction, the clocks are sped up 16x
11	If six window comparator trips in a row in the same direction, the clocks are sped up 16x

Adaptive Loop Fast Start Count (Address 0x3, Bitfield: [6:5])

WOS_RMS can be set to Low/High to switch the sampling interval of the comparator signal between 1 seconds and 0.5 seconds. This effectively changes the low pass corner frequency from 1Hz to 2Hz.

WOS_RMS	Comparator Sampling Interval (seconds)
Low	1
High	0.5

Adaptive Loop Update Frequency (Address 0x4, Bitfield: [5])

Max_PGA_Gain and **Min_PGA_Gain** limits are the maximum and minimum allowable gains of the WoS PGA, which define the boundary for the control loop. The PGA Gain would not go higher or lower than the values set in the registers when the ZPL adaptive threshold is being tracked. The bitfields on these registers can be set to any value between '0000' and '11111' corresponding to threshold range between 45 - 91.5 dBSPL as per the Table given in WOS_PGA_GAIN register above.

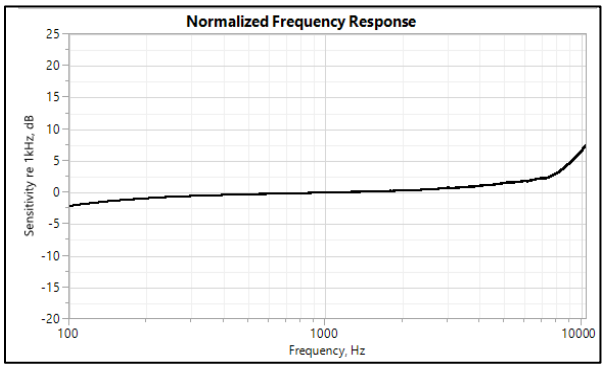
WOS_THRESH can be used to program the margin to the threshold from 6 dBSPL to 18 dBSPL. The table below outlines the different DOUT threshold values available. Essentially, this programs the amount of margin above the average acoustic input level that is needed to trip the DOUT comparator. For example, a code of 100 for WOS_THRESH will program the microphone to trigger at a level 5x above the average acoustic noise level.

WOS_THRESH	Threshold (dBSPL)	Trigger input level rel. to average acoustic noise level
000 (Reserved)	N/A	See note below
001	6.0	2x
010	9.5	3x
011	12.0	4x
100	14.0	5x
101	15.5	6x
110	16.9	7x
111	18.0	8x

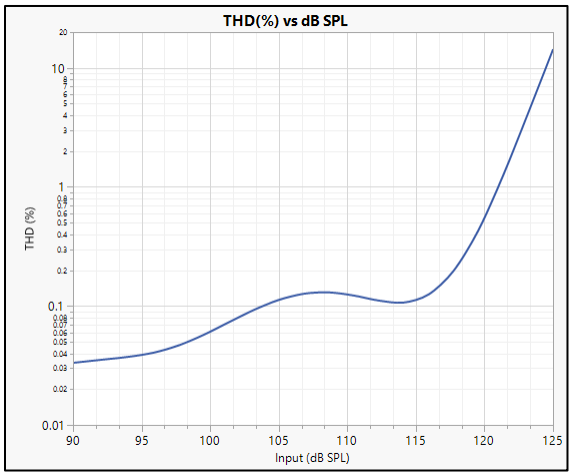
Dout Comparator Threshold Programmable Values

Note: WOS_THRESH value of 000 is not recommended for VM3011. This setting corresponds to the RMS level of the background acoustic noise. Therefore, DOUT will trip all the time just from fluctuations in input audio amplitude, and the microphone will trigger consistently.

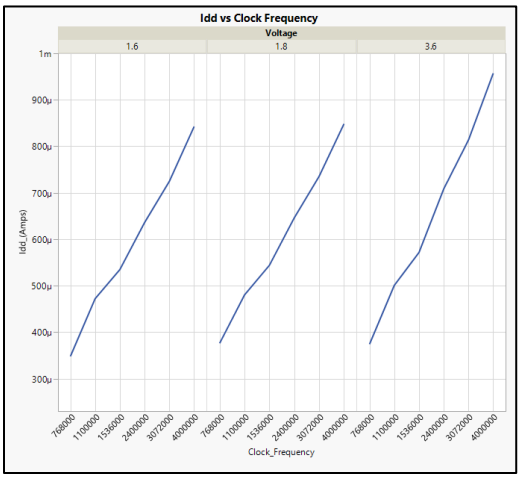
TYPICAL PERFORMANCE CHARACTERISTICS



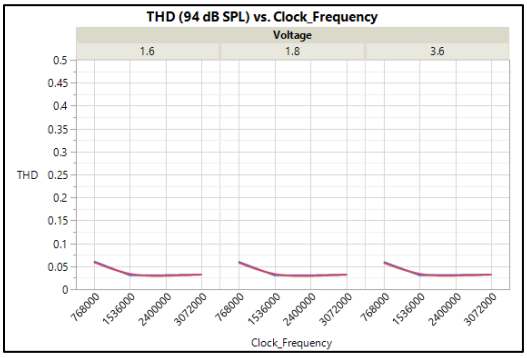
a. Normalized Frequency Response



b. THD (%) vs dB SPL



c. Idd vs Clock over Vdd



d. THD vs Clock Rate over Vdd

SOLDER REFLOW PROFILE

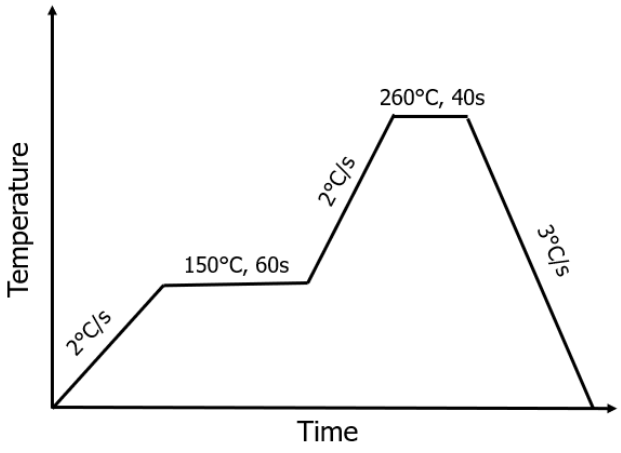


Figure 6: Solder Reflow Profile

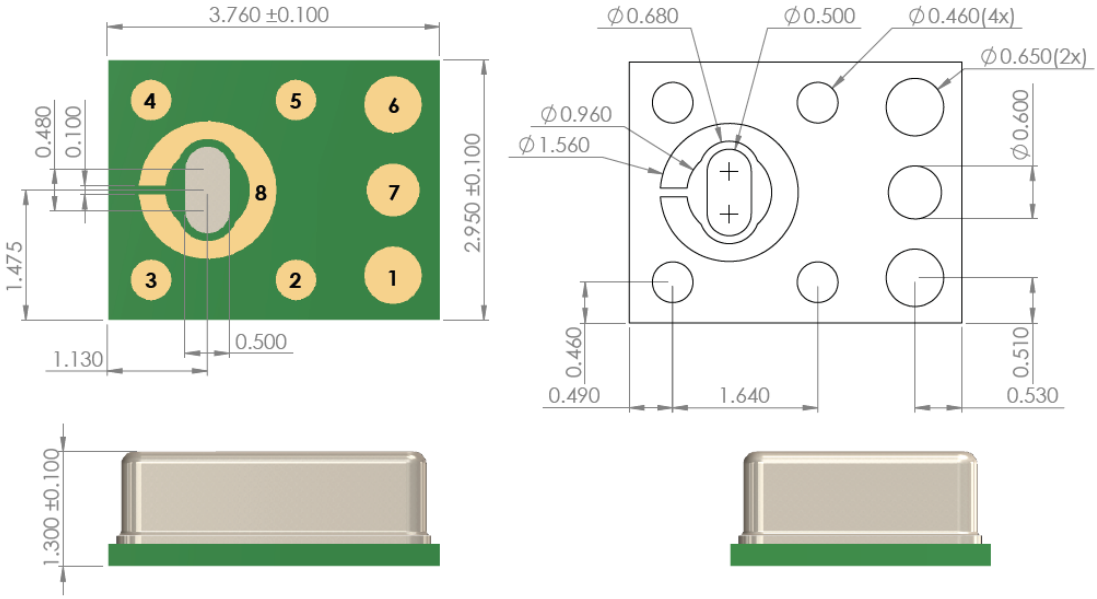
HANDLING INSTRUCTIONS

The Piezo MEMS microphone is very robust to harsh environments such as dust and moisture. However, to avoid mechanical damage to the mic, we recommend using appropriate handling procedures when manually handling the parts or when using pick and place equipment. The following guidelines will avoid damage:

- Do not apply a vacuum to the bottom side of the microphone. A vacuum pen may be used with care on the top side only.
- Do not apply very high air pressure over the port hole.
- Do not insert any large particles or objects in the port hole. The microphone is robust to small particles per IP5x specification.
- Do not board wash or clean after the reflow process or expose the acoustic port to harsh chemicals.

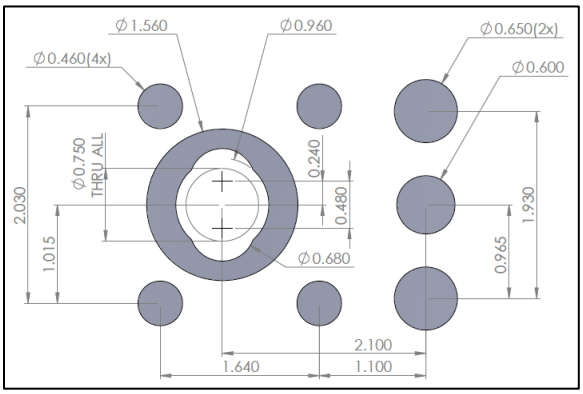
Please refer to this Application Note for Microphone Assembly Guidelines.

DIMENSIONS AND PIN LAYOUT

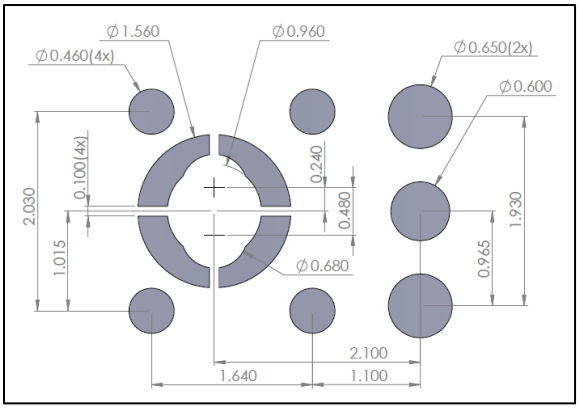


Pin Number	Pin Name	Description
1	DATA	PDM Digital Output
2	SDA	I2C Data (Threshold Control)
3	DOUT	Dout (ZPL Flag)
4	SCL	I2C CLK (Threshold Control)
5	CLK	PDM Clock Input
6	VDD	Power Supply
7	L/R SELECT	Left/Right Channel Select
8	GND	Ground

PCB DESIGN AND LAND PATTERN LAYOUT

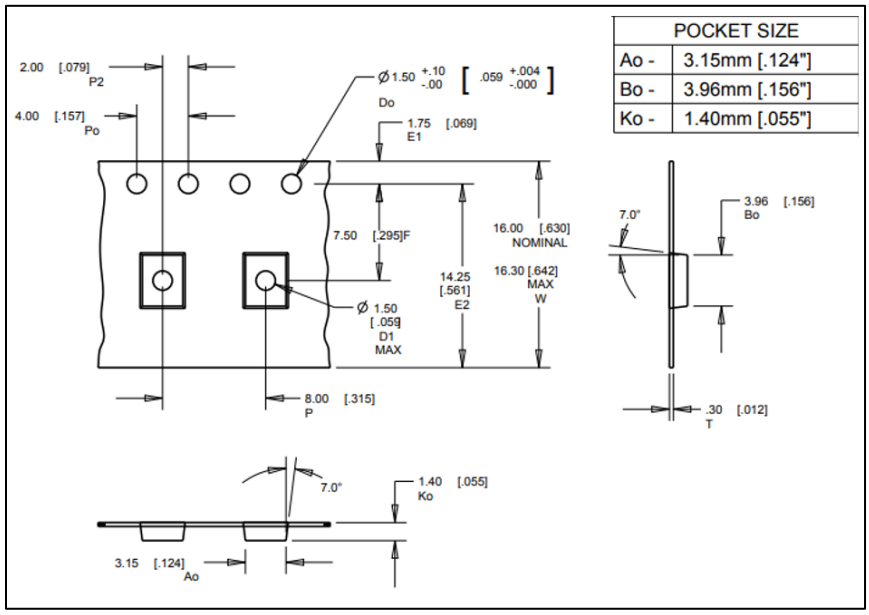


PCB Land Pattern – All dimensions are in mm

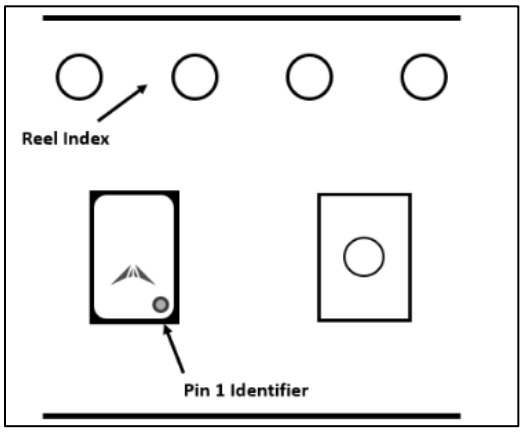


Solder Stencil Pattern – All dimensions are in mm

TAPE AND REEL SPECIFICATIONS

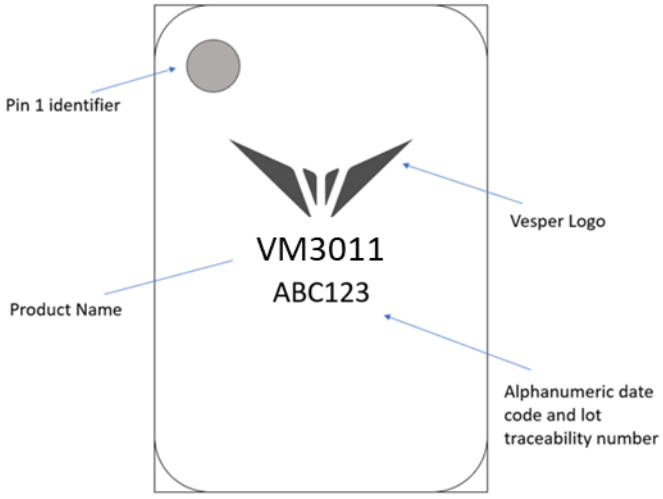


Tape and Reel specification - All dimensions in millimeters



Part Orientation in Reel (Note: Dimensions not to scale)

LID MARKING



Lid Marking Description

SUPPORTING DOCUMENTS

AN9 – Introduction to Digital Adaptive ZeroPower Listening™ Microphone

VM3011_Coupon_PCB_UserGuide - Vesper VM3011 Coupon PCB board user guide

VM3011_3D_Model – Vesper VM3011 3D CAD Layout

AN3 – Vesper Piezoelectric MEMS Microphone Assembly Guidelines

COMPLIANCE INFORMATION

Electrostatic discharge (ESD) sensitive device:
Although this product features industry-standard protection circuitry, damage may occur if subjected to excessive ESD. Proper ESD precautions should be taken to avoid damage to the device.

CONTACT DETAILS

Vesper Technologies
77 Summer St Floor 8
Boston, MA 02110
Email: info@vespermems.com

LEGAL INFORMATION

For any questions or comments on the datasheet email: erratum@vespermems.com

REVISION HISTORY

Revision	Date	Description
0.0.0	12/20/2019	Initial Revision
0.0.1	12/26/2019	Added section "Notes for Engineering Samples" after table of contents
0.0.2	1/20/2020	Updated package diagram Updated details on WDT_Delay and I2C Watchdog timer Added electrical specification of I/O stage and bus line
0.0.3	4/3/2020	Added description of feature "Ambient Sound Engine" including PGA Gain to SPL translation table Added power-up sequence Updated layout, PCB and Stencil pattern drawings Updated header and footer to new style
0.0.4	4/29/2020	Updated recommended PCB port hole shape from slot to 0.75mm round port hole
0.0.5	05/20/2020	Updated Standby Mode Data Output
0.0.6	07/06/2020	Renamed DOUT_RAW to Reserved Added DOUT_CLEAR bit Removed Note for Engineering Samples Updated PSRR Added section on I2C Operation
0.0.7	07/20/2020	Updated Power Consumption Values
0.0.8	07/30/2020	Updated Application Circuit Diagram

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