32V;1.5μA I_Q,150mA Low Dropout Voltage Regulator

Features

- Low Quiescent Current：1.5μA
- High Input Voltage： Up to 32V
- High Output Current：≥150mA
- Dropout Voltage：
  300mV@100mA（3.3V）
- VT7133B ±2 % Output Accuracy
  VT7133A ±1 % Output Accuracy
- High-accuracy Output Voltage
- Good Transient Response
- Integrated Short-Circuit Protection
- Integrated Thermal Protection
- Over-Temperature Protection
- Support Fixed Output Voltage：
  1.8, 2.5, 3.0, 3.3, 3.6，4.0，4.2 and 5.0V
- Available Package:
  SOT23-3L、SOT89-3L

Applications

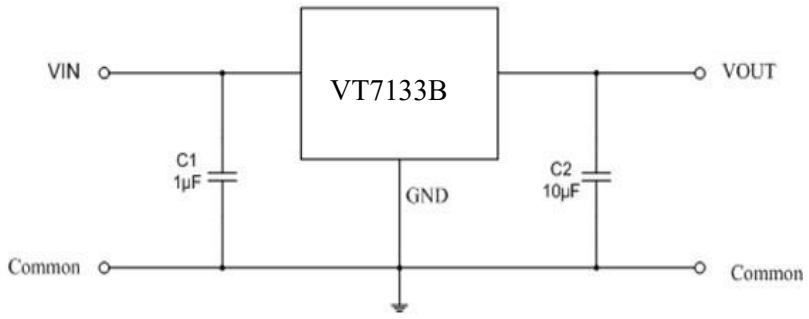
- Portable, Battery Powered Equipment
- Battery-powered equipment
- Smoke detector and sensor
- Audio/Video Equipment
- Weighting Scales
- Home Automation

General Description

The VT7133 series is a high voltage， ultralow-power， low dropout voltage regulator. The device can deliver 100mA output current with a dropout voltage of 300mV and allows an input voltage as high as 32V. The typical quiescent current is only 1.5μA.

The device is available in fixed output voltages of 1.8, 2.5, 3.0, 3.3, 3.6, 4.0, 4.2 and 5.0V.The device features integrated short-circuit and thermal shutdown protection.Although designed primarily as fixed voltage regulators, the device can be used with external components to obtain variable voltages.

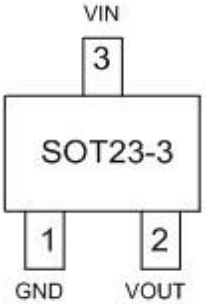
Application Circuits



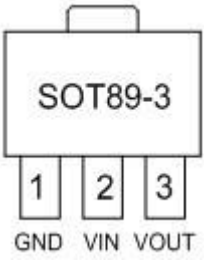
Typical Application Circuit for VT7133

32V;1.5μA I_Q,150mA Low Dropout Voltage Regulator

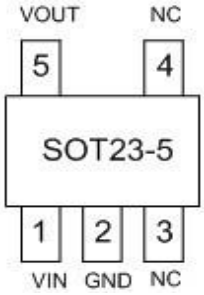
Pin Configuration (Routine)



SOT23-3L



SOT89-3L



SOT23-5L

Pin Description

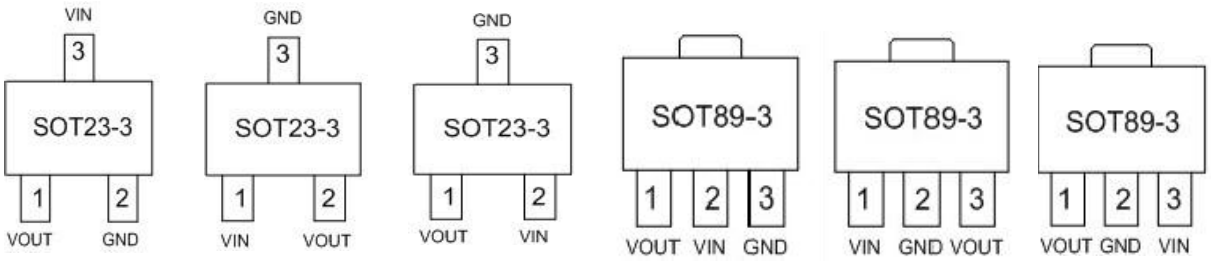
Pin No.			Pin Name	Pin Function
SOT89-3L	SOT23-3L	SOT23-5L		
1	1	2	GND	Ground.
2	3	1	VIN	Supply voltage input
3	2	5	VOUT	Output of the regulator.
-----	-----	3、4	NC	No Internal Connection.

Order Information

VT7133 ①②-③④⑤

Designator	Symbol	Description
①②	S5\S3\P3	SOT23-5L\SOT23-3L\SOT89-3L
③④	Integer	Output Voltage(18, 25, 30, 33, 36,40,42, 50)
⑤	A	±1 % Output Accuracy
	B	±2 % Output Accuracy

Packages and Pin Assignment (Customized)



SA **SB** **SC** **PA** **PB** **PC**

32V;1.5μA I_Q,150mA Low Dropout Voltage Regulator

Marking Information:

Represents product series

Mark	Product Series
AF	VT7133

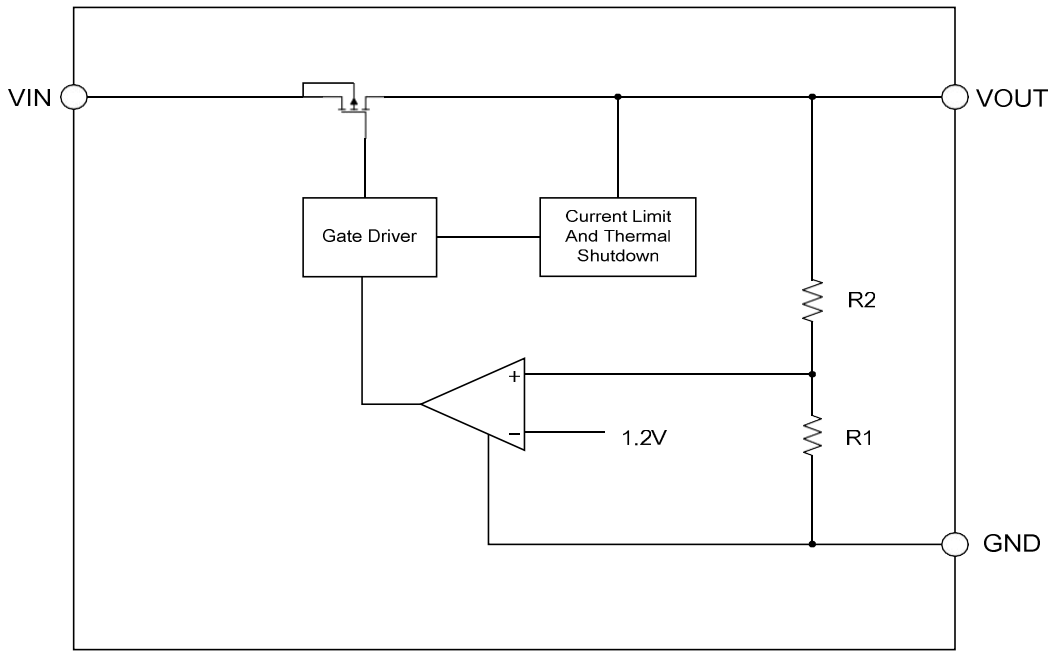
Represents output Voltage

Mark	Output Voltage(V)				Mark	Output Voltage(V)			
18	-	1.8	-		36		3.6		
25	-	2.5	-		40		4.0		
30	-	3.0	-		42		4.2		
33	-	3.3	-		50		5.0		

Represents type of regulator

Mark		Product Series
±1 % Output Accuracy	±2 % Output Accuracy	VT7133
A	B	

Functional Block Diagram



32V;1.5μA I_Q,150mA Low Dropout Voltage Regulator

Absolute Maximum Ratings

Item	Description	Min	Max	Unit
Voltage	VIN Pin to GND Pin	-0.3	32	V
	VOUT Pin to GND pin	-0.3	6	V
	VOUT Pin to VIN Pin	-35	0.3	V
Current	Peak output	Internally limited		
Temperature	Operating Ambient Temperature	-40	85	℃
	Storage Temperature	-40	150	℃
	Operating virtual junction Temperature	-	150	℃
Thermal Resistance (Junction to Ambient)	SOT89	180		℃/W
	SOT23-3	380		℃/W
	SOT23-5	300		℃/W
Power Dissipation	SOT89	600		mW
	SOT23-3	300		mW
	SOT23-5	400		mW
Electrostatic discharge rating	Human Body Model（HBM）	4		kV
	Charged Device Model（MM）	100		V

Note： Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

32V;1.5μA I_Q,150mA Low Dropout Voltage Regulator

Electrical characteristics （At TA=25°C, CIN=1uF, VIN=VOUTNOM+1.0V, COUT=10μF, unless otherwise noted）

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage		—	—	36	V
I_{GND}	Quiescent Current	VIN=12V, No load	—	1.3	1.5	μA
V_{OUT} (VT7133)	Output Voltage	VIN=12V, I_{OUT} =10mA	-2%		2%	VOUT
I_{OUT_MAX}	Output Current		150	20	—	mA
V_{DROP}	Dropout Voltage*1 (VT7133-50)	I_{OUT}=10mA , ΔV_{OUT}= - V_{OUTNOM}*2%	—	45	—	mV
		I_{OUT}=100mA , ΔV_{OUT}= - V_{OUTNOM}*2%	—	30	—	mV
		I_{OUT}=200mA , ΔV_{OUT}= - V_{OUTNOM}*2%	—	500	—	mV
	Dropout Voltage*1 (VT7133-33)	I_{OUT}=100mA , ΔV_{OUT}= - V_{OUTNOM}*2%	—	30	—	mV
		I_{OUT}=100mA , ΔV_{OUT}= - V_{OUTNOM}*2%	—	300	—	mV
		I_{OUT}=200mA , ΔV_{OUT}= - V_{OUTNOM}*2%	—	500	—	mV
ΔV_{OUT}	Load Regulation	1mA≤I_{OUT}≤100mA	—	20	—	mV
ΔV_{OUT} x100/ ΔV_{IN} x V_{OUT}	Line Regulation	I_{OUT}=1mA, V_{IN}=(V_{OUTNOM}+1V) to 35V	—	0.2	—	%/V
I_{LIMIT}	Current Limit	V_{IN}=(V_{OUTNOM}+1V) to 35V R_{LOAD}=V_{OUTNOM}/1A	—	450	—	mA
T_{SHDN}	Thermal Shutdown Threshold		—	125	—	℃

Note：*1 Dropout Voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.

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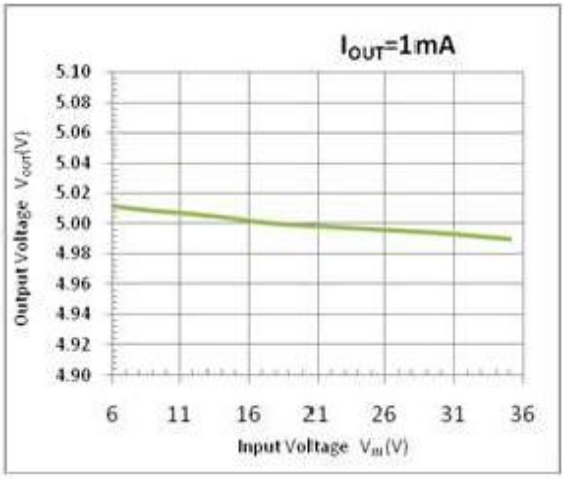
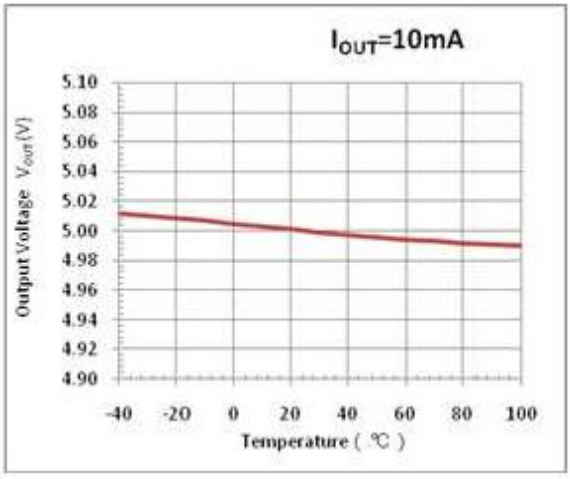
Typical Performance Characteristics:

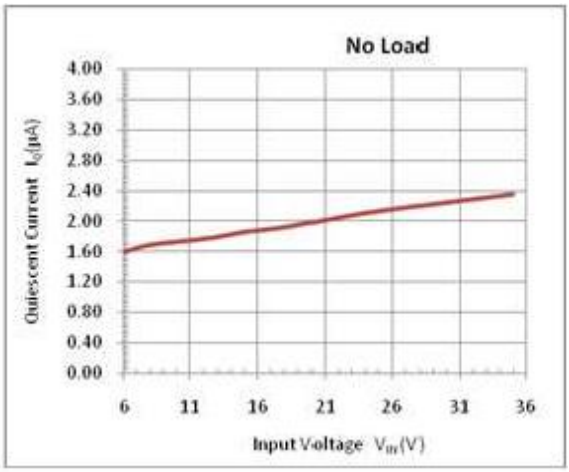
Condition: TA=25°C, VIN=VOUTNOM+1.0 V,IOUT=1mA, COUT=10uF, unless otherwise noted.



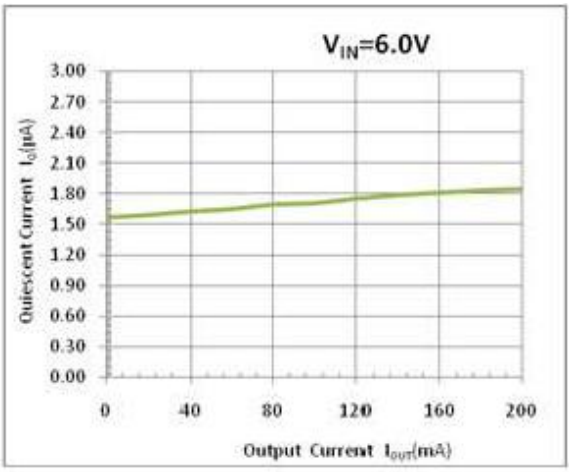
Output Voltage vs. Input Voltage



Output Voltage vs. Temperature

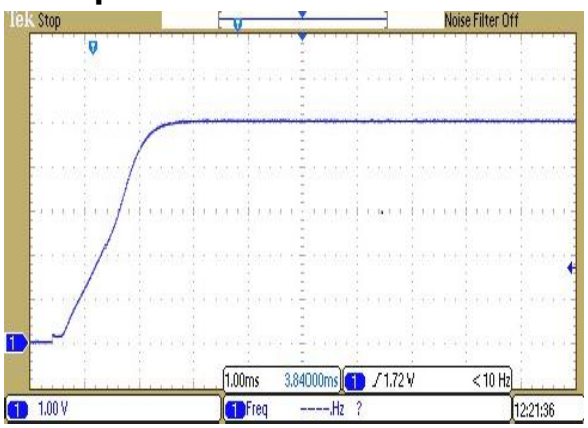


Quiescent Current vs. Input Voltage

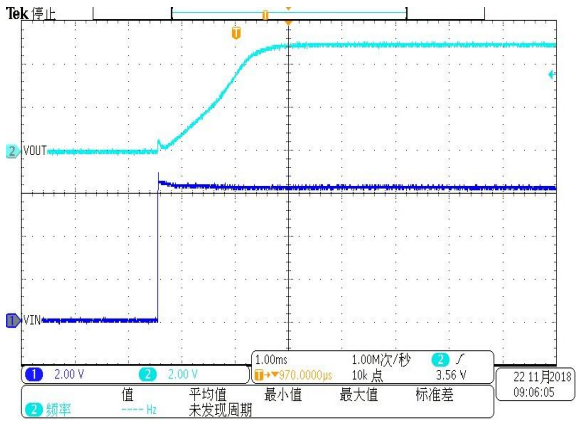


Quiescent Current vs. Output Current

Startup:



V_{IN}=6.0V， No Load， C_{OUT}=10uF



V_{IN}=6.0V， I_{OUT}=30mA， C_{OUT}=10uF

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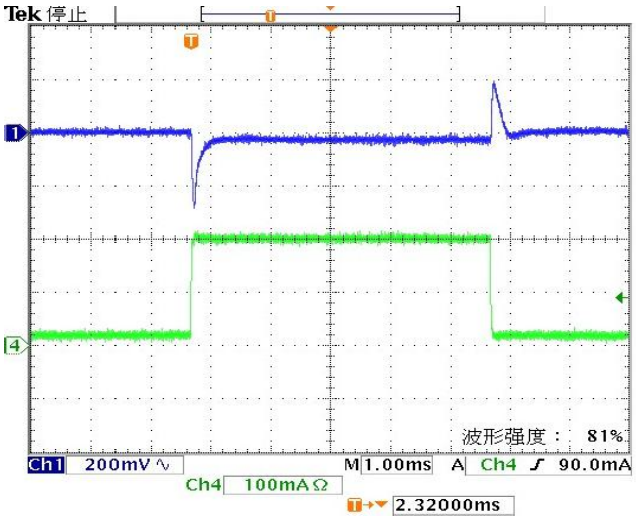
Transient Response

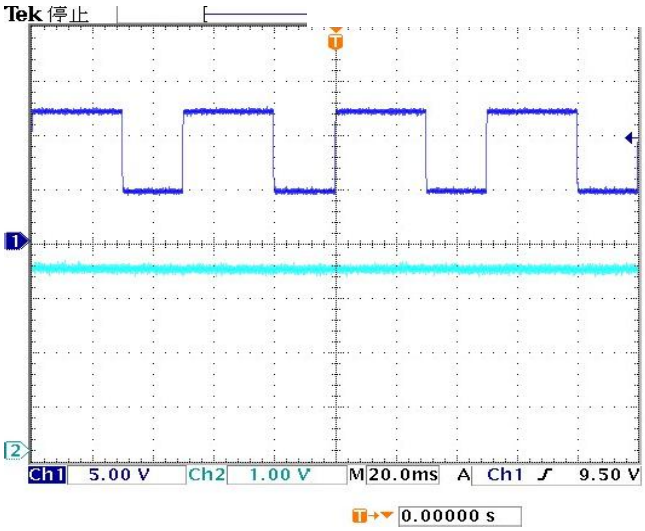
Load Transient

V_{IN}=12.0V, C_{OUT}=10uF, I_{OUT}=10mA to 200mA



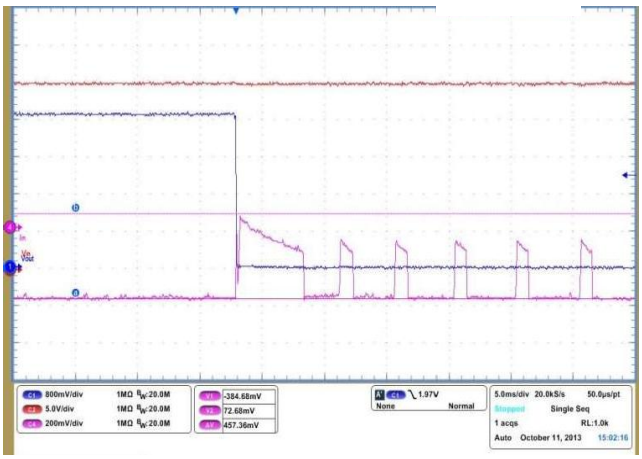
Line Transient

V_{IN}=5.0V to 12.0V, C_{OUT}=10uF, I_{OUT}=1mA

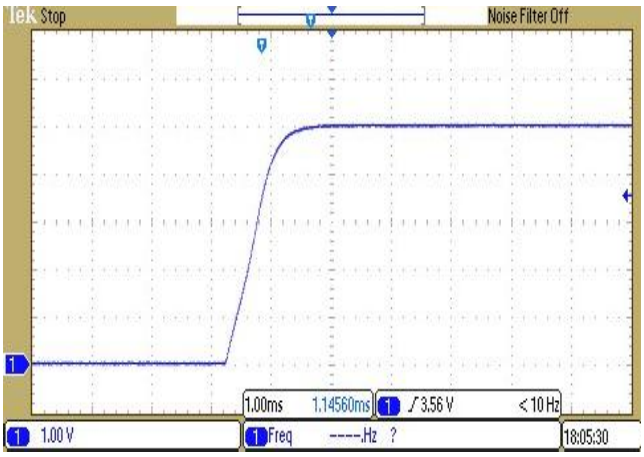


Short Protection

V_{IN}=25.0V， Short Protection Occurred



V_{IN}=25.0V， Short Protection Removed



Application Guideline

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between V_{DD} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 10μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage VDROP also can be expressed as the voltage drop on the pass-FET at specific output current (IRATED) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized asan resistance RDS(ON). Thus the dropout voltage can bedefined as ($V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$). Fornormal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DROP}$) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below: TA=25°C, PCB,

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

PD = (VIN – VOUT) × IOUT

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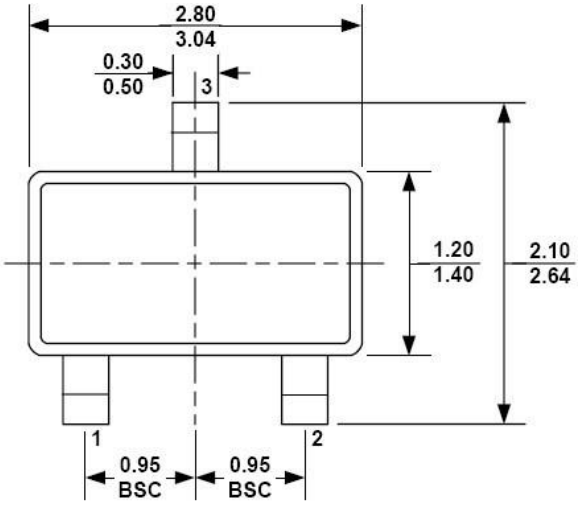
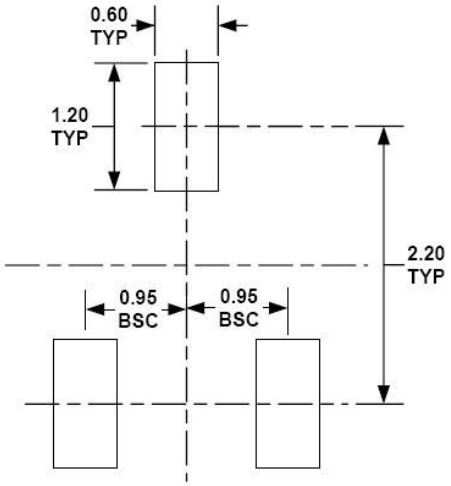
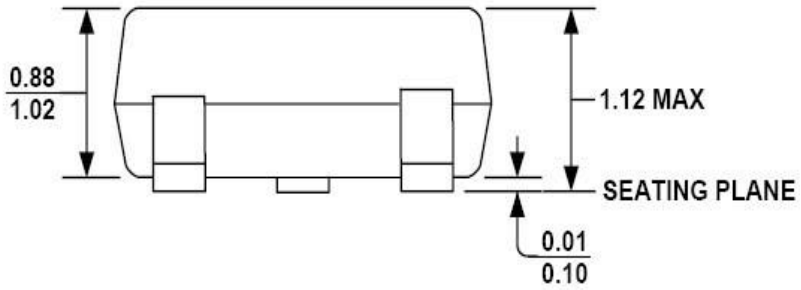
Packaging Information SOT23-3L



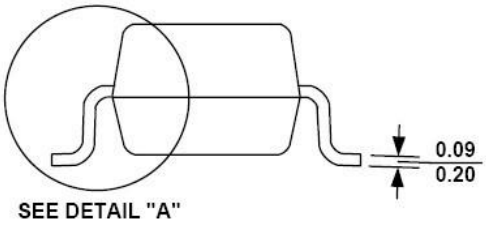
TOP VIEW



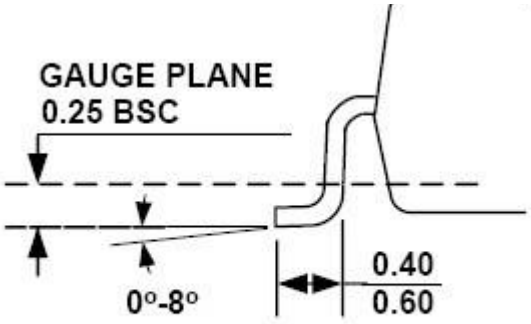
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



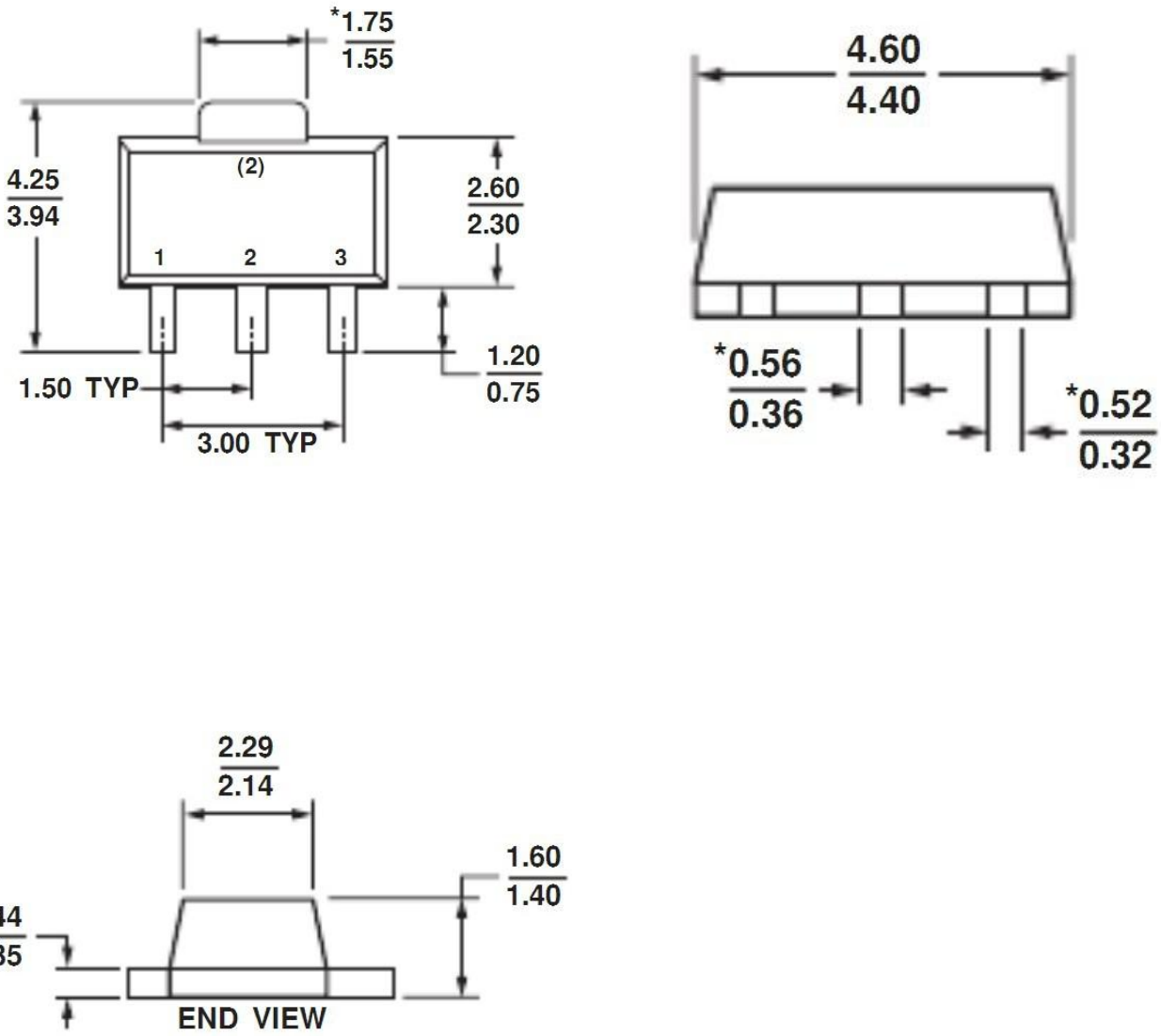
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC TO-236, VARIATION AB.
6) DRAWING IS NOT TO SCALE.

32V;1.5μA I_Q,150mA Low Dropout Voltage Regulator

Packaging Information SOT89-3L



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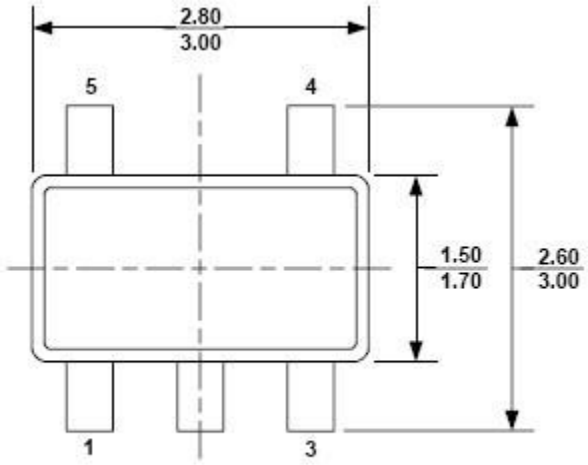
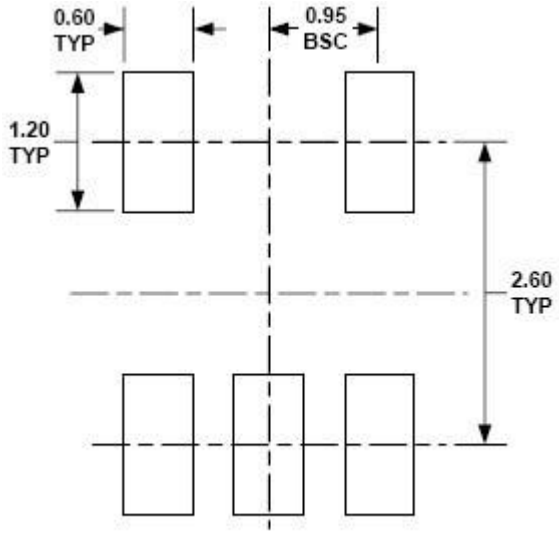
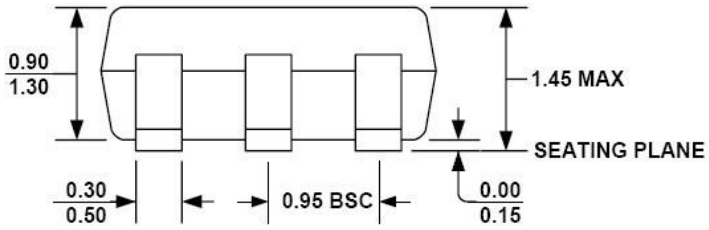
Packaging Information SOT23-5L



TOP VIEW



RECOMMENDED LAND PATTERN



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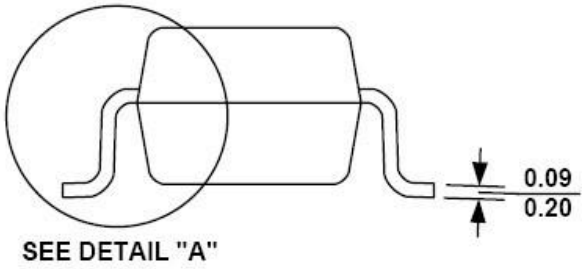
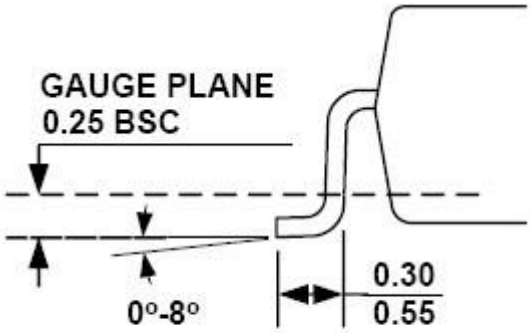


SIDE VIEW



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