# VICOR

## IBC Module
## IB0xxQ120T60xx-xx

c UL us · RoHS · c TÜV NRTL us · CE

## 4:1 Intermediate Bus Converter Module: Up to 760W Output



Size:
2.30 x 1.45 x 0.42in
58.4 x 36.8 x 10.6mm

### Features & Benefits

- Input: 36 – 60$V_{DC}$
  (38 – 55$V_{DC}$ for IB048x)

- Output: 12.0$V_{DC}$ at 48$V_{IN}$

- Output current up to 60A

- Output power: up to 760W *

- 2250$V_{DC}$ isolation
  (1500$V_{DC}$ isolation for IB048x)

- 98.0% peak efficiency

- Low profile: 0.42" height above board

- Industry standard 1/4 Brick pinout

- Sine Amplitude Converter™ (SAC™)

- Low noise 1MHz ZVS/ZCS

* Lower power models available

### Typical Applications

- Enterprise networks
- Optical access networks
- Storage networks
- Automated test equipment

### Product Description

The Intermediate Bus Converter (IBC) Module is a very efficient, low profile, isolated, fixed ratio converter for power system applications in enterprise and optical access networks.
Rated at up to 520W from 36$V_{IN}$ and up to 760W from 50 to 60$V_{IN}$, the IBC conforms to an industry standard quarter-brick footprint while supplying power greatly exceeding competitive quarter-bricks. Its leading efficiency enables full load operation at 45°C with only 400LFM airflow. Its small cross section facilitates unimpeded airflow — above and below its thin body — to minimize the temperature rise of downstream components. A baseplate option is available for alternative cooling schemes.

## Part Ordering Information

| Product Function | Input Voltage | | Package | Output Voltage (Nom.) x 10 | | | Temperature Grade | Output Current | | Enable Logic | Pin Length | Options | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I | B | 0 x x | Q | 1 | 2 | 0 | T | 6 | 0 x | x | – x | x |

IB = Intermediate Bus Converter

Q = Quarter Brick Format

T = -40°C ≤ $T_{OPERATING}$ ≤ +100°C
-40°C ≤ $T_{STORAGE}$ ≤ +125°C

N = Negative
P = Positive

00 = Open frame
BP = Baseplate

048 = 38 – 55$V_{DC}$
050 = 36 – 60$V_{DC}$
054 = 36 – 60$V_{DC}$ *
* Operating transient to 75$V_{DC}$

120 = ($V_{OUT}$ nominal @ $V_{IN}$ = 48$V_{DC}$ x 10
(4:1 transfer ratio)

60 = Max Rated Output Current

1 = 0.145"
2 = 0.210"
3 = 0.180"

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## Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

| Parameter | Comments | Min | Max | Unit |
|---|---|---|---|---|
| Input voltage (+IN to –IN) | See Input Range Specific Characteristics for details | -0.5 | 75 | $V_{DC}$ |
| Input voltage slew rate | | | 5 | V / µs |
| EN to –IN | | -0.5 | 20 | $V_{DC}$ |
| Output voltage (+OUT to –OUT) | See OVP setpoint max | -0.5 | (see note) | $V_{DC}$ |
| Output current | $P_{OUT} \le 650W$ | | 60 | A |
| Dielectric withstand | | | | |
|    Input to output | 1min | 2250 1500 for IB048x | | $V_{DC}$ |
|    Output to baseplate | 1min | 707 | | |
| Temperature | | | | |
|    Operating junction | Hottest semiconductor | -40 | 125 | |
|    Operating baseplate | | -40 | 100 | °C |
|    Storage | | -55 | 125 | |

## Electrical Specifications

Specifications valid at 48$V_{IN}$, 100% rated load and 25°C ambient, unless otherwise indicated.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Input Range Specific Characteristics** | | | | | | |
| | | | | | | |
| **Part Number IB048Q120T60xx-xx** | | | | | | |
| Operating input voltage | | | 38 | 48 | 55 | $V_{DC}$ |
| Non-operating input surge withstand | | < 100ms | | | 75 | $V_{DC}$ |
| Operating input dV / dt | | | 0.003 | | 5 | V / µs |
| Undervoltage protection | | | | | | |
|    Turn–on | | | 33 | | 38 | $V_{DC}$ |
|    Turn–off | | | 31 | | 36 | $V_{DC}$ |
|    Turn–on / turn–off hysteresis | | | 2 | | | $V_{DC}$ |
|    Time constant | | | | | 7 | µs |
|    Undervoltage blanking time | | UV blanking time is enabled after start up | 50 | 100 | 200 | µs |
| Overvoltage protection | | | | | | |
|    Turn–off | | | 60 | | 64 | $V_{DC}$ |
|    Turn–on | | | 55 | | 64 | $V_{DC}$ |
|    Time constant | | | | | 4 | µs |
| DC output voltage band | | No load, over $V_{IN}$ range | 9.5 | 12.0 | 13.8 | $V_{DC}$ |
| Output OVP set point | | Module will shut down | 15.0 | | 16.0 | $V_{DC}$ |
| Dielctric withstand | | Input to output and input to baseplate; 1min | 1500 | | | $V_{DC}$ |
| | | Output to baseplate | 707 | | | |
| Insulation resistance | | Input to output | | | 30 | MΩ |

## Electrical Specifications (Cont.)

Specifications valid at $48V_{IN}$, 100% rated load and 25°C ambient, unless otherwise indicated.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Input Range Specific Characteristics** | | | | | | |
| | | | | | | |
| **Part Number IB050Q120T60xx-xx** | | | | | | |
| Operating input voltage | | | 36 | 48 | 60 | $V_{DC}$ |
| Non-operating input surge withstand | | < 100ms | | | 75 | $V_{DC}$ |
| Operating input dV / dt | | | 0.003 | | 5 | V / µs |
| Undervoltage protection | | | | | | |
| Turn–on | | | 31 | | 36 | $V_{DC}$ |
| Turn–off | | | 29 | | 34 | $V_{DC}$ |
| Turn–on / turn–off hysteresis | | | 2 | | | $V_{DC}$ |
| Time constant | | | | | 7 | µs |
| Undervoltage blanking time | | UV blanking time is enabled after start up | 50 | 100 | 200 | µs |
| Overvoltage protection | | | | | | |
| Turn–off | | | 65 | | 69 | $V_{DC}$ |
| Turn–on | | | 60 | | 69 | $V_{DC}$ |
| Time constant | | | | | 4 | µs |
| DC output voltage band | | No load, over $V_{IN}$ range | 9.0 | 12.0 | 15.0 | $V_{DC}$ |
| Output OVP set point | | Module will shut down | 16.2 | | 17.2 | $V_{DC}$ |
| Dielctric withstand | | Input to output and input to baseplate; 1min | 2250 | | | $V_{DC}$ |
| | | Output to baseplate | 707 | | | |
| Insulation resistance | | Input to output | | 30 | | MΩ |

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## Electrical Specifications (Cont.)

Specifications valid at 48V$_{IN}$, 100% rated load and 25°C ambient, unless otherwise indicated.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Input Range Specific Characteristics** | | | | | | |
| | | | | | | |
| **Part Number IB054Q120T60xx-xx** | | | | | | |
| Operating input voltage | | | 36 | 48 | 60 | V$_{DC}$ |
| Non-operating input surge withstand | | < 100ms | | | 75 | V$_{DC}$ |
| Operating input dV / dt | | | 0.003 | | 5 | V / µs |
| Undervoltage protection | | | | | | |
|    Turn–on | | | 31 | | 36 | V$_{DC}$ |
|    Turn–off | | | 29 | | 34 | V$_{DC}$ |
|    Turn–on / turn–off hysteresis | | | 2 | | | V$_{DC}$ |
|    Time constant | | | | | 7 | µs |
|    Undervoltage blanking time | | UV blanking time is enabled after start up | 50 | 100 | 200 | µs |
| Overvoltage protection | | | | | | |
|    Turn–off | | | 76 | | 79.5 | V$_{DC}$ |
|    Turn–on | | | 75 | | 78 | V$_{DC}$ |
|    Time constant | | | | | 4 | µs |
| DC output voltage band | | No load, over V$_{IN}$ range | 9.0 | 12.0 | 15.0 | V$_{DC}$ |
| Output OVP set point | | Module will shut down | 19 | | 19.8 | V$_{DC}$ |
| Dielctric withstand | | Input to output and input to baseplate; 1min | 2250 | | | V$_{DC}$ |
| | | Output to baseplate | 707 | | | |
| Insulation resistance | | Input to output | | 30 | | MΩ |

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## Electrical Specifications (Cont.)

Specifications valid at 48V$_{IN}$, 100% rated load and 25°C ambient, unless otherwise indicated.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| | | **Common Input Specifications** | | | | |
| Turn ON delay | | | | | | |
|    Start-up inhibit | | V$_{IN}$ reaching turn-on voltage to enable function operational, see Figure 6 | 20 | 25 | 30 | ms |
|    Turn-on delay | | Enable to 10% V$_{OUT}$; pre-applied V$_{IN}$, 0 load capacitance, see Figure 7 | | | 75 | µs |
| Output voltage rise time | | From 10% to 90% V$_{OUT}$, 10% load, 0 load capacitance | | | 75 | µs |
| Restart turn-on delay | | See page 14 for restart after EN pin disable | | | 250 | ms |
| No load power dissipation | | | | | | |
|    Enabled | | | | 3.3 | 5.5 | W |
|    Disabled | | | | 0.15 | 0.20 | W |
| Input current | | Low line, full load | | | 15.3 | A |
| Inrush current overshoot | | Using test circuit in Figure 21, 15% load, high line, see Figure 4 | | | 11.3 | A |
| Input reflected ripple current | | At max power; Using test circuit in Figure 22; see Figure 5 | | | 750 | mArms |
| Peak short circuit input current | | | | | 45 | A |
| Repetitive short circuit peak current | | | | | 25 | A |
| Internal input capacitance | | | | 17.6 | | µF |
| Internal input inductance | | | | 5 | | nH |
| Recommended external input capacitance | | 200nH maximum source inductance | 47 | | 470 | µF |

## Electrical Specifications (Cont.)

Specifications valid at 48V$_{IN}$, 100% rated load and 25ºC ambient, unless otherwise indicated.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Common Output Specifications** | | | | | | |
| Output power * | | See Figure 24 | 0 | | 760 | W |
| Output current | | P ≤ 760W | | | 60 | A |
| Output start up load | | of I$_{OUT}$ max, maximum output capacitance | | | 15 | % |
| Effective output resistance | | | | 2.4 | | mΩ |
| Line regulation (K factor) | | V$_{OUT}$ = K • V$_{IN}$ @ no load | 0.245 | 0.250 | 0.252 | |
| Current share accuracy | | Full power operation; See Parallel Operation on page 15; up to 3 units | | | 10 | % |
| Efficiency | | | | | | |
|    50% load | | See Figures 1 – 3 | 97.5 | 98.0 | | % |
|    Full load | | See Figures 1 – 3 | 97.0 | 97.3 | | % |
| Internal output inductance | | | | 1.6 | | nH |
| Internal output capacitance | | | | 75 | | µF |
| Load capacitance | | Nominal load | 0 | | 3000 | µF |
| Output voltage ripple | | 20MHz bandwidth using test circuit in Figure 23 | | 60 | 150 | mVp-p |
| Output overload protection threshold | | Of I$_{OUT}$ max, will not shut down when started into max C$_{OUT}$ and 15% load. Auto restart with duty cycle < 10% | 105 | | 150 | % |
| Overcurrent protection time constant | | | | | 1.2 | ms |
| Short circuit current response time | | | | | 1.5 | µs |
| Switching frequency | | | | 1.0 | | MHz |
| Dynamic response – load | | Load change: ±25% of I$_{OUT}$ max, Slew rate (dI/dt) = 1A/µs See Figures 11–14 | | | | |
|    V$_{OUT}$ overshoot / undershoot | | | | | 100 | mV |
|    V$_{OUT}$ response time | | | | 1 | | µs |
| Dynamic response – line | | Line step of 5V in 1µs, within V$_{IN}$ operating range. (C$_{IN}$ = 500µF, C$_O$ = 350µF) (Figure 15 illustrates similar converter response when subjected to a more severe line transient.) | | | | |
|    V$_{OUT}$ overshoot | | | | | 1.25 | V |
| Pre-bias voltage | | Unit will start up into a pre-bias voltage on the output | 0 | | 15 | V$_{DC}$ |

\* Does not exceed IPC-9592 derating guidelines. At 70ºC ambient, full power operation may exceed IPC-9592 guidelines, but does not exceed component ratings, does not activate OTP and does not compromise reliability.

## Electrical Specifications (Cont.)

Specifications valid at 48V$_{IN}$, 100% rated load and 25°C ambient, unless otherwise indicated.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Control & Interface Specifications** | | | | | | |
| Enable (negative logic) | | Referenced to –IN | | | | |
|    Module enable threshold | | | 0.8 | | | V$_{DC}$ |
|    Module enable current | | V$_{EN}$ = 0.8V | | 130 | 200 | µA |
|    Module disable threshold | | | | | 2.4 | V$_{DC}$ |
|    Modeule disable current | | V$_{EN}$ = 2.4V | | | 10 | µA |
|    Disable hysteresis | | | | 500 | | mV |
|    Enable pin open circuit voltage | | | 2.0 | 2.5 | 3.0 | V$_{DC}$ |
|    EN to –IN resistance | | Open circuit | | 35 | | kΩ |
| Enable (positive logic) | | Referenced to –IN | | | | |
|    Module enable threshold | | | 2.0 | 2.5 | 3.0 | V$_{DC}$ |
|    Module disable threshold | | | | | 1.45 | V$_{DC}$ |
|    EN source current (operating) | | V$_{EN}$ = 5V | | | 2 | mA |
|    EN voltage (operating) | | | 4.7 | 5 | 5.3 | V$_{DC}$ |
| **General Characteristics** | | | | | | |

- Conditions: T$_{CASE}$ = 25°C, 75% rated load and specified input voltage range unless otherwise specified.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MTBF | | Calculated per Telcordia SR-332, 40°C | 1.0 | | | Mhrs |
| Service life | | Calculated at 30°C | 7 | | | Years |
| Overtemperature shut down | | T$_J$ ; Converter will reset when overtemperature condition is removed | 125 | 130 | 135 | °C |
| Mechanical | | | | | | |
|   Weight | | Open frame (without baseplate) | | 1.38 / 39.1 | | oz / g |
| | | Baseplate version | | 2.25 / 63.9 | | oz / g |
|   Length | | | | 2.30 / 58.4 | | in / mm |
|   Width | | | | 1.45 / 36.8 | | in / mm |
|   Height above customer board | | Open frame version | | 0.42 / 10.6 | | in / mm |
| | | With baseplate | | 0.45 / 11.4 | | in / mm |
|   Pin solderability | | Storage life for normal solderability | | | 1 | Years |
|   Moisture sensitivity level | MSL | Not applicable, for wave soldering only | N/A | | | |
| Clearance to customer board | | From lowest component on IBC; open frame model | | 0.11 / 2.9 | | in / mm |
| | | From lowest component on IBC; baseplate model | | 0.02 / 0.6 | | in / mm |
| Altitude, operating | | Derate operating temp 1°C per 1000 feet above sea level | -500 | | 10000 | Feet |
| Relative humidity, operating | | Non condensing | 10 | | 90 | % |
| RoHS compliance | | Compatible with RoHS directive 2002/95/EC | | | | |
| Agency approvals | | UL/CSA 60950-1 | | | | cURus |
| | | UL/CSA 60950-1, EN60950-1 | | | | cTUVus |
| | | Low voltage directive (2006/95/EC) | | | | CE |

## Electrical Specifications (Cont.)

Specifications valid at 48V$_{IN}$, 100% rated load and 25ºC ambient, unless otherwise indicated.

| Environmental Qualification | | |
|---|---|---|
| • IPC-9592A, based on Class II Category 2 the following detail is applicable; pre-conditioning required. | | |
| **Test Description** | **Test Detail** | **Min. Quanity Tested** |
| 5.2.3 HALT (Highly Accelerated Life Testing) | Low temp | 3 |
| | High temp | 3 |
| | Rapid thermal cycling | 3 |
| | 6 DOF random vibration test | 3 |
| | Input voltage test | 3 |
| | Output load test | 3 |
| | Combined stresses test | 3 |
| 5.2.4 THB (Temperature Humidity Bias) | (72hr presoak required) 1000hrs – continuous bias | 30 |
| 5.2.5 HTOB (High Temperature Operating Bias) | Power cycle – On 42 minutes<br>Off 1 minute, On 1 minute, Off 1 minute, On 1 minute, Off 1 minute, On 1 minute, Off 1 minute, On 1 minute, Off 10 minutes. Alternating between maximum and minimum operating voltage every hour. | 30 |
| 5.2.6 TC (Temperature Cycling) | 700 cycles, 30 minute dwell at each extreme – 20C minimum ramp rate | 30 |
| 5.2.7 PTC (Power & Temperature Cycling) | Reference IPC-9592A | 3 |
| 5.2.8 – 5.2.13 Shock and Vibration | Random Vibration – Operating IEC 60068-2-64 (normal operation vibration) | 3 |
| | Random Vibration Non-operating (transportation) IEC 60068-2-64 | 3 |
| | Shock Operating – normal operation shock IEC 60068-2-27 | 3 |
| | Free fall – IEC 60068-2-32 | 3 |
| | Drop Test 1 full shipping container (box) | 1 |
| 5.2.14 Other Environmental Tests | 5.2.14.1 Corrosion Resistance – Not required | N / A |
| | 5.2.14.2 Dust Resistance – Unpotted class II GR-1274-CORE | 3 |
| | 5.2.14.3 SMT Attachment Reliability IPC-9701 – J-STD-002 | N / A |
| | 5.2.14.4 Through Hole solderability – J-STD-002 | 5 |
| ESD Classification Testing | HBM testing - JESD22-A114 | 3 |
| Total Quantity (estimated) | | **138** |

## Application Characteristics: Waveforms
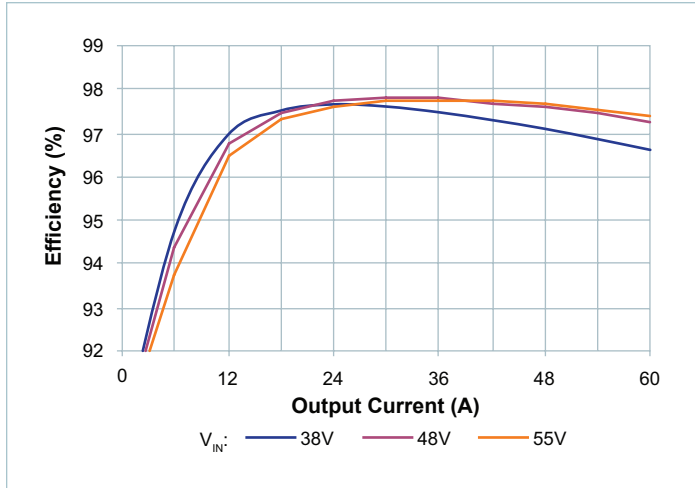


*Figure 1* — *Efficiency vs. output current, 25°C ambient*
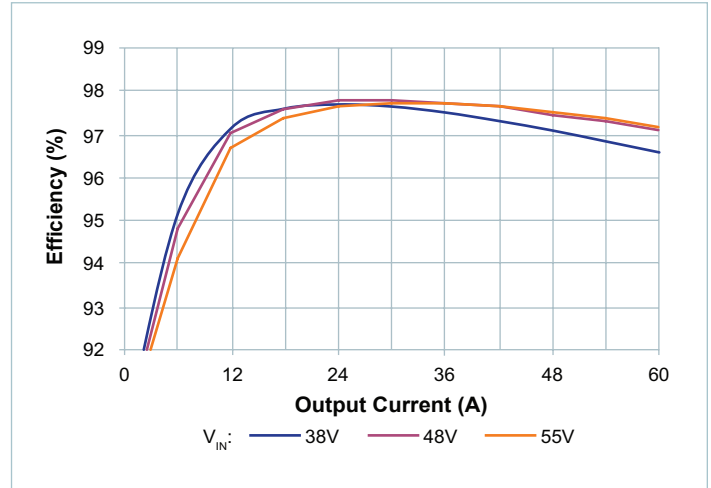


*Figure 2* — *Efficiency vs. output current, 55°C ambient*
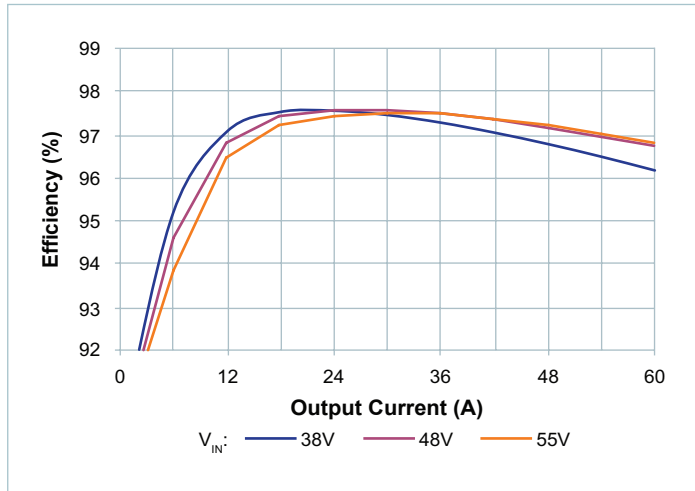


*Figure 3* — *Efficiency vs. output current, 70°C ambient*



CH1 Enable Pin: 5V/div
CH2 I$_{IN}$: 2A/div
CH3 V$_{OUT}$: 5V/div
Timebase: 400μs/div
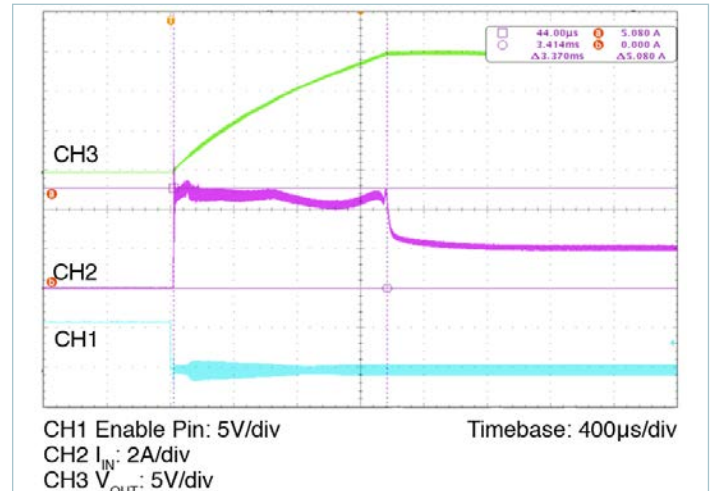
*Figure 4* — *Inrush current at high line 15% load; 5A/div, max load capacitance*



CH1 I$_{IN}$ Ripple: 0.2A/div　　　Timebase: 400ns/div
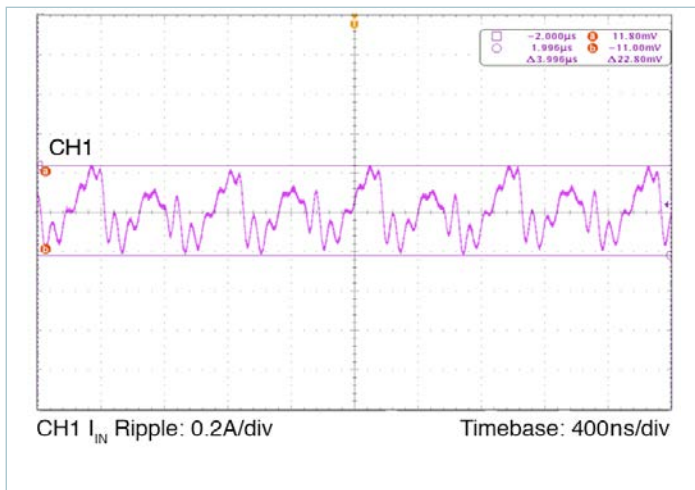
*Figure 5* — *Input reflected ripple current at nominal line, full load See Figure 22 for setup*



CH2 V$_{IN}$: 10V/div
CH4 V$_{OUT}$: 5V/div
Timebase: 4ms/div
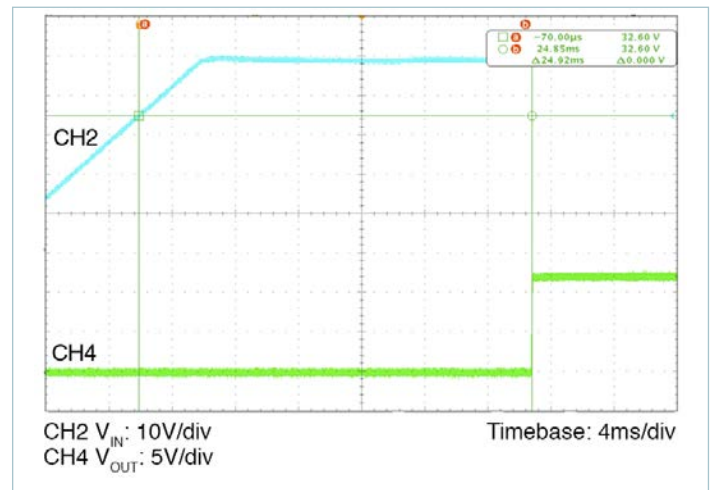
*Figure 6* — *Turn on delay time; V$_{IN}$ turn on delay at nominal line, 15% load*

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## Application Characteristics: Waveforms (Cont.)
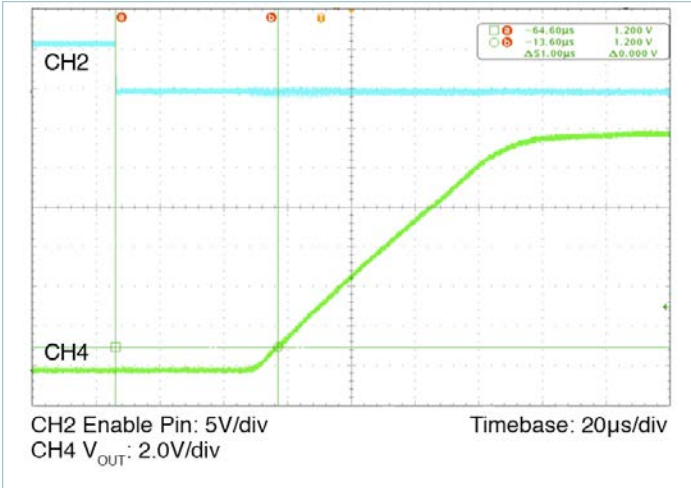


*Figure 7* — *Turn on delay time; enable at nominal line, 15% load, 0 capacitance.*

CH2 Enable Pin: 5V/div          Timebase: 20µs/div
CH4 V$_{OUT}$: 2.0V/div



*Figure 8* — *Output voltage rise time at nominal line, 10% load, 0 capacitance*

CH4 V$_{OUT}$: 2.0V/div          Timebase: 20µs/div
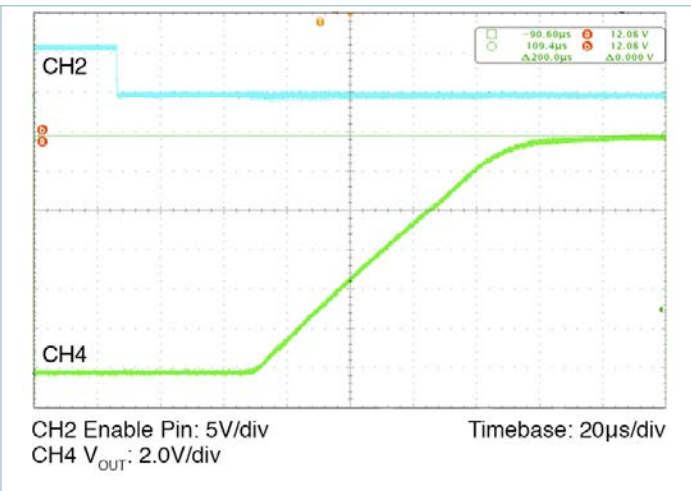


*Figure 9* — *Overshoot at turn on at nominal line, 15% load, 0 capacitance*

CH2 Enable Pin: 5V/div          Timebase: 20µs/div
CH4 V$_{OUT}$: 2.0V/div
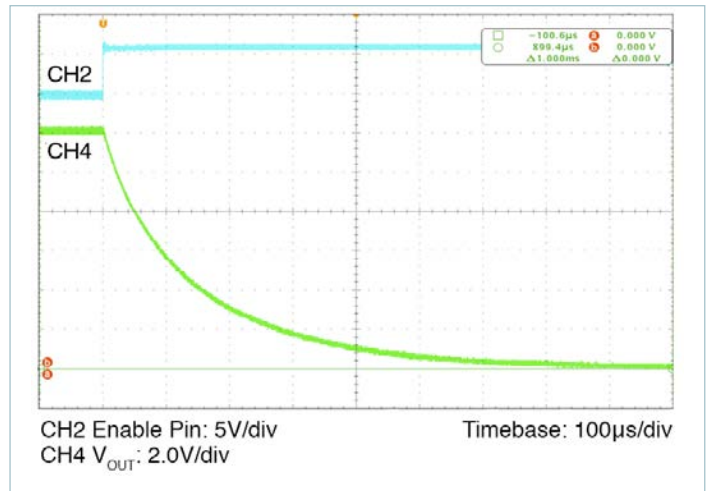


*Figure 10* — *Undershoot at turn off at nominal line; 15% load, 0 load capacitance*

CH2 Enable Pin: 5V/div          Timebase: 100µs/div
CH4 V$_{OUT}$: 2.0V/div
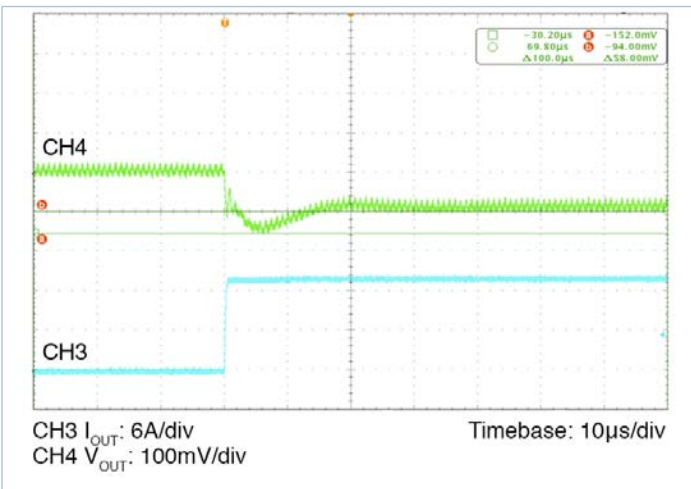


*Figure 11* — *Load transient response; nominal line, load step 75–100%*

CH3 I$_{OUT}$: 6A/div          Timebase: 10µs/div
CH4 V$_{OUT}$: 100mV/div
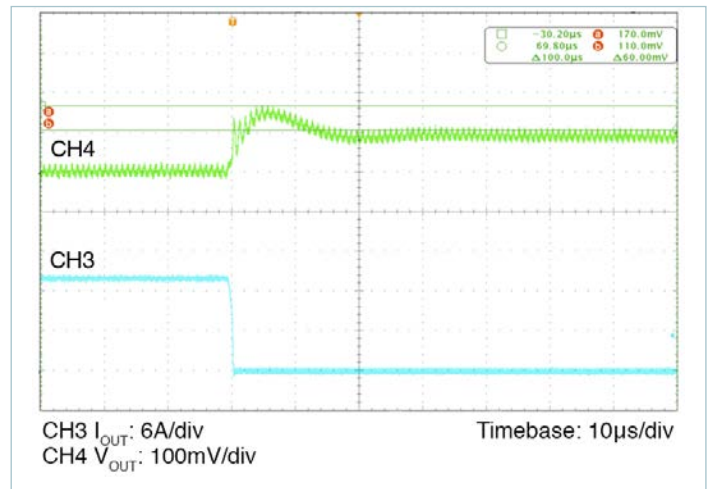


*Figure 12* — *Load transient response; full load to 75%; nominal line*

CH3 I$_{OUT}$: 6A/div          Timebase: 10µs/div
CH4 V$_{OUT}$: 100mV/div

## Application Characteristics: Waveforms (Cont.)
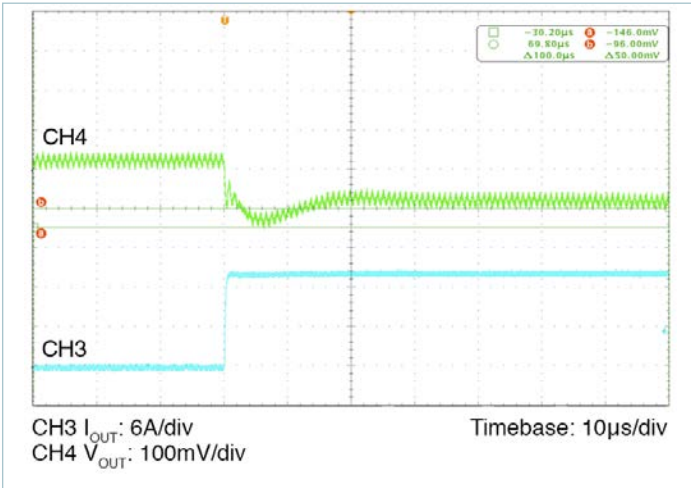
*Figure 13* — *Load transient response, nominal line Load step 0–25%*
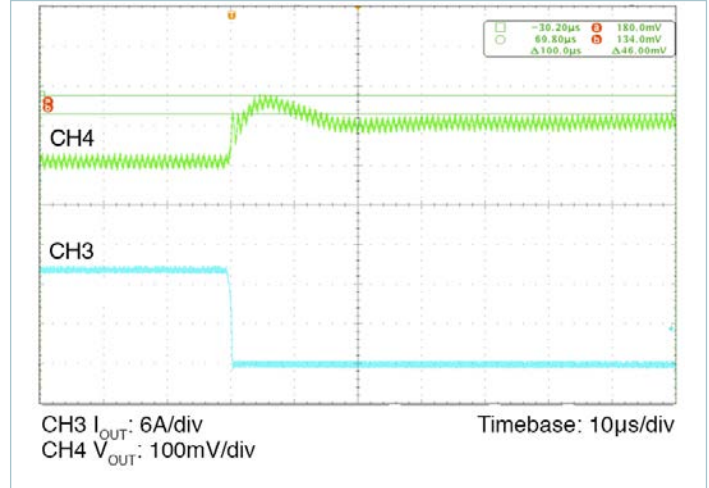
*Figure 14* — *Load transient response; nominal line Load step 25–0%*
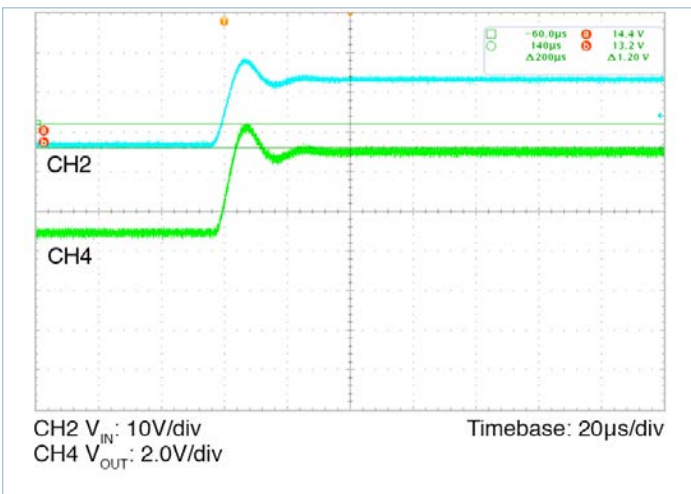
*Figure 15* — *Input transient response; $V_{IN}$ step low line to high line at full load*
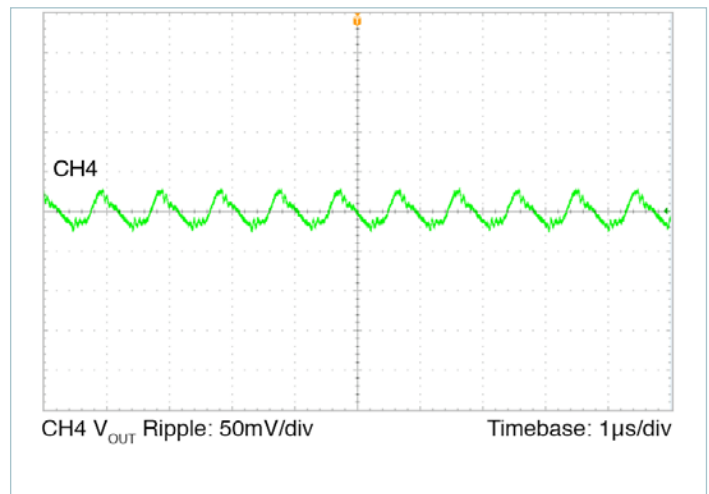
*Figure 16* — *Output ripple; nominal line, full load*
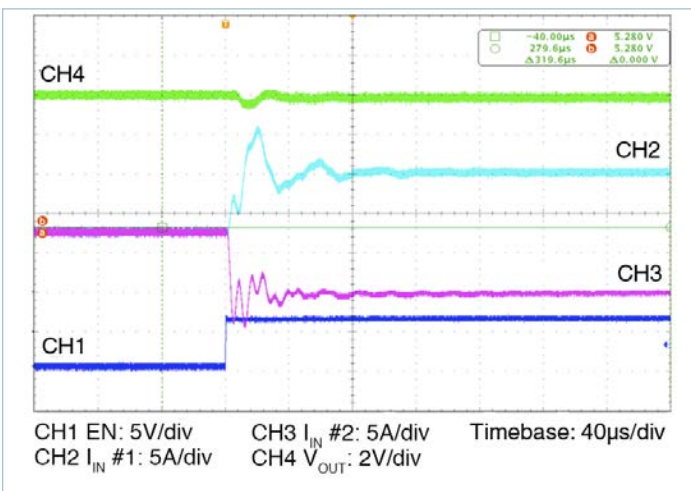
*Figure 17* — *Two modules parallel array test. $V_{OUT}$ and $I_{IN}$ change when one module is disabled. Nominal $V_{IN}$, $I_{OUT} = 60A$*
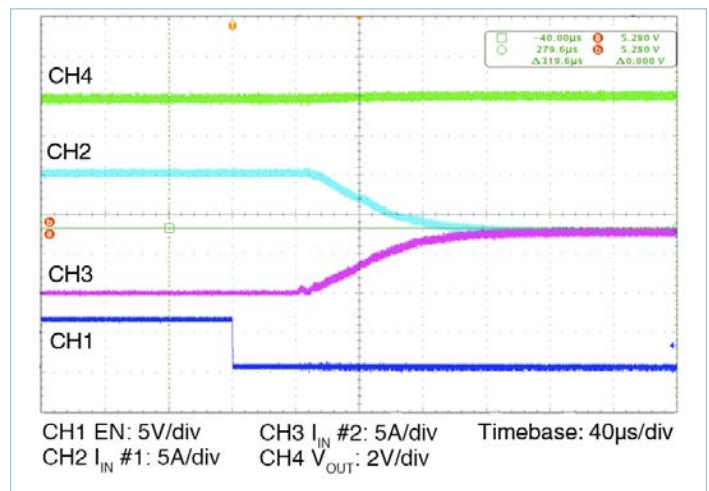
*Figure 18* — *Two modules parallel array test. $V_{OUT}$ and $I_{IN}$ change when one module is enabled. Nominal $V_{IN}$, $I_{OUT} = 60A$*

## Application Characteristics: Waveforms (Cont.)
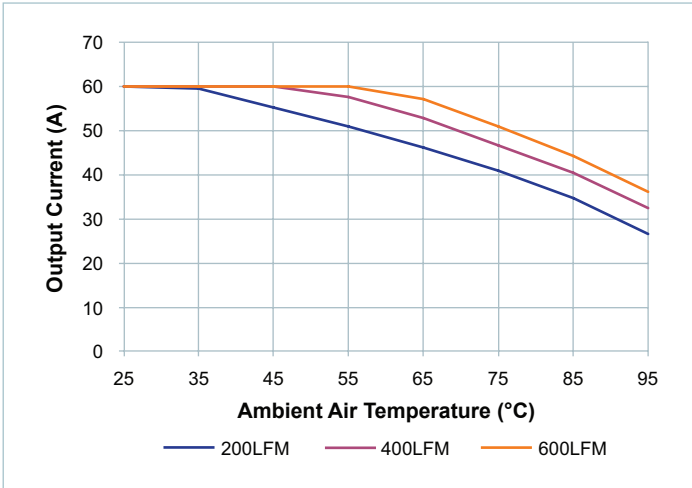
**Figure 19** — Maximum output current derating vs. ambient air temperature. Transverse airflow. Board and junction temperatures within IPC-9592 derating guidelines
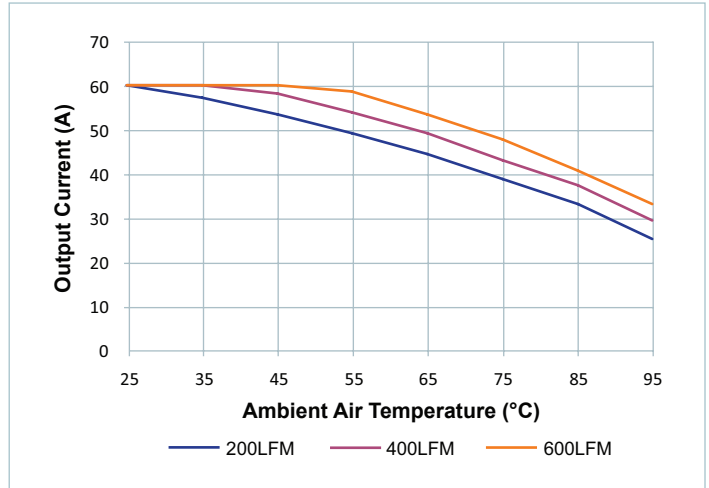
**Figure 20** — Maximum output current derating vs. ambient air temperature. Longitudinal airflow. Board and junction temperatures within IPC-9592 derating guidelines
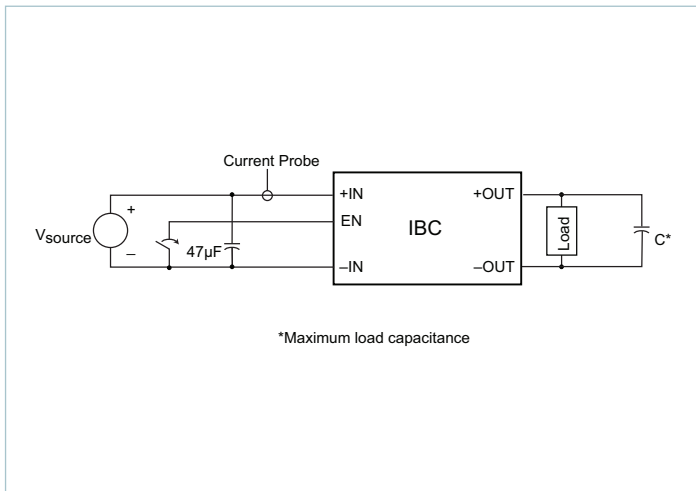
**Figure 21** — Test circuit; inrush current overshoot
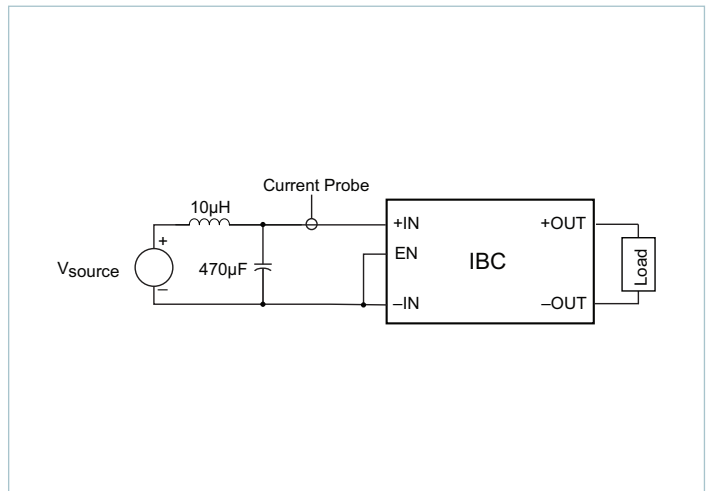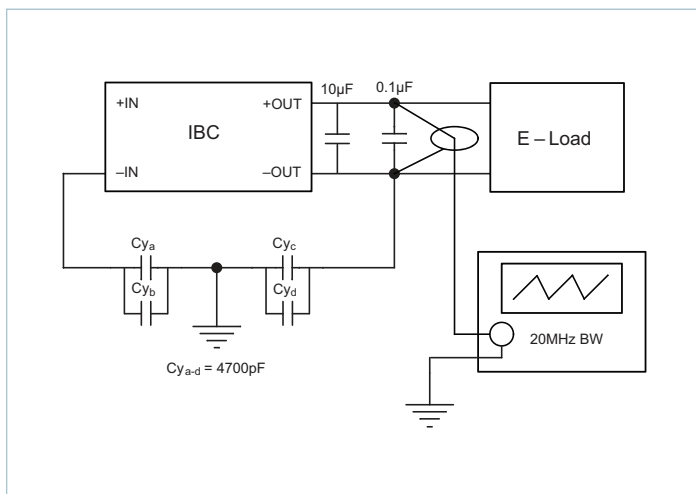
**Figure 22** — Test circuit; input reflected ripple current

**Figure 23** — Test circuit; output voltage ripple
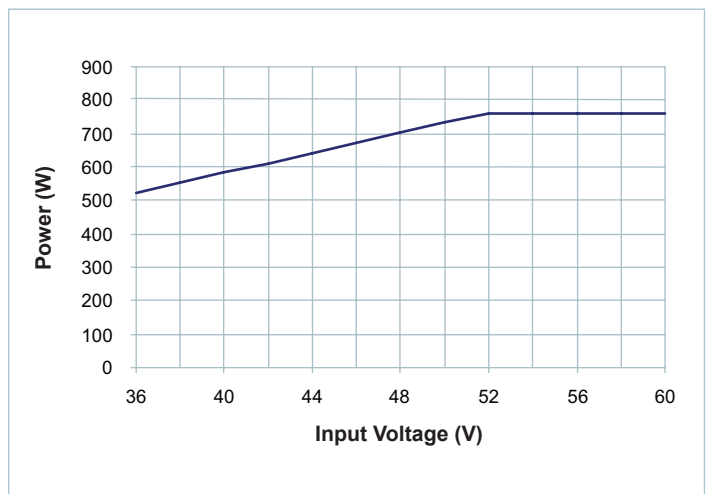
**Figure 24** — Maximum output ower vs. input voltage

## Application Characteristics: Thermal Data
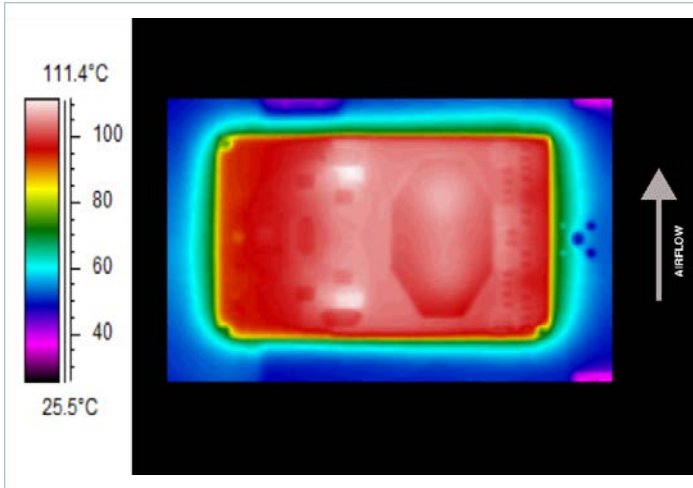


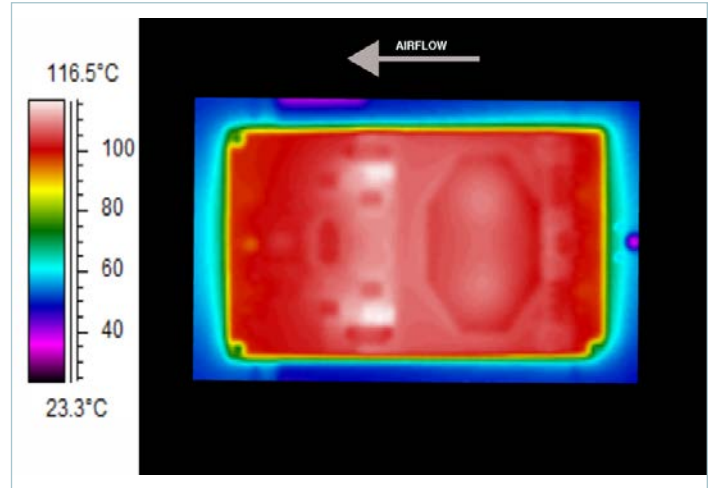*Figure 25* — *Thermal plot, 200LFM, 25°C, 48V$_{IN}$, 700W output power*



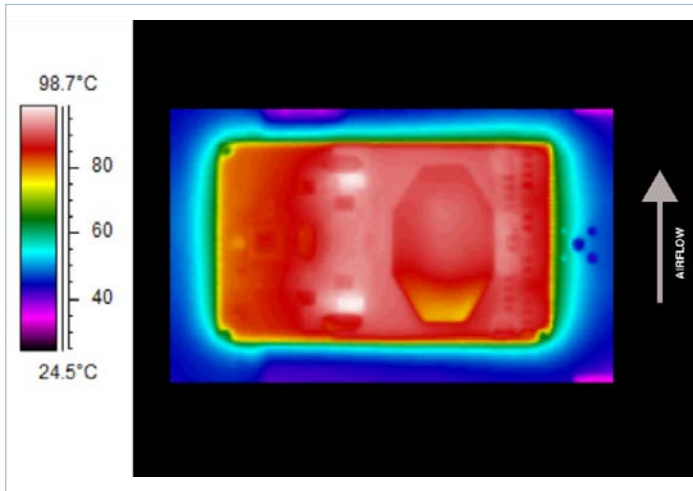*Figure 26* — *Thermal plot, 200LFM, 25°C, 48V$_{IN}$, 700W output power*



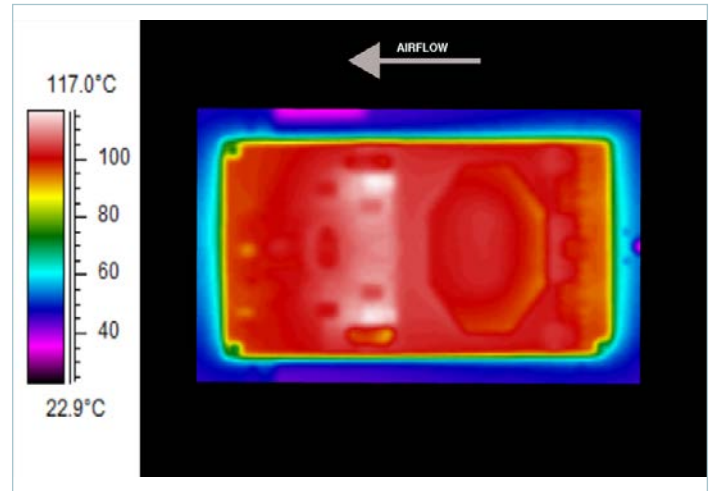*Figure 27* — *Thermal plot, 400LFM, 25°C, 48V$_{IN}$, 700W output power*



*Figure 28* — *Thermal plot, 400LFM, 25°C, 48V$_{IN}$, 700W output power*
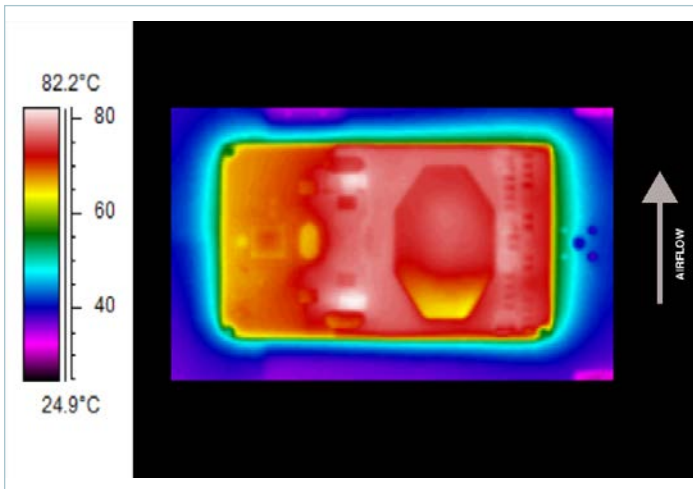


*Figure 29* — *Thermal plot, 600LFM, 25°C, 48V$_{IN}$, 700W output power*
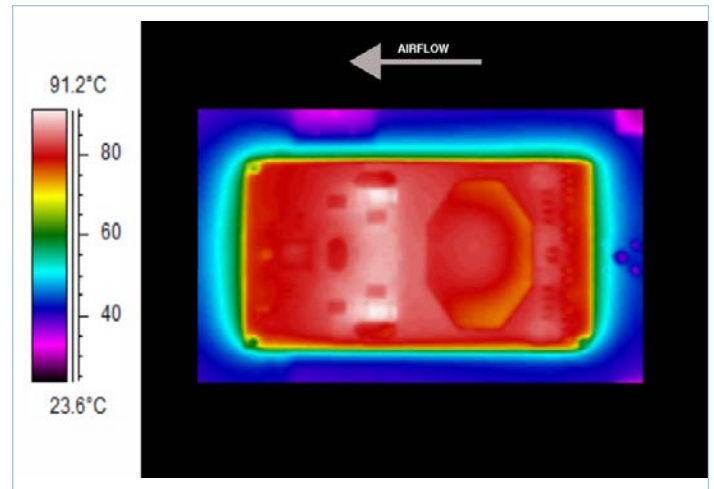


*Figure 30* — *Thermal plot, 600LFM, 25°C, 48V$_{IN}$, 700W output power*

## Pin / Control Functions

**+IN / –IN — DC Voltage Input Pins**

The IBC input voltage range should not be exceeded. An internal undervoltage/overvoltage lockout function prevents operation outside of the normal operating input range. The IBC turns on within an input voltage window bounded by the "Input undervoltage turn-on" and "Input overvoltage turn-off" levels, as specified. The IBC may be protected against accidental application of a reverse input voltage by the addition of a rectifier in series with the positive input, or a reverse rectifier in shunt with the positive input located on the load side of the input fuse.

The connection of the IBC to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be 47µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

**EN — Enable/Disable**

**Negative logic option**

If the EN port is left floating, the IBC output is disabled. Once this port is pulled lower than $0.8V_{DC}$ with respect to –IN, the output is enabled. The EN port can be driven by a relay, optocoupler, or open collector transistor. Refer to Figures 6 and 7 for the typical enable / disable characteristics. This port should not be toggled at a rate higher than 1Hz. The EN port should also not be driven by or pulled up to an external voltage source.

**Positive logic option**

If the EN port is left floating, the IBC output is enabled. Once this port is pulled lower than $1.4V_{DC}$ with respect to –IN, the output is disabled. This action can be realized by employing a relay, optocoupler, or open collector transistor. This port should not be toggled at a rate higher than 1Hz.

The EN port should also not be driven by or pulled up to an external voltage source. The EN port can source up to 2mA at $5V_{DC}$. The EN port should never be used to sink current.

If the IBC is disabled using the EN pin, the module will attempt to restart approximately every 250ms. Once the module has been disabled for at least 250ms, the turn on delay after the EN pin is enabled will be as shown in Figure 7.

**+OUT / –OUT — DC Voltage Output Pins**

Total load capacitance at the output of the IBC should not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the IBC, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the IBC.
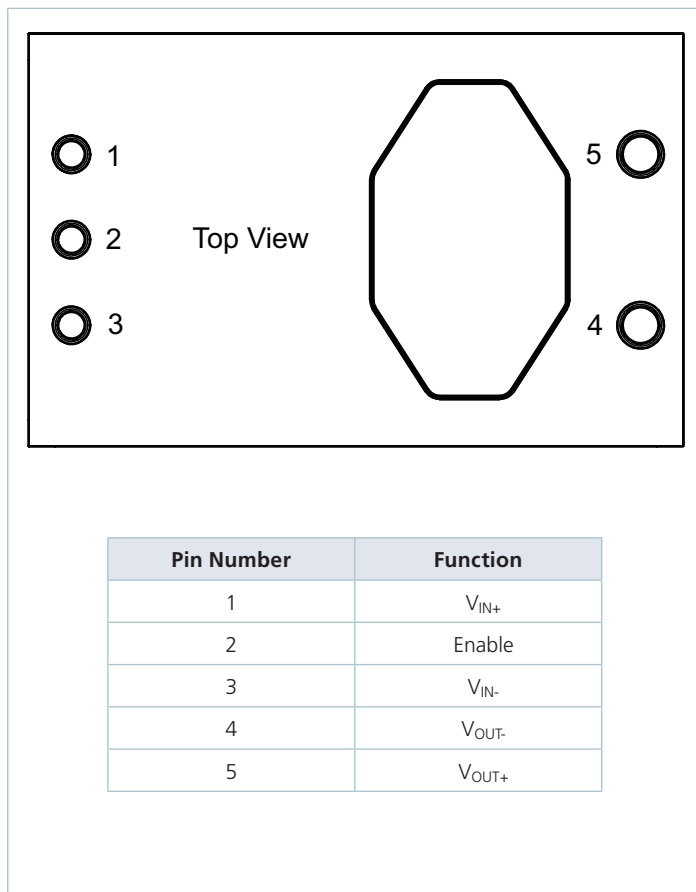


| Pin Number | Function |
|---|---|
| 1 | $V_{IN+}$ |
| 2 | Enable |
| 3 | $V_{IN-}$ |
| 4 | $V_{OUT-}$ |
| 5 | $V_{OUT+}$ |

***Figure 31*** — *IBC Pin Designations*

## Applications Note

### Parallel Operation

The IBC will inherently current share when operated in an array. Arrays may be used for higher power or redundancy in an application. Current sharing accuracy is maximized when the source and load impedance presented to each IBC within an array are equal. The recommended method to achieve matched impedances is to dedicate common copper planes within the PCB to deliver and return the current to the array, rather than rely upon traces of varying lengths. In typical applications the current being delivered to the load is larger than that sourced from the input, allowing narrower traces to be utilized on the input side if necessary. The use of dedicated power planes is, however, preferable.

One or more IBCs in an array may be disabled without adversely affecting operation or reliability as long as the load does not exceed the rated power of the enabled IBCs.

The IBC power train and control architecture allow bi-directional power transfer, including reverse power processing from the IBC output to its input. The IBC's ability to process power in reverse improves the IBC transient response to an output load dump.

### Thermal Considerations

The temperature distribution of the VI Brick® can vary significantly with its input / output operating conditions, thermal management and environmental conditions. Although the PCB is UL rated to 130°C, it is recommended that PCB temperatures be maintained at or below 125°C. For maximum long term reliability, lower PCB temperatures are recommended for continuous operation, however, short periods of operation at 125°C will not negatively impact performance or reliability.

WARNING: Thermal and voltage hazards. The IBC can operate with surface temperatures and operating voltages that may be hazardous to personnel. Ensure that adequate protection is in place to avoid inadvertent contact.

### Input Impedance Recommendations

To take full advantage of the IBC capabilities, the impedance presented to its input terminals must be low from DC to approximately 5MHz. The source should exhibit low inductance and should have a critically damped response. If the interconnect inductance is excessive, the IBC input pins should be bypassed with an RC damper (e.g., 47µF in series with 0.3Ω) to retain low source impedance and proper operation. Given the wide bandwidth of the IBC, the source response is generally the limiting factor in the overall system response.

Anomalies in the response of the source will appear at the output of the IBC multiplied by its K factor. The DC resistance of the source should be kept as low as possible to minimize voltage deviations. This is especially important if the IBC is operated near low or high line as the overvoltage/undervoltage detection circuitry could be activated.

### Input Fuse Recommendations

The IBC is not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of VI Bricks must always be incorporated within the power system. A fast acting fuse should be placed in series with the +IN port. See safety agency approvals.

### Application Notes

For IBC and VI Brick application notes on soldering, thermal management, board layout, and system design visit www.vicorpower.com.
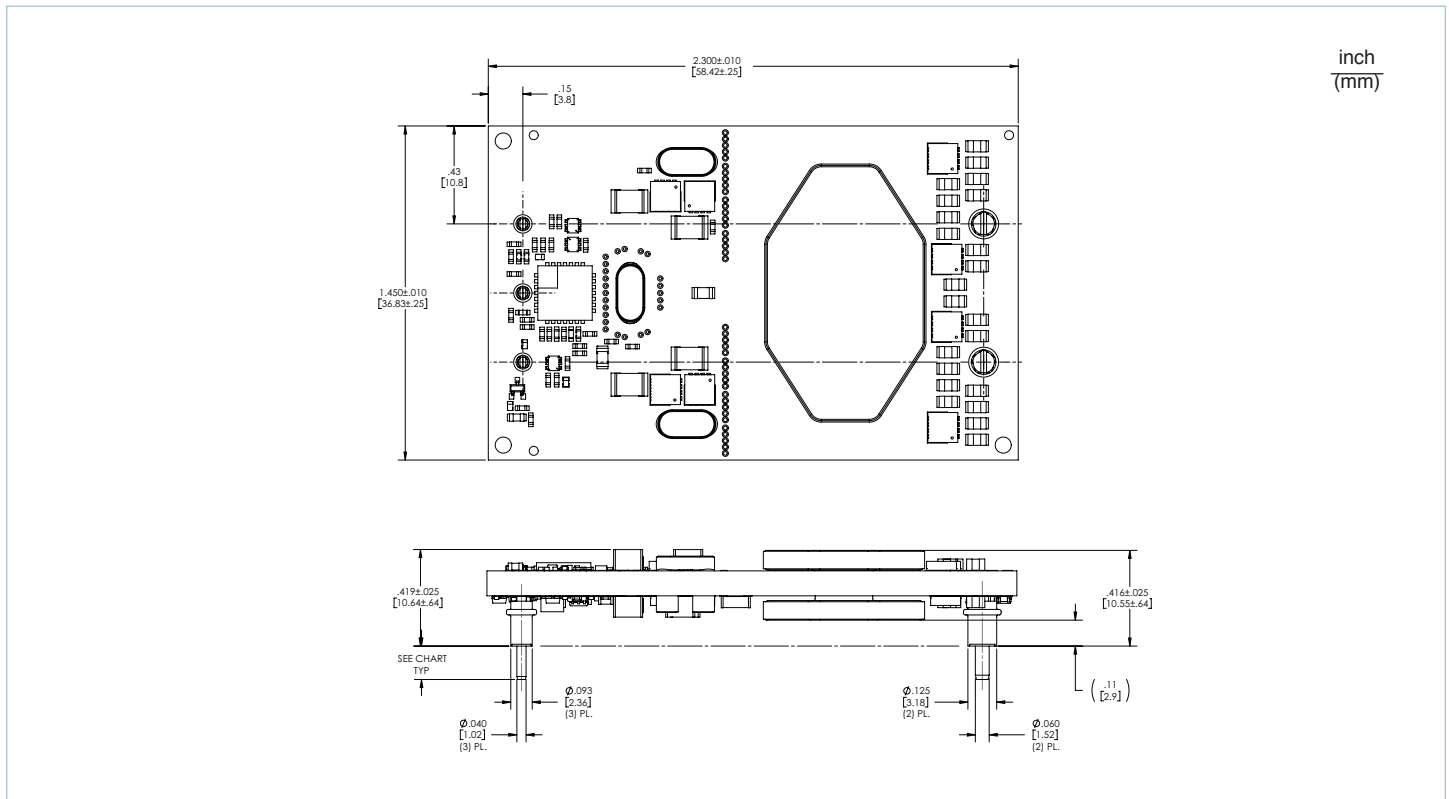
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## Mechanical Drawings



*Figure 32* — IBC outline drawing
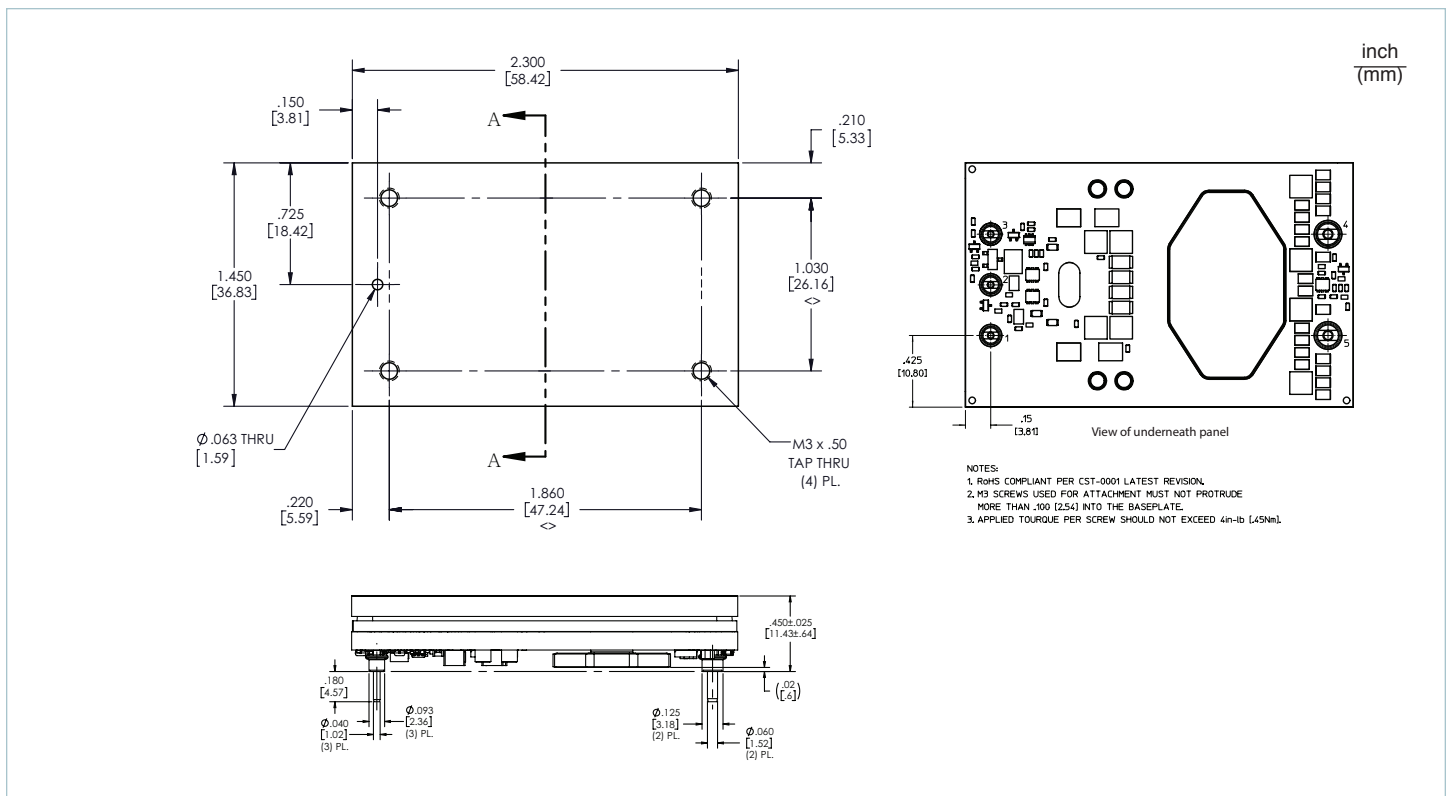


*Figure 33* — IBC outline drawing – baseplate option

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## Mechanical Drawings (Cont.)

inch
(mm)

RECOMMENDED HOLE PATTERN

2.000±.003
[50.80±.08]

1          5

.300±.003
[7.62±.08]        2                    Top View

.300±.003
[7.62±.08]        3

4

∅ .080±.003
[2.03±.08]
(3) PL.

∅ .100±.003
[2.54±.08]
(2) PL.

NOTES:
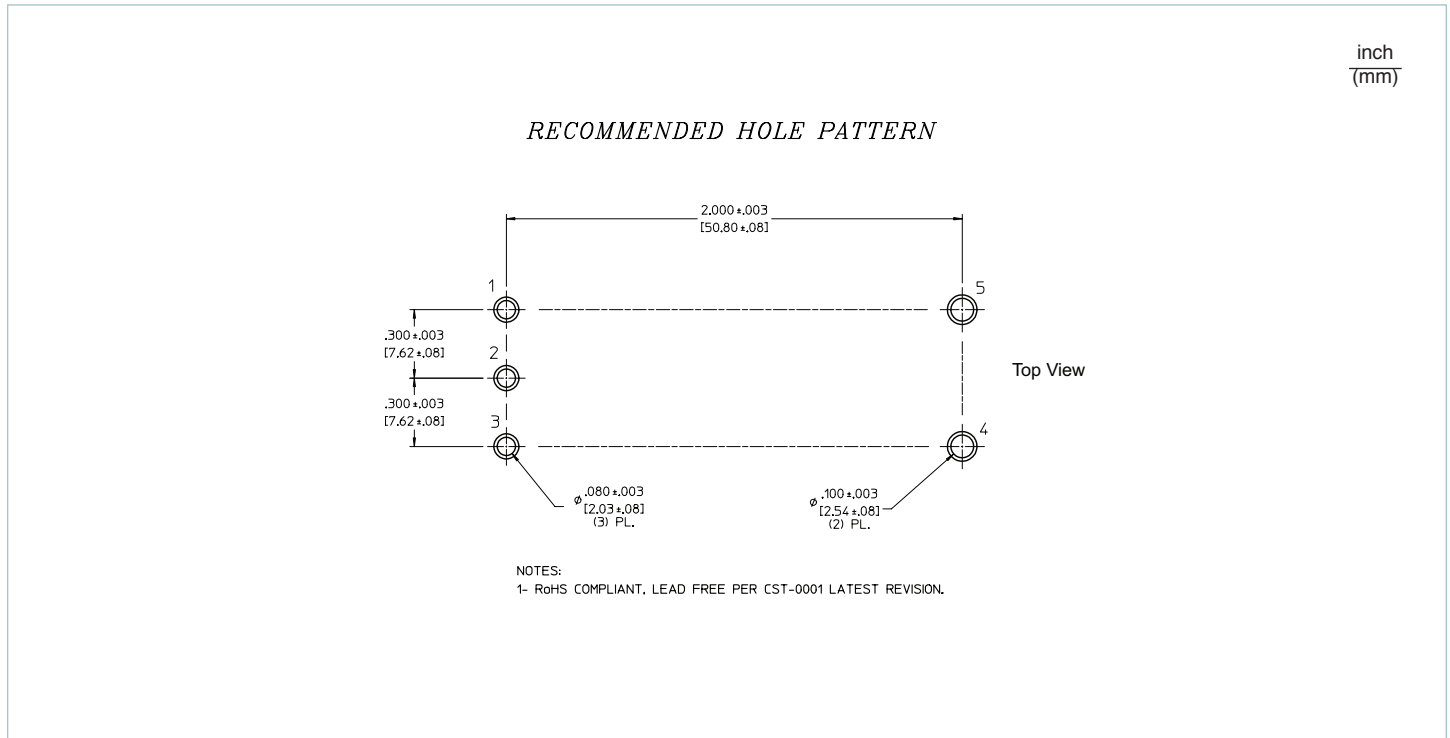1– RoHS COMPLIANT, LEAD FREE PER CST–0001 LATEST REVISION.

*Figure 34* — *IBC PCB recommended hole pattern*

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