PI2001-EVAL1

Cool-ORing™ Series

PI2001-EVAL1 Active ORing Evaluation Board User Guide

Contents

Cool-ORing™ Series

PI2001-EVAL1 Evaluation Board featuring the *Cool-ORing* PI2001 Universal Active ORing controller.

The PI2001-EVAL1 Evaluation Board is intended to acquaint the user with the benefits and features of the Cool-ORing™ PI2001 Universal Active ORing controller. It is not designed to be installed in end-use equipment.

Please read this document before setting up the PI2001-EVAL1 Evaluation Board and refer to the PI2001 product data sheet for device specifications, functional description and characteristics.

During operation, the power devices and surrounding structures can be operated safely at high temperatures.

- Remove power and use caution when connecting and disconnecting test probes and interface lines to avoid inadvertent short circuits and contact with hot surfaces.
- When testing electronic products always use approved safety glasses. Follow good laboratory practice and procedures.

Introduction

The PI2001-EVAL1 allows the user to test the basic principle and operational characteristics of an Active ORing function in a redundant power architecture, while also experiencing the benefits and value of the PI2001 solution versus conventional Active ORing solutions. The PI2001-EVAL1 evaluation board is configured to receive two independent power source inputs, per a typical redundant power architecture, through two Active ORing channels that are combined to form a redundant power output. Each channel contains a PI2001 controller and an N-channel power MOSFET. The MOSFET foot print can take an SO-8 or Power SO-8 MOSFET package. Each channel is capable of up to 20 A, for high current Active ORing, above 20 A, the two channels provided on the evaluation board can be paralleled in a master/slave configuration and OR'd with a second evaluation board.

The PI2001-EVAL1 evaluation board is designed with optimized PCB layout and component placement to represent a realistic high density final design for an embedded Active ORing solution for ≤ 7 Vbus applications requiring up to 20 A. This evaluation board is intended as an easy and simple way to test the electrical and thermal performance of the PI2001 Active ORing controller.

Both dynamic and steady state testing of the PI2001 can be completed on the PI2001-EVAL1 evaluation board, in addition to using the key features of the product. Dynamic testing can be completed under a variety of system level fault conditions to check for response time to faults.

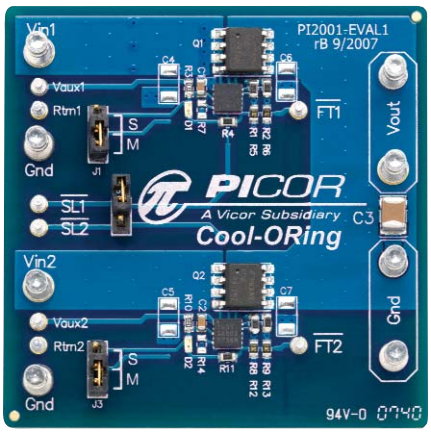
This document provides basic instructions for initial start-up and configuration of the evaluation board. Further information on the functionality of the PI2001 can be found in the PI2001 product data sheet.

Cool-ORing™ PI2001 Product Description

The Cool-ORing PI2001 with an external industry standard N-channel MOSFET provides a complete Active ORing solution designed for use in redundant power system architectures. The PI2001 controller with N-channel MOSFET enables extremely low power loss with fast dynamic response to fault conditions, critical for high availability systems. A master / slave feature allows the paralleling of PI2001 solutions for high current Active ORing requirements. The PI2001 can also drive multiple paralleled MOSFETs.

The PI2001 controller with a low Rds(on) N-channel MOSFET provides very high efficiency and low power loss during steady state operation. The PI2001 controller provides an active low fault flag output to the system during excessive forward current, light load, reverse current, over-voltage, under-voltage, and over-temperature fault conditions. A temperature sensing function indicates a fault if the maximum junction temperature exceeds 160°C. The under-voltage and over-voltage thresholds are programmable via an external resistor divider.

Figure 1 shows a photo of the PI2001-EVAL1 evaluation board, with two PI2001 controllers and two N-channel MOSFETs used to form the two Active ORing channels. The board is built with two identical Active ORing circuits with options and features that enable the user to fully explore the capabilities of the PI2001 universal Active ORing controller.



Terminals Rating

Vin1, Vin2	8V / 24 A
Vaux1, Vaux2, (R2 = R4 = 10 Ω)	-0.3 V to 17.3 V / 40 mA
$\overline{SL1}$, $\overline{SL2}$	-0.3 V to 8.0 V / 10 mA
$\overline{FT1}$, $\overline{FT2}$	-0.3 V to 17.3 V / 10 mA

Figure 1 *– PI2001-EVAL1 Evaluation Board (1.8" x 1.8")*

Terminal	Description
Vin1	**Power Source Input #1** or bus input designed to accommodate up to 20 A continuous current.
Vaux1	**Auxiliary Input Voltage #1** to supply PI2001 VC power. Vaux1 should be equal to Vin1 plus 5 V or higher. See details in Auxiliary Power Supply (Vaux) section of the PI2001 data sheet.
Rtn1	**Vaux1 Return Connection:** Connected to Ground plane
Gnd	**Vin & Vout Return Connection:** Three Gnd connections are available and are connected to a common point, the Ground plane. Input supplies Vin1 & Vin2 and the output load at Vout should all be connected to their respective local Gnd connection.
$\overline{SL1}$	**PI2001 (U1) Slave Input-Output Pin:** For monitoring U1 slave pin. When U1 is configured as the Master, this pin functions as an output that drives slaved PI2001 devices. When U1 is configured in Slave mode, $\overline{SL1}$ serves as an input.
$\overline{SL2}$	**PI2001 (U2) Slave Input-Output Pin:** For monitoring U2 slave pin. When U2 is configured as the Master, this pin functions as an output that drives slaved PI2001 devices. When U2 is configured in Slave mode, $\overline{SL2}$ serves as an input.
Vin2	**Power Source Input #2** or bus input designed to accommodate up to 20 A continuous current.
Vaux2	**Auxiliary Input Voltage #2** to supply PI2001 VC power. Vaux2 should be equal to Vin2 plus 5 V or higher. See details in Auxiliary Power Supply (Vaux) section of the PI2001 data sheet.
Rtn2	**Vaux2 Return Connection:** Connected to Ground plane
$\overline{FT1}$	**PI2001 (U1) Fault Pin:** Monitors U1 fault conditions
$\overline{FT2}$	**PI2001 (U2) Fault Pin:** Monitors U2 fault conditions
Vout	**Output:** Q1 and Q2 MOSFET Drain pins connection, connect to the load high side.

Table 1 *– PI2001-EVAL1 Evaluation Board terminals description*

Jumper	Description
J1, J3	BK Jumpers: Connect jumper across M for master mode and across S for slave mode. Remove jumper to adjust reverse fault blanking time using Rbk. Rbk is R7 for U1 and R14 for U2 shown in the schematic, Figure 2.
J2	Slave Jumper: Remove the jumper unless one of the PI2001 is configured in slave mode.

Table 2 *– PI2001-EVAL1 Evaluation Board jumpers description*

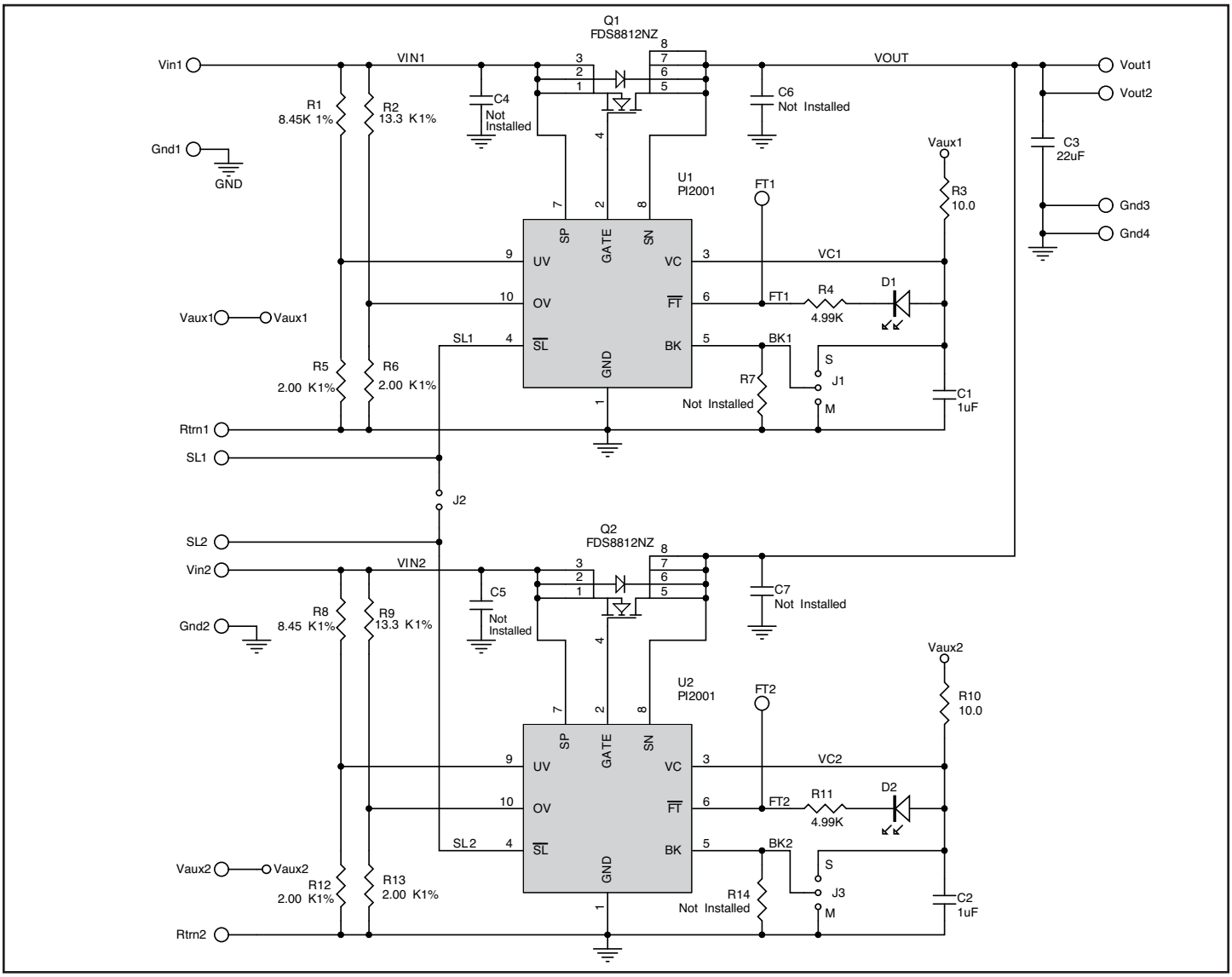


***Figure 2** – PI2001-EVAL1 Evaluation Board schematic.*

Item	QTY	Reference Designator	Value	Description	Footprint	Manufacturer
1	2	C1, C2	1 µF	Capacitor, MLCC X5R, 1 µF,16 V	0603	
2	1	C3	22 µF	Capacitor, MLCC X7R, 22 µF, 25 V	1210	
3	4	C4, C5, C6, C7		Not installed	1206	
4	2	D1, D2		LED, Super Red	THIN 0603	Lite-On, Inc.,
5	8	$\overline{FT1}$, $\overline{FT2}$, Rtn1, Rtn2, $\overline{SL1}$, $\overline{SL2}$, Vaux1, Vaux2		Turret Test point	TURRET-1528	Keystone Electronics
6	7	Gnd1, Gnd2, Gnd3, Gnd4, Vin1, Vin2, Vout1, Vout2		Turret Test point	TURRET-1502	Keystone Electronics
7	2	J1, J3		Header Pins 0.1" pitch	2 x 3mm	
8	1	J2		Header Pins 0.1" pitch	2 x 2mm	
9	2	Q1, Q2		FDS8812NZ 30 V, 20 A, N-MOSFET	SO-8	Fairchild
10	2	R1, R8	8.45 KΩ	Resistor,8.45 KΩ,1%	0603	
11	2	R2, R9	13.3 KΩ	Resistor,13.3 KΩ,1%	0603	
12	2	R3, R10	10 Ω	Resistor,10 Ω,5%	0603	
13	2	R4, R11	4.99 KΩ	Resistor, 4.99 KΩ,5%	0603	
14	4	R5, R6, R12, R13	2.00 KΩ	Resistor, 2.00 KΩ,1%	0603	
15	2	R7, R14	Not Installed		0603	
16	2	U1, U2	PI2001	Picor Universal Active ORing Controller	3mmx3mm; 10-TDFN	PICOR

***Table 3** – PI2001-EVAL1 Evaluation Board bill of materials*

Reference Designator	Value	Functional Description
C1, C2	1 µF	VC Bypass Capacitor
C3	22 µF	Output (Load) Capacitor
C4, C5, C6, C7	Not installed	Snubber to reduce voltage ringing when the device turns off
D1, D2	LED	To indicate a fault exist when it is on
J1, J3	Jumper	To select between Master and Slave Modes
J2	Jumper	Connection between $\overline{SL1}$ and $\overline{SL2}$
Q1, Q2	N-MOSFET	ORing Main Switch
R1, R8	8.45 KΩ	UV Voltage Divider Resistor (R2UV in Figure 4)
R2, R9	13.3 KΩ	OV Voltage Divider Resistor (R2OV in Figure 4)
R3, R10	10 Ω	VC Bias resistor
R4, R11	4.99 KΩ	LED Current Limiter
R5, R6	2.00 KΩ	UV Voltage Divider Resistor (R1UV in Figure 4)
R7, R14	Not Installed	BK Delay Timer Programmable Resistor
U1, U2	PI2001	Universal Active ORing Controller

***Table 4** – Component functional description*

Initial Test Set Up

To test the PI2001-EVAL1 evaluation board it is necessary to configure the jumpers (J1, J2 and J3) first based on the required board configuration.

Failure to configure the jumpers prior to the testing may result in improper circuit behavior

Baseline Test Procedure (Refer to Figure 3)

1.0 Recommended Equipment

1.1 Two DC power supplies - 0-10 V; 25 A.
1.2 DC power supply 12 V; 100 mA.
1.3 DC electronic load - 50 A minimum.
1.4 Digital Multimeter
1.5 Oscilloscope.
1.6 Appropriately sized interconnect cables.
1.7 Safety glasses.
1.8 PI2001 Product Data sheet.

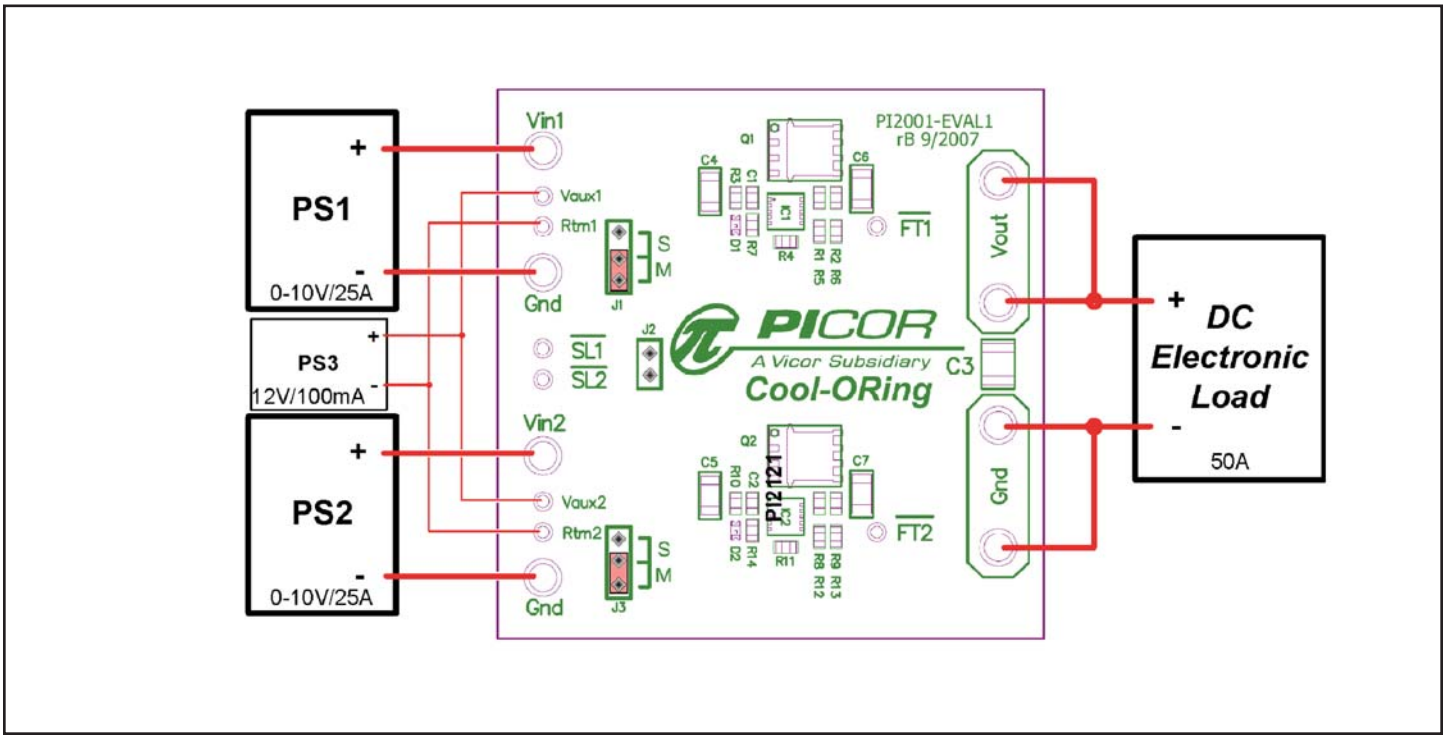


***Figure 3** – Layout configuration for a typical redundant power application, using PI2001 with both solutions configured in Master Mode.*

Before initial power-up follow these steps to configure the evaluation board for specific end application requirements:

2.0 Undervoltage (UV) and Overvoltage (OV) resistors set up:

2.1 UV and OV programmable resistors are configured for a 3.3 V Vin (BUS voltage) application in a two-resistor voltage divider configuration as shown in Figure 4. UV is set to 2.6 V and OV is set for 3.8 V, R1OV and R1UV are 2.00KΩ 1%. If PI2121-EVAL1 is required to be used in a different Vin voltage . . application please follow the following steps to change the resistor values.

2.1.1 It is important to consider the maximum current that will flow in the resistor divider and maximum error due to UV and OV input . current.

$$R1_{UV} = \frac{V(UV_{TH})}{I_{RUV}}$$

2.1.2 Set $R1_{UV}$ and $R1_{OV}$ value based on system allowable minimum current and 1% error; $I_{RUV} \geq 100\ \mu A$

$$R2_{UV} = R1_{UV}\left(\frac{V(UV)}{V(UV_{TH})} - 1\right)$$

Where:

$V(UV_{TH})$: UV threshold voltage

V(UV) : UV voltage set (0.5 V typ)

I_{RUV}: $R1_{UV}$ current

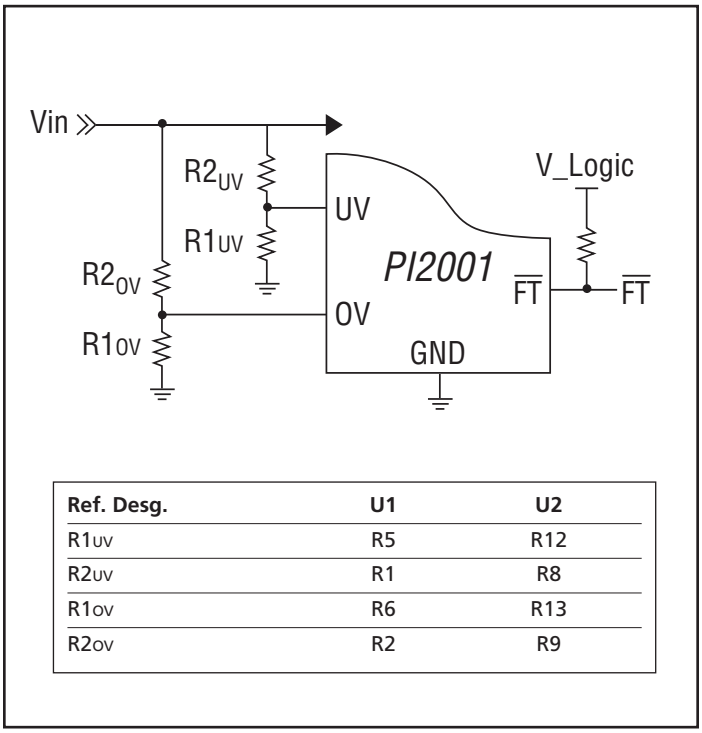
$$R2_{OV} = R1_{OV}\left(\frac{V(OV)}{V(OV_{TH})} - 1\right)$$

Where:

$V(OV_{TH})$: OV threshold voltage

V(OV) : OV voltage set (0.5 V typ)

I_{ROV}: $R1_{OV}$ current



Ref. Desg.	U1	U2
$R1_{UV}$	R5	R12
$R2_{UV}$	R1	R8
$R1_{OV}$	R6	R13
$R2_{OV}$	R2	R9

Figure 4 *– UV & OV two-resistor divider configuration*

2.1.3 Example for 2.0 V Vin (BUS voltage), to set UV and OV for ±10% Vin set UV at 1.8 V and OV at 2.2 V.

$$R2_{UV} = R1_{UV}\left(\frac{V(UV)}{V(UV_{TH})} - 1\right) = 2.00\ K\Omega * \left(\frac{1.8\ V}{0.5\ V} - 1\right) = 5.20\ K\Omega \text{ (or } 5.23\ K\Omega \text{ \% standard value)}$$

$$R2_{OV} = R1_{OV}\left(\frac{V(OV)}{V(OV_{TH})} - 1\right) = 2.00\ K\Omega * \left(\frac{2.2\ V}{0.5\ V} - 1\right) = 6.80\ K\Omega \text{ (or } 6.81\ K\Omega \text{ \% standard value)}$$

3.0 Blanking timer setup:

3.1 The blanking timer provides noise filtering for typical switching power conversion that might cause premature reverse current detection by masking the reverse fault condition. The shortest blanking time is 50 ns when the BK pin is connected to ground. Connecting an external resistor (R_{BK}, reference designators R7 for U1 and R14 for U2) between the BK pin and ground will increase the blanking time as shown in Figure 5.

Where: $R_{BK} \leq 200\ K\Omega$

Note: *When BK is connected to VC for slave mode . operation,then the blanking time will be 270 ns typically.*

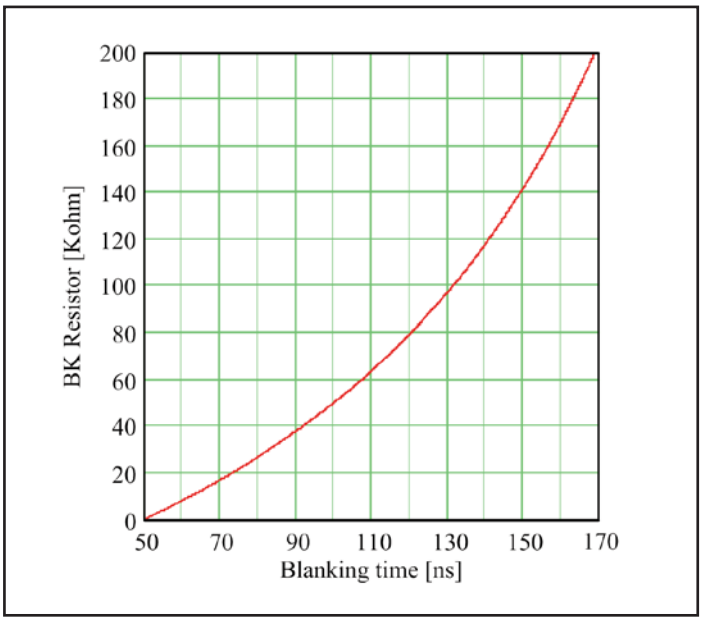


Figure 5 *–BK Resistor selection versus Blanking Time*

4.0 Auxiliary Power Supply (Vaux):

4.1 The PI2001 Controller has a separate input (VC) that provides power to the control circuitry and the gate driver. An internal voltage regulator (VC) clamps the VC voltage to 15.5 V typically.

4.2 Connect independent power source to Vaux inputs of PI2001-EVAL1 Evaluation Board to supply power to the VC input. The Vaux voltage should be 5V higher than Vin (redundant power source output voltage) to fully enhance the MOSFET. If the MOSFET is replaced with different MOSFET, make sure that Vaux= Vin + 0.5 V + required voltage to be enhance the MOSFET.

4.3 10 Ω bias resistors (Rbias, reference designators R3 and R10) are installed on the PI2001-EVAL1 between each Vaux input and VC pin of one of the PI2001 controller.

4.4 If Vaux is higher than the Clamp voltage, 15.5 V typical, the Rbias value has to be changed using the following equations:

4.4.1 Select the value of Rbias using the following equation:

$$Rbias = \frac{Vaux_{min} - VC_{clampMAX}}{IC_{max}}$$

4.4.2 Calculate Rbias maximum power dissipation:

$$Pd_{Rbias} = \frac{(Vaux_{max} - VC_{clampMIN})^2}{Rbias}$$

Where:

$Vaux_{min}$: Vaux minimum voltage

$Vaux_{max}$: Vaux maximum voltage

$VC_{ClampMAX}$: Maximum controller clamp voltage, 16.0 V

$VC_{ClampMIN}$: Minimum controller clamp voltage, 14.0 V

IC_{max}: Controller maximum bias current, use 4.2 mA

4.4.3 For example, if the minimum Vaux = 22 V and the maximum Vaux = 28 V

$$Rbias = \frac{Vaux_{min} - VC_{clampMAX}}{IC_{max}} = \frac{22\ V - 16\ V}{4.2\ mA} = 1.429\ K\Omega$$

,use 1.43 KΩ 1% resistor

$$Pd_{Rbias} = \frac{(Vaux_{max} - VC_{clampMIN})^2}{Rbias} = \frac{(28\ V - 14.0\ V)^2}{1.43\ K\Omega} = 137\ mW$$

Note: *Minimize the resistor value for low Vaux voltage levels to avoid a voltage drop that may reduce the VC voltage lower than required to drive the gate of the internal MOSFET.*

5.0 Hook Up of the Evaluation Board

5.1 OV and UV resistors values are configured for a 3.3 V input voltage. If you are using the evaluation board in a different input voltage level you have to adjust the resistor values by replacing R1, R2, R8 and R9, or remove R2, R5, R9 and R12 to disable UV and OV. Please refer to the UV/OV section for details to set R1, R2, R8 and R9 proper values.

5.2 Verify that the jumpers J1 and J3 are installed for master mode [across M] and no Jumper on J2.

5.3 Connect the positive terminal of PS1 power supply to Vin1. Connect the ground terminal of PS1 to its local Gnd. Set the power supply to 3.3 V. Keep PS1 output disabled (OFF).

5.4 Connect the positive terminal of PS2 power supply to Vin2. Connect the ground terminal of PS2 to its local Gnd. Set the power supply to 3.3 V. Keep PS2 output disabled (OFF).

5.5 Connect the positive terminal of PS3 power supply to Vaux1 and Vaux2. Connect the ground terminal of this power supply to Rtn1 and Rtn2. Set the power supply to 12 V. Keep PS3 output disabled (OFF).

5.6 Connect the electronic load to the output between Vout and Gnd. Set the load current to 10 A.

5.7 Enable (turn ON) PS1 power supply output.

5.8 Turn on the electronic load.

5.9 Verify that the electronic load input voltage reading is one diode voltage drop below 3.3 V.

5.10 Enable (turn ON) PS3 power supply output.

5.11 Verify that the electronic load voltage reading increases to a few millivolts below 3.3 V. This verifies that the MOSFET is in conduction mode.

5.12 D1 should be off. This verifies that there is no fault condition.

5.13 Reduce PS1 output voltage to 2 V,

5.14 D1 should turn on, this verifies that the circuit is in an under-voltage fault condition.

5.15 Increase PS1 output to 3.3 V, D1 should turn off, then increase PS1 output to 4 V, D1 should turn on indicating an over-voltage fault condition

5.16 Verify that Vin2 is at 0V. This verifies that the PI2001 (U2) FET (Q2) is off.

5.17 D2 should be on. This is due to a reverse voltage fault condition caused by the bus voltage being high with respect to the input voltage (Vin2).

5.18 Enable (turn ON) PS2 output.

5.19 Verify that both PS1 and PS2 are sharing load current evenly by looking at the supply current.

5.20 Disable (turn OFF) PS1, PS2 and PS3 outputs.

5.21 Enable (turn ON) PS2 output then Enable PS3 output.

5.22 Verify that the electronic load voltage reading is few millivolts below 3.3 V. This verifies that the PI2001 (U2) MOSFET (Q2) is in conduction mode.

5.23 D2 should be off. This verifies that there is no fault condition.

5.24 Reduce PS2 output voltage to 2 V,

5.25 D2 should turn on, this verifies that the circuit is in an under-voltage fault condition.

5.26 Increase PS2 output to 3.3 V, D2 should turn off, then increase PS2 output to 4 V, D2 should turn on indicating an over voltage fault condition.

5.27 Verify that Vin1 is at 0V. This verifies that the PI2001 (U1) FET (Q1) is off.

5.28 D1 should be on. This is due to a reverse voltage fault condition caused by the bus voltage being high with respect to the input voltage (Vin1).

6.0 Slave Mode: Slave Mode can be demonstrated in two setups; either by using one PI2001-EVAL1 evaluation board as a single ORing function with both PI2001 effectively in parallel or two PI2001-EVAL1 evaluation boards to demonstrate a true redundant 40A system. The following test steps use a single PI2001-EVAL1 in a slave mode application.

Note: *In this experiment U1 is configured in master mode and U2 is configured in slave mode.*

6.1 BK pin (J1) of the master device will be connected to ground [across M] while the slaved device BK pin (J3) is connected to VCC [across S]. Place a jumper across J2 to connect slave pins together.

6.2 Connect the positive terminal of PS1 power supply to Vin1. Connect the ground terminal of this power supply to Gnd. Set the power supply to 3.3 V. Keep PS1 output disabled (OFF).

6.3 Connect the positive terminal of PS2 power supply to Vin2. Connect the ground terminal of this power supply to Gnd. Set the power supply to 3.3 V. Keep PS2 output disabled (OFF).

6.4 Connect the positive terminal of PS3 power supply to Vaux1 and Vaux2. Connect the ground terminal of this power supply to Rtn1 and Rtn2. Set the power supply to 12 V. Keep PS3 output disabled (OFF).

6.5 Connect the electronic load between Vout and Gnd. Set the load current to 10 A.

6.6 Enable (Turn ON) PS2, and PS3 outputs, and keep PS1 output disabled (OFF).

6.7 Turn on the electronic load.

6.8 Verify that electronic load voltage drops to a diode drop below PS2. This verifies that the Q2 is off due to the Master (U1) not being on.

6.9 Enable (turn on) PS1 output:

6.10 Verify that the electronic load input voltage reading is a few millivolts below 3.3 V and PS1 and PS2 are sharing the load current evenly. This verifies that both MOSFET's, Q1 and Q2, are in conduction mode.

7.0 Input short circuit test

7.1 To emulate a real application, the BUS supplies for this test should have a solid output source such as DC-DC converter that supplies high current and can be connected very close to the evaluation board to reduce stray parasitic inductance. Or use the prospective supply sources of the end application where the PI2001 will be used.

7.2 Stray parasitic inductance in the circuit can contribute to significant voltage transient conditions, particularly when the MOSFET is turned-off after a reverse current fault has been detected. When a short is applied at the output of the input power sources and the . evaluation board input (Vin), a large reverse current is sourced from the evaluation board output through the ORing MOSFET. The reverse current in the MOSFET may reach over 60 A in some conditions before the MOSFET is turned off. Such high current conditions will store high energy even in a small parasitic element, and can be represented as ½ Li2. A 1 nH parasitic inductance with 60 A reverse current will generate 1.8 µJ. When the MOSFET is turned off, the stored energy will be released and will produce a high negative voltage at the MOSFET source and high positive voltage at the MOSFET drain. This event will create a high voltage difference across the drain and source of the MOSFET.

7.3 Apply a short at one of the inputs (Vin1 or Vin2) when the evaluation board is configured with both controllers (U1 and U2) in master mode. The short can be applied electronically using a MOSFET connected between Vin and Gnd or simply by connecting Vin to Gnd. Then measure the response time between when the short is applied and the MOSFET is disconnected (or turned off). An example for PI2001 response time to an input short circuit is shown in Figure 6.

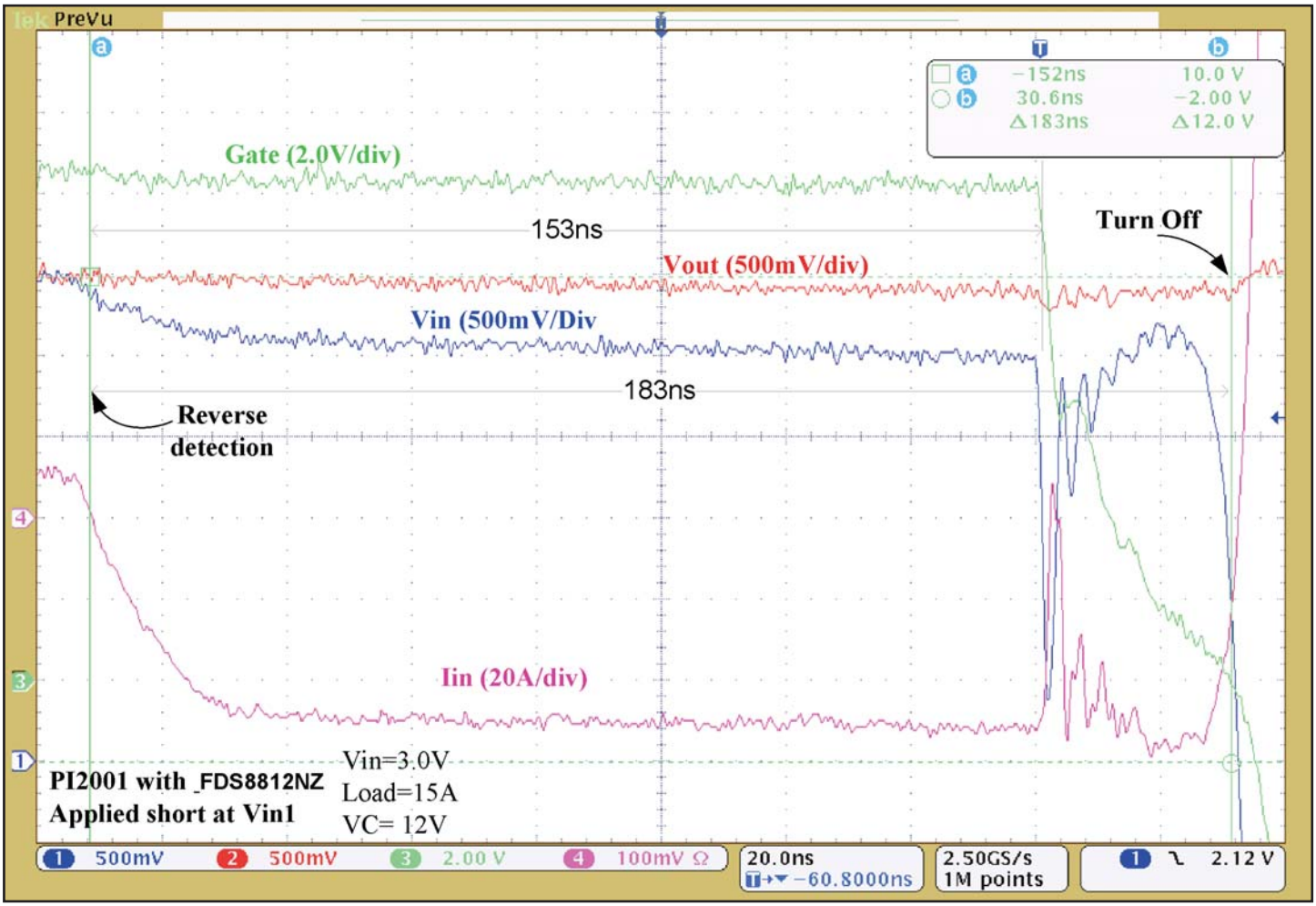


Figure 6 *– Plot of PI2001 response time to reverse current detection*

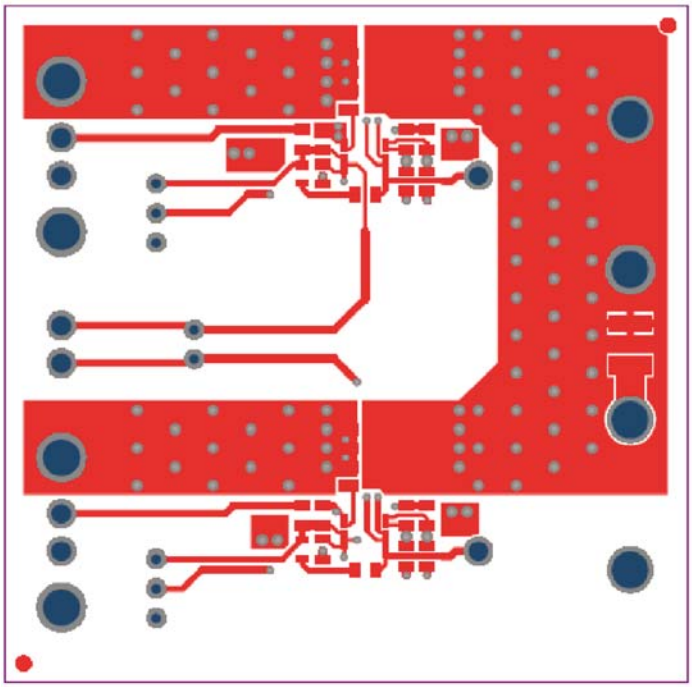


Figure 7a *– PI2001-EVAL1 layout top layer. Scale 2.0:1*

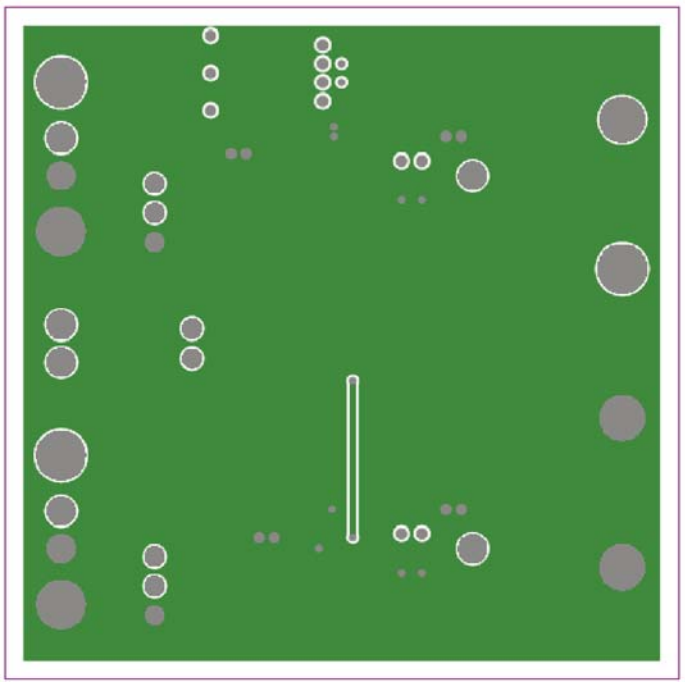


Figure 7b *– PI2001-EVAL1 layout mid layer 2. Scale 2.0:1*

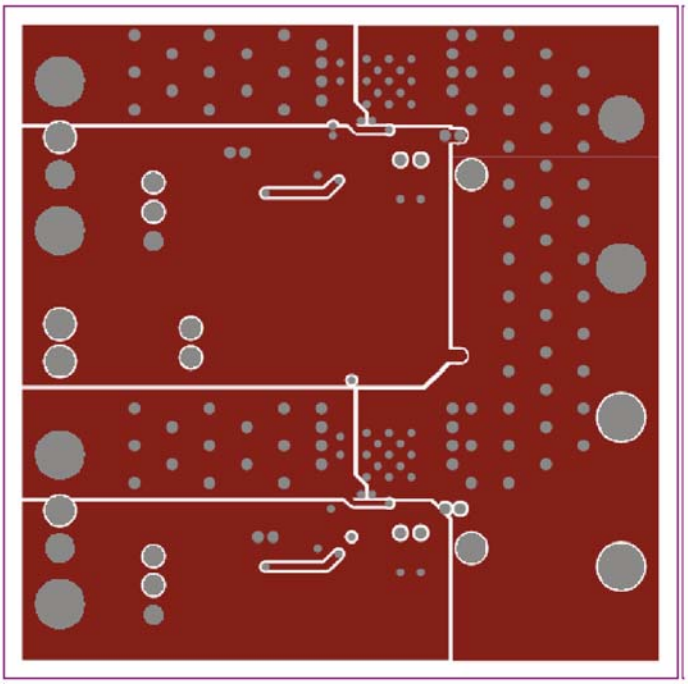


Figure 7c *– PI2001-EVAL1 layout mid layer 1. Scale 2.0:1*

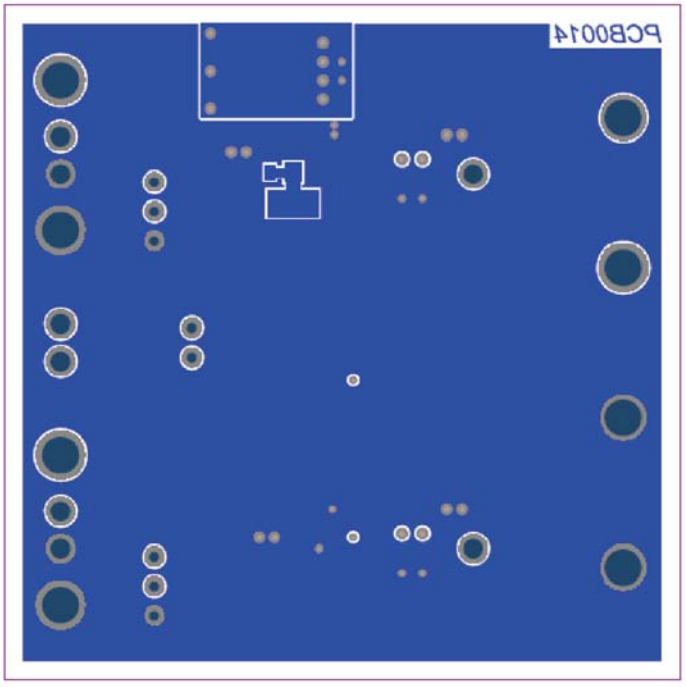
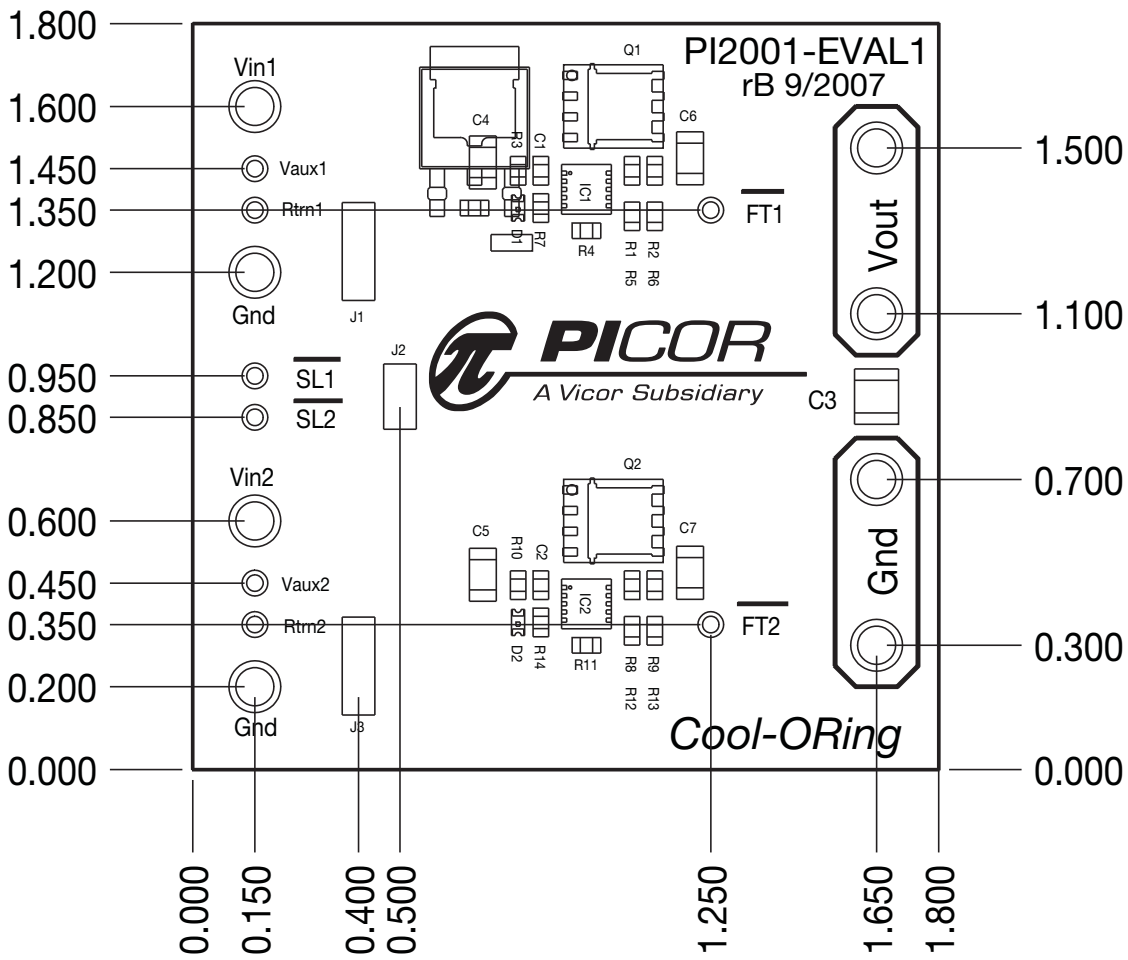


Figure 7d *– PI2001-EVAL1 layout Bottom layer. Scale 2.0:1*

Mechancial Drawing



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