PI2007-EVAL1

Cool-ORing® Series

PI2007-EVAL1 48V Bus High Side Active ORing
Evaluation Board User Guide

Content

Cool-ORing® Series

PI2007-EVAL1 Evaluation Board featuring the Cool-ORing PI2007 Active ORing controller.

The PI2007-EVAL1 Evaluation Board is intended to acquaint the user with the benefits and features of the *Cool-ORing®* PI2007 Active ORing controller. It is not designed to be installed in end-use equipment.

Please read this document before setting up the PI2007-EVAL1 Evaluation Board and refer to the PI2007 product datasheet for device specifications, functional description and characteristics.

During operation, the power devices and surrounding structures can be operated safely at high temperatures.

- Remove power and use caution when connecting and disconnecting test probes and interface lines to avoid inadvertent short circuits and contact with hot surfaces.
- When testing electronic products always use approved safety glasses. Follow good laboratory practice and procedure.

Introduction

The PI2007-EVAL1 allows the user to test the basic principles and operational characteristics of an Active ORing function in a redundant power architecture, while also experiencing the benefits and value of the PI2007 solution versus conventional Active ORing solutions. The PI2007-EVAL1 evaluation board is configured to receive two independent power source inputs, per a typical redundant power architecture, through two Active ORing channels that are combined to form a redundant power output. Each channel contains a PI2007 controller and a 100V N-channel power MOSFET. The MOSFET foot print can take an SO-8 or Power SO-8 MOSFET package. Each channel is capable of up to 6A.

The PI2007-EVAL1 evaluation board is designed with optimized PCB layout and component placement to represent a realistic high density final design for an embedded high side Active ORing solution for 48V Bus (36V to 75V) applications requiring up to 6 A. This evaluation board is intended as an easy and simple way to test the electrical and thermal performance of the PI2007 Active ORing controller.

Both dynamic and steady state testing of the PI2007 can be completed on the PI2007-EVAL1 evaluation board, in addition to using the key features of the product. Dynamic testing can be completed under a variety of system level fault conditions to check for response time to faults.

This document provides basic instructions for initial start-up and configuration of the evaluation board. Further information on the functionality of the PI2007 can be found in the PI2007 product data sheet.

Cool-ORing® PI2007 Product Description

The Cool-ORing PI2007 with an external industry standard 100V N-channel MOSFET provides a complete Active ORing solution designed for use in wide range (36V to 75V) 48V Bus redundant power system architectures. The PI2007 controller with an N-channel MOSFET enables extremely low power loss with fast dynamic response to fault conditions, critical for high availability systems.

The PI2007 controller with a low $R_{DS(on)}$ N-channel MOSFET provides very high efficiency and low power loss during steady state operation. The PI2007 controller provides an active low fault flag output to the system during excessive forward current or reverse current, or during a VC under voltage.

Figure 1 shows a photo of the PI2007-EVAL1 evaluation board, with two PI2007 controllers and two N-channel MOSFETs used to form the two Active ORing channels. The board is built with two identical Active ORing circuits with options and features that enable the user to fully explore the capabilities of the PI2007 Active ORing controller.

Terminals Maximum Rating:

Vin1, Vin2,	75Vdc/6A
	100V (100ms pulse)
Vout	75V/12A
	100V (100ms pulse)
$\overline{FT}1$, $\overline{FT}2$	-0.3V to 17.3V / 10mA
VL1, VL2 (R5=R6=1.5kΩ)*	5.5V
* VL1, VL2 voltage can be higher than 5.5V, but R5 and R6 values have to be increased to accommodate the LEDs	

Figure 1: PI2007-EVAL1 Evaluation Board PCB (1.8" x 1.8")

Terminal	Description
Vin1	**Power source Input #1** or bus input designed to accommodate up to 6A continuous current.
Vin2	**Power source Input #2** or bus input designed to accommodate up to 6A continuous current.
$\overline{FT}1$	**PI2007 (U1) Fault pin:** Monitors U1 fault conditions and level shifted to be referenced to the Rtn terminal
$\overline{FT}2$	**PI2007 (U2) Fault pin:** Monitors U2 fault conditions and level shifted to be referenced to the Rtn terminal
EN1	**PI2007 (U1) Enable**: leave open to enable the PI2007 and connect to return (Low) to disable PI2007
EN2	**PI2007 (U2) Enable:** leave open to enable the PI2007 and connect to return (Low) to disable PI2007
VL1	**Fault pin $\overline{FT}1$ LED supply**
VL2	**Fault pin $\overline{FT}2$ LED supply**
Vout	**Output:** Q1 and Q2 MOSFETs drain connection, connect to the load high side.
Rtn	**Return Connection:** Three Rtn connections are available and are connected to a common point, the Ground plane. Input supplies Vin1, Vin2, and the output load at Vout should all be connected to their respective local Rtn connection.

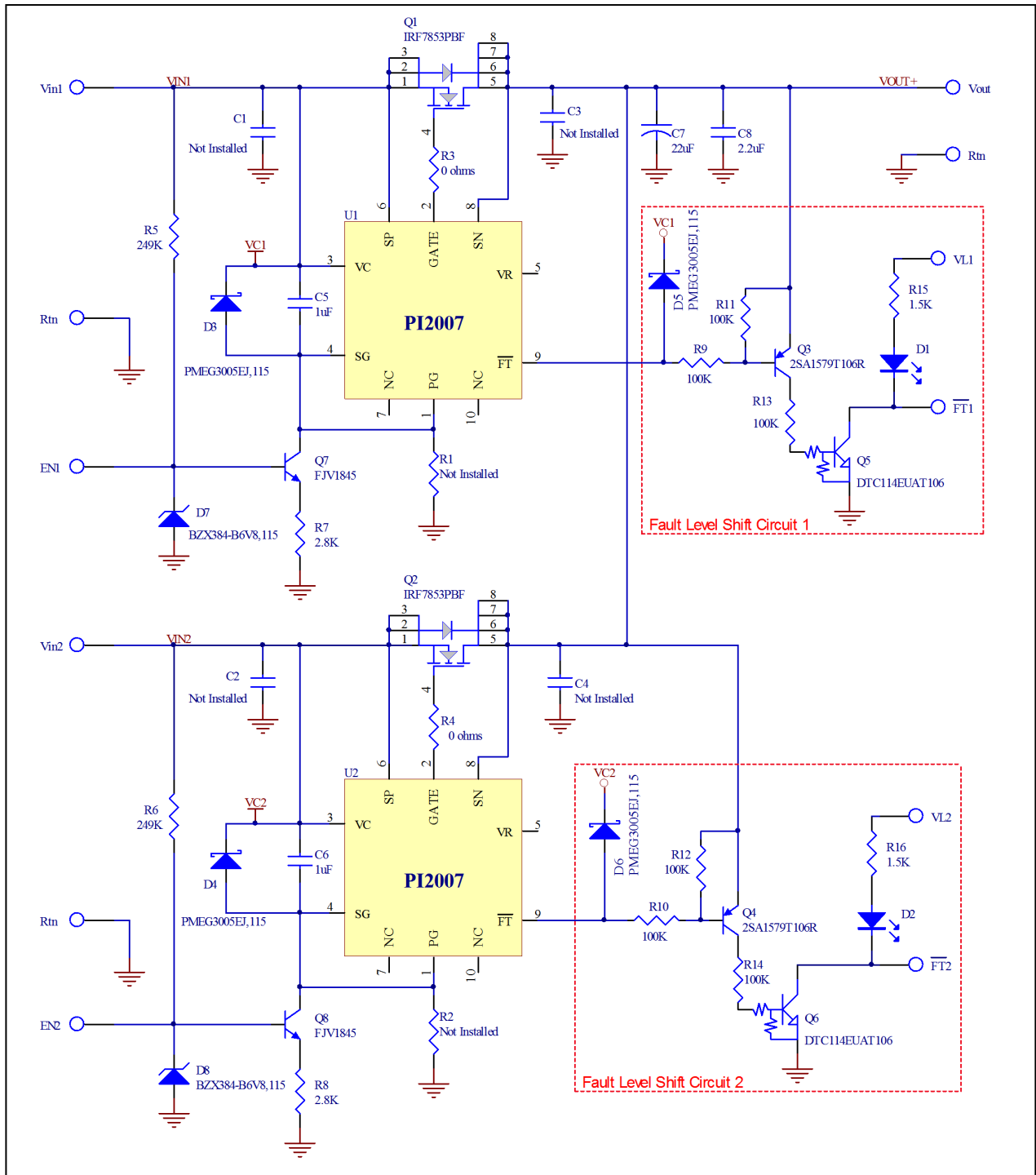**Table 1:** PI2007-EVAL1 Evaluation Board Terminals Description

Figure 2: PI2007-EVAL1 Evaluation Board schematic.

Item	QTY	Ref. Designator	Value/Part NO.	Description	Footprint	Manufacturer
1	4	C1, C2, C3, C4	Not Installed	MLCC Capacitor, X7R, 1µF,50V	1206	
2	2	C5, C6	1uF	MLCC Capacitor, X7R, 1µF,50V,	0805	
3	1	C7	22uF	Electrolytic Capacitor 22µF,100V	Panasonic _E/F	Panasonic
4	1	C8	2.2uF	MLCC Capacitor, X7R, 2.2µF,100V	1812	
5	2	D1, D2	LTST-C191CKT	LED, Red	0603 LED	Lite-On
6	4	D3, D4, D5, D6	PMEG3005EJ,115	Schottky Diode, 30V, 500mA	SOD-323	NXP
7	2	D7, D8	BZX384-B6V8,115	Zener Diode, 6.8V	SOD-323F	ON Semi
8	6	EN1, EN2, $\overline{FT}$1, $\overline{FT}$2, VL1, VL2	1528	Turret Testpoint	TURRET - 1528	Keystone Electronics
9	6	Rtn, Rtn, Rtn, Vin1, Vin2, Vout	1502	Turret Testpoint	TURRET - 1502	Keystone Electronics
10	2	Q1, Q2	IRF7853PBF	N-MOSFET,100V,8.3A	SO-8	International Rectifier
11	2	Q3, Q4	2SA1579T106R	PNP Transistor, 120V 50mA	SOT-323	Rohm
12	2	Q5, Q6	DTC114EUAT106	NPN - Pre-Biased,50V, 50mA	SOT-323	Rohm
13	2	Q7, Q8	FJV1845	NPN -Transistor, 120V, 50mA	SOT-23	Fairchild
14	2	R3, R4	0 ohms	Resistor,0 ohms,1%,0.1W	0603	
15	2	R5, R6	249K	Resistor,249K,1%,0.125W	0805	
16	2	R7, R8	2.8K	Resistor,2.8K,1%,0.1W	0603	
17	6	R9, R10, R11, R12, R13, R14	100K	Resistor,100K,1%,0.125W	0805	
18	2	R15, R16	1.5K	Resistor,1.5K,1%,0.1W	0603	
19	2	U1, U2	PI2007-00-QEIG	Picor Cool ORing Controller IC	3x3mm 10L TDFN	PICOR

Table 2: PI2007-EVAL1 Evaluation Board Bill of Materials

Ref. Designator	Value/Part NO.	Functional Description
C1, C2, C3, C4	Not Installed	Snubber capacitors to reduce voltage ringing when the device turns off. Add the capacitors if a long harnesses are used to connect the power source or load to the board.
C5, C6	1uF	VC Bypass Capacitor
C7	22uF	Output (Load) Capacitor
C8	2.2uF	Output (Load) Capacitor
D1, D2	LTST-C191CKT	To indicate a fault exists when it is on
D3, D4, D5, D6	PMEG3005EJ,115	Bypass diodes
D7, D8	BZX384-B6V8,115	Constant Current bias circuit Zener
Q7, Q8	FJV1845	Constant Current bias circuit Transistor
R5, R6	249K	Constant Current bias circuit, bias resistors
R7, R8	2.8K	Constant Current bias circuit, sets the current limiting
R15, R16	1.5K	LED current limit resistor, selected to operate at 3.3V and 5.0V logic voltage. Replace R15 and R16 with the proper resistor value for different logic voltage.
U1, U2	PI2007	Cool ORing Controller

Table 3: Component functional description

Test Procedure

Initial Test Set Up

The PI2007-EVAL1 is designed with two bias circuit options, bias resistor R_{PG} (R1 and R2) and a constant current circuit. The constant current biasing circuits are installed; where R1 and R2 are not installed.

Leave the enable inputs (EN1 and EN2) disconnected (open).

Baseline Test Procedure – PI2007 (Refer to Figure 3)

1. **Recommended Material**

    1.1. **Material Needed-Picor supplied**

        1.1.1. PI2007-EVAL1

        1.1.2. PI2007 Product Datasheet

    1.2. **Recommended Users Supplied Equipment**

        1.2.1. Two DC power supplies: 0-100V; 10A each.

        1.2.2. One low power logic voltage power supply

        1.2.3. Load: electronic Load, Power resistors or actual load.

        1.2.4. Multimeter.

        1.2.5. Oscilloscope.

        1.2.6. Appropriately sized interconnect cables.

        1.2.7. Safety glasses.

Figure 3: Layout configuration for a typical redundant power application, using the PI2007.

Before initial power-up follow these steps to configure the evaluation board for specific end application requirements:

2. **EN inputs:**

   2.1. The enable inputs (EN1 and EN2) were left unconnected (open). PI2007 devices will be enabled when the enable pins are open. To disable the PI2007, connect the enable input to return (Rtn) with a wire or with an active device (Transistor or MOSFET). **Leave EN1 and EN2 unconnected for the initial test.**

3. **Control Circuitry Bias:**

   3.1. The PI2007 control circuitry and the gate driver for the MOSFET are biased through the VC pin. An internal regulator clamps VC pin voltage with respect to the PG pin (VC-PG), to 11.7V typically. A bias resistor R_{PG} (R1 and R2) or a Constant Current bias circuit is required if the voltage at the VC pin is higher than the minimum Voltage Clamp (V_{VC-CLM}, 11V). PI2007-EVAL1 has both circuits laid out. The constant current bias circuit components are installed while R_{PG} is not installed.

   3.2. If R_{PG} is desired instead of the constant current bias circuit to save components: remove the constant current bias circuit components from the evaluation board. The constant current bias circuit components for upper ORing (U1) are Q7, R5, R7 and D7, the constant current bias circuit components for lower ORing (U2) are Q8, R6, R8 and D8. The R_{PG} value can be selected using the following equations:

   $$R_{PG} = \frac{V_{VC\,min} - V_{VC-SGND\,Max}}{I_{VC\,max} + 0.1mA}$$

   And R_{PG} maximum power dissipation is:

   $$Pd_{RPG} = \frac{(V_{VC\,max} - V_{VC-SGND\,Min})^2}{R_{PG}}$$

   Where:
   $V_{VC\,min}$:   VC pin minimum applied voltage (Vin to Rtn)
   $V_{VC\,max}$:   VC pin maximum applied voltage (Vin to Rtn)

$V_{VC-SGND\,Max}$: Controller maximum clamp voltage, 12.5V
$V_{VC-SGND\,Min}$: Controller minimum clamp voltage, 11V
$I_{VC\,max}$:   Controller maximum bias current, use 2.0mA
0.1mA :   0.1mA is added for margin

R_{PG} calculation example

Vin (minimum) = 40V and Vin (maximum) = 50V

$$R_{PG} = \frac{V_{VC\,min} - V_{VC-SGND\,Max}}{I_{VC\,max} + 0.1mA}$$

$$R_{PG} = \frac{40V - 12.5V}{2.1mA} = 13.1K\Omega$$

$$Pd_{RPG} = \frac{(V_{VC\,max} - V_{VC-SGND\,Min})^2}{R_{PG}}$$

$$Pd_{RPG} = \frac{(50V - 11V)^2}{13.1K\Omega} = 116mW$$

4. **Hook Up of the Evaluation Board**

   4.1. Connect the positive terminal of PS1 power supply to Vin1. Connect the ground terminal of PS1 to its local Rtn. Set the power supply to 48V. **Keep PS1 output disabled, off.**

   4.2. Connect the positive terminal of PS2 power supply to Vin2. Connect the ground terminal of PS2 to its local Rtn. Set the power supply to 48V. **Keep PS2 output disabled, off.**

   4.3. Connect the logic power supply PS3 positive terminal to VL1 and VL2. Connect the ground terminal of this power supply to a Rtn terminal. Set the power supply to the desired logic voltage level, 3.3V or 5V. **Keep PS3 output disabled, off.**

   4.4. Connect the electronic load to the output between Vout and its local Rtn. Set the load current to 5A.

   4.5. Enable (turn on) PS1 power supply output.

   4.6. Enable (turn on) PS3 power supply output.

   4.7. Turn on the electronic load.

   4.8. Verify that the electronic load voltage reading increases to a few millivolts below 48V. This verifies that the MOSFET Q1 is in conduction mode.

4.9. Verify that Vin2 is low. This verifies that the Q2 MOSFET is off.

4.10. D2 should be on. This is due to a reverse voltage fault condition caused by the bus voltage being high with respect to the input voltage (Vin2).

4.11. Enable (turn on) PS2 output.

4.12. Verify that both PS1 and PS2 are sharing load current evenly by looking at the supply current. *Power supplies output may need adjustment to set current sharing between the supplies.*

4.13. Disable (turn off) PS1, PS2, and PS3 outputs.

4.14. Enable (turn on) PS2 output then Enable PS3 outputs.

4.15. Verify that the electronic load voltage reading is few millivolts below 48V. This verifies that the MOSFET is in conduction mode.

4.16. D2 should be off. This verifies that there is no fault condition.

4.17. Verify that Vin1 is low. This verifies that the MOSFET Q1 is off.

4.18. D1 should be on. This is due to a reverse voltage fault condition caused by the bus voltage being high with respect to the input voltage (Vin1).

5. Input short circuit test:

PI2007 has a very fast response (80ns) to a reverse current (Input short) fault condition. Measuring a short period event requires attention to the test set-up. Before proceeding, consider the following:

5.1. To emulate a real application, the BUS supplies for this test should have a solid output source such as a DC-DC converter that supplies high current and can be connected very close to the evaluation board to reduce stray parasitic inductance, or use the prospective supply sources of the end application where the PI2007 will be used. Typical bench power supplies have slow response to output load change. In this test when the power supply output is shorted and then released, the bench power supply may produce high output voltage with high current capability that may damage the device under test.

5.2. Do not install Input capacitors (C1 and/or C2) in this test.

5.3. Output capacitor (C7) should be installed.

5.4. Place the scope probes very close to the MOSFET drain and source to measure Vout and Vin, and make sure that the scope ground leads are very short. You may use a close by ground pad for the scope probe return, such as C1, C2, C3 and C4 Rtn pads.

5.5. Apply a short at one of the inputs (Vin1 or Vin2) when both controllers (U1 and U2) are on, PS1 and PS2 are enabled. The short can be applied electronically using a MOSFET connected between Vin and Rtn or simply by connecting Vin to Rtn. Then measure the response time between when the short being applied and the MOSFET being disconnected (or turned off). An example for PI2007 response time to an input short circuit is shown in Figure 4.
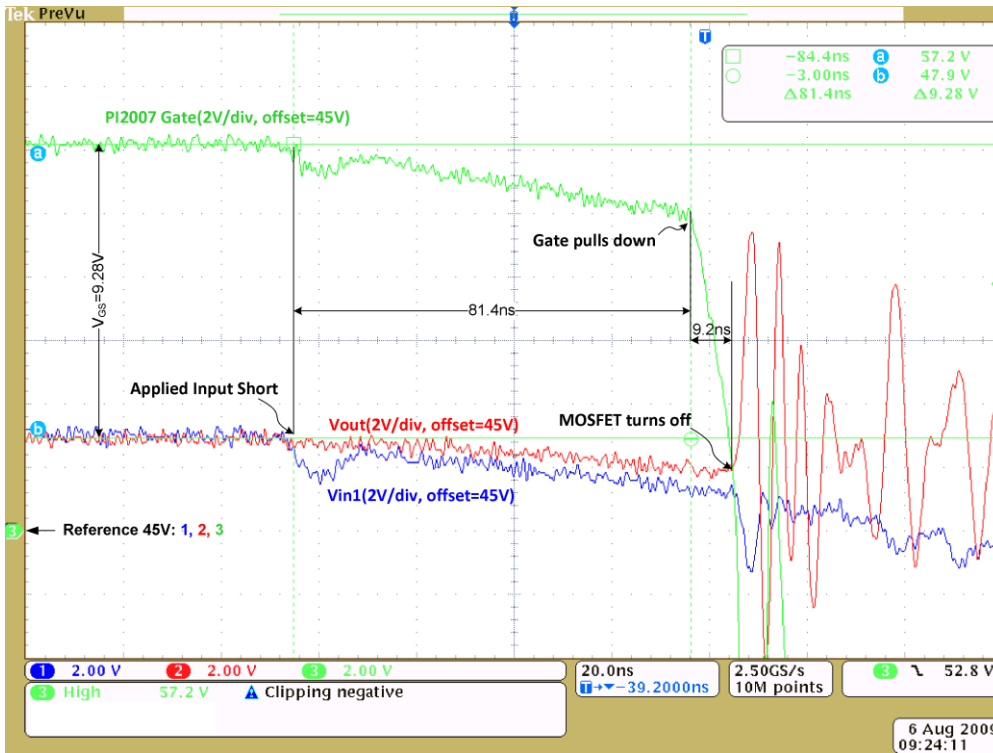
Test Setup:
DUT: PI2007-EVAL1
Vin1 = 48V
Vin2 = 48V
Output Load = 6A

Test:
Both input sources are turned on and sharing the load current, then applied a short for **1ms** with a fast turn on MOSFET between Vin1 and Rtn.

Test purpose:
To show the PI2007 response to a fault condition, where the output of the input source is shorted or tried to source current from the load (Vout)

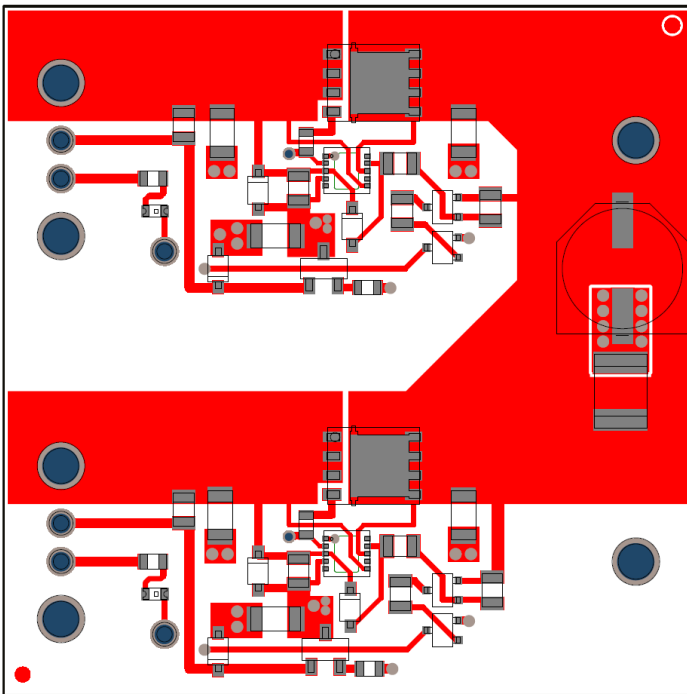**Figure 4:** Plot of PI2007 response time to reverse current detection

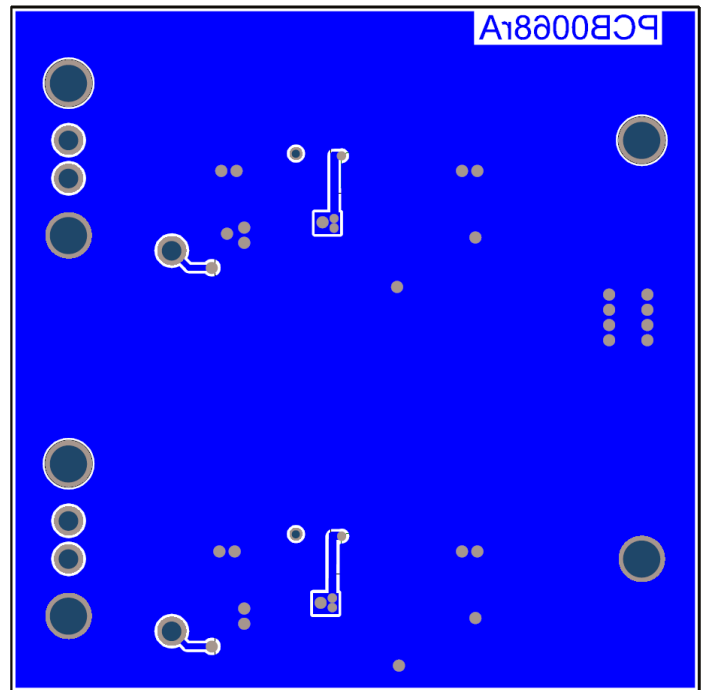**Figure 5:** PI2007-EVAL1 layout top layer. Scale 2.0:1

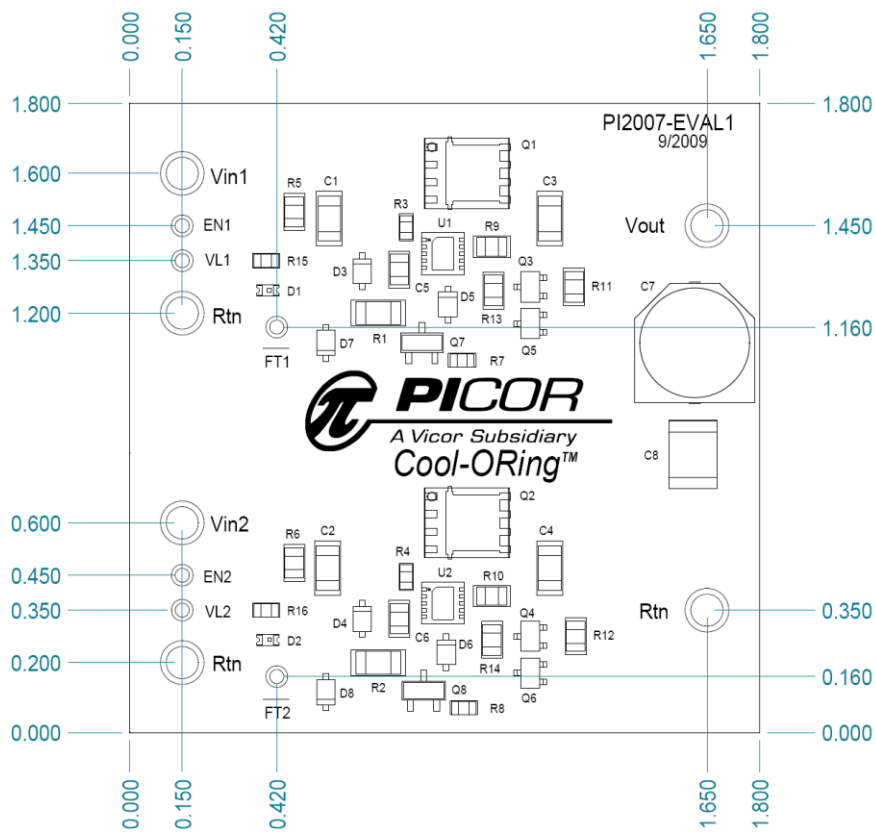**Figure 6:** PI2007-EVAL1 layout bottom layer 2. Scale 2.0:1

Figure 7: PI2007-EVA1 evaluation board mechanical drawing.

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