

8 – 36V_{IN} ZVS Buck Regulator Family

Product Description

The PI33xx is a family of high-efficiency, wide-input-range DC-DC ZVS Buck regulators integrating controller, power switches and support components all within a high-density System-in-Package (SiP). The integration of a high-performance Zero-Voltage Switching (ZVS) topology, within the PI33xx series, increases point-of-load performance providing best-in-class power efficiency. The PI33xx requires only an external inductor and minimal capacitors to form a complete DC-DC switching-mode Buck Regulator.

| Device | Output Voltage | | I _{OUT} Max |
|---------------------------|----------------|--------------|----------------------|
| | Set | Range | |
| PI3301-01 | 3.3V | 2.3 – 4.1V | 15A |
| PI3301-00 | 3.3V | 2.3 – 4.1V | 10A |
| PI3302-00 | 5.0V | 3.3 – 6.5V | 10A |
| PI3303-00 | 12V | 6.5 – 13.0V | 8A |
| PI3305-00 | 15V | 10.0 – 16.0V | 8A |

The ZVS architecture also enables high-frequency operation while minimizing switching losses and maximizing efficiency. The high-switching-frequency operation reduces the size of the external filtering components, improves power density, and enables very fast dynamic response to line and load transients. The PI33xx series sustains high switching frequency all the way up to the rated input voltage without sacrificing efficiency and, with its 20ns minimum on-time, supports large step-down conversions up to 36V_{IN}.



Features & Benefits

- High-efficiency ZVS Buck topology
- Wide input voltage range of 8 – 36V
- Very-fast transient response
- High-accuracy pre-trimmed output voltage
- User-adjustable soft start & tracking
- Power-up into pre-biased load (select versions)
- Parallel capable with single-wire current sharing
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- –40 to 125°C operating range (T_J)
- Standard I²C™ functionality & programmability:
 - V_{OUT} margining
 - Fault reporting
 - Enable and SYNCI pin polarity
 - Phase delay (interleaving multiple regulators)

Applications

- High-Efficiency Systems
- High-Voltage Battery Operation

Package Information

- 10 x 14 x 2.6mm LGA SiP

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Order Information

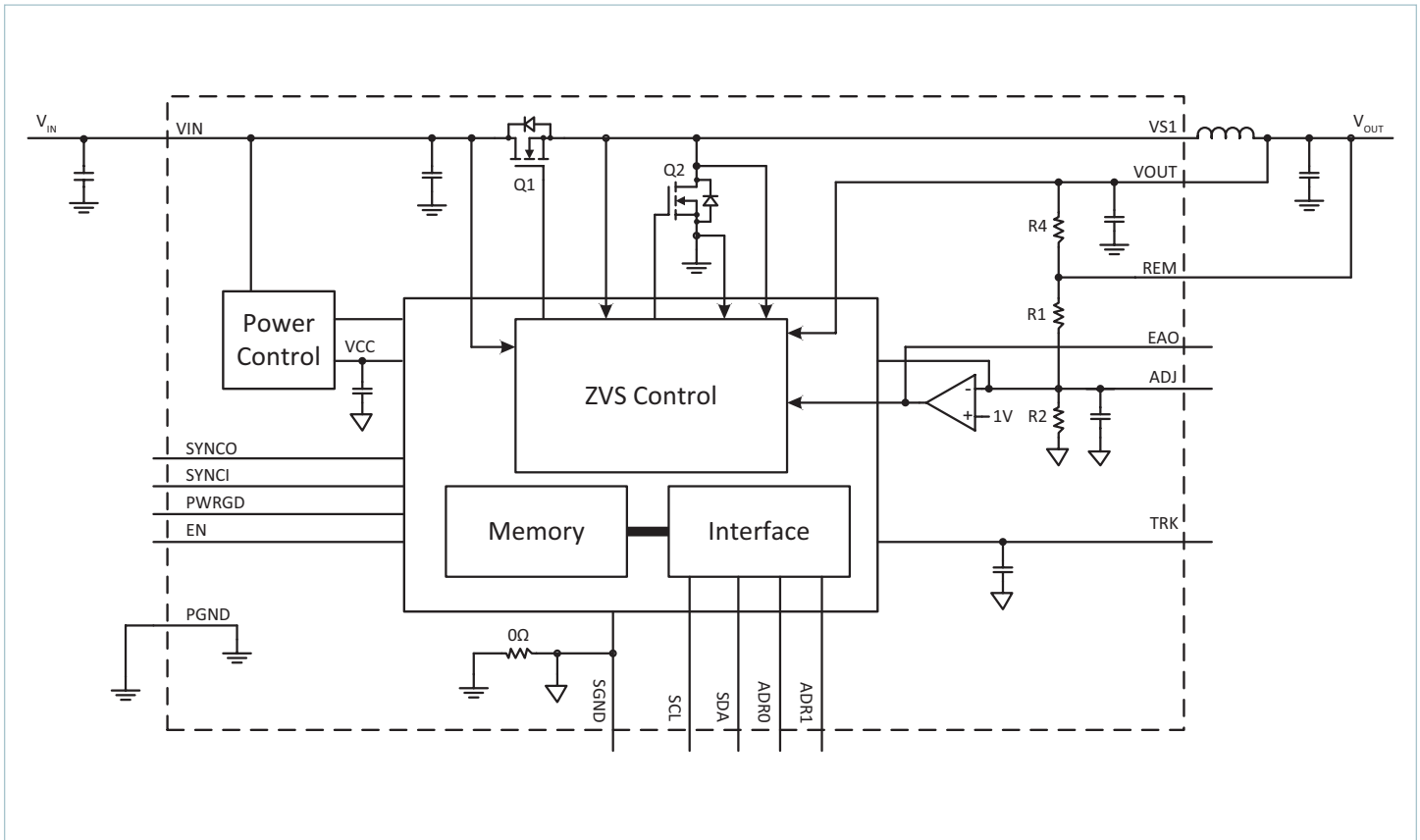
| Part Number | Output Range | | I _{OUT} Max | Package | Transport Media |
|----------------|--------------|--------------|----------------------|-----------------------|-----------------|
| | Set | Range | | | |
| PI3301-01-LGIZ | 3.3V | 2.3 – 4.1V | 15A | 10 x 14mm 123-pin LGA | TRAY |
| PI3301-00-LGIZ | 3.3V | 2.3 – 4.1V | 10A | 10 x 14mm 123-pin LGA | TRAY |
| PI3302-00-LGIZ | 5.0V | 3.3 – 6.5V | 10A | 10 x 14mm 123-pin LGA | TRAY |
| PI3303-00-LGIZ | 12V | 6.5 – 13.0V | 8A | 10 x 14mm 123-pin LGA | TRAY |
| PI3305-00-LGIZ | 15V | 10.0 – 16.0V | 8A | 10 x 14mm 123-pin LGA | TRAY |

Absolute Maximum Ratings

| Name | Rating |
|--|--|
| VIN | -0.7 to 36V |
| VS1 | -0.7 to 36V _{DC} |
| SGND | 100mA |
| PWRGD, SYNCO, SYNCI, EN, EAO, ADJ, TRK, ADR1, ADR2, SCL, SDA | -0.3 to 5.5V / 5mA |
| VOUT, REM | PI3301-xx-LGIZ PI3302-00-LGIZ PI3303-00-LGIZ PI3305-00-LGIZ |
| | -1.0 to 18V |
| | -1.5 to 21V |
| | -3.6 to 25V |
| | -4.5 to 25V |
| Storage Temperature | -65 to 150°C |
| Operating Junction Temperature | -40 to 125°C |
| Soldering Temperature for 20 seconds | 245°C |
| ESD Rating | 2kV HBM, 1kV CDM |

Notes: At 25°C ambient temperature. Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted. Test conditions are per the specifications within the individual product electrical characteristics.

Functional Block Diagram

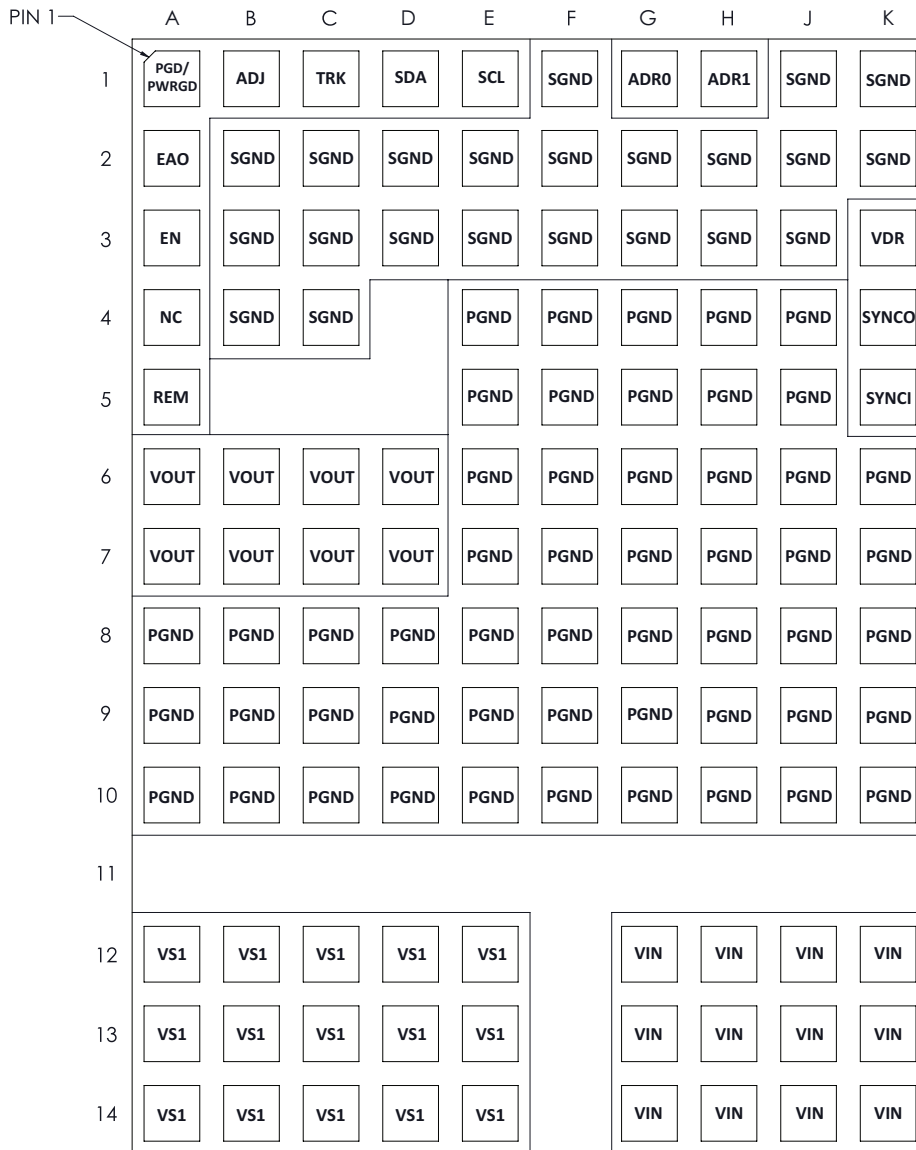


Simplified block diagram

Pin Description

| Pin Name | Number | Description |
|----------|---------|--|
| SGND | Block 1 | Signal Ground: Internal logic ground for EA, TRK, SYNCI, SYNCO, ADJ and I ² C™ (options) communication returns. SGND and PGND are star connected within the regulator package. |
| PGND | Block 2 | Power Ground: VIN and VOUT power returns. |
| VIN | Block 3 | Input Voltage: and sense for UVLO, OVLO and feed-forward ramp. |
| VOUT | Block 5 | Output Voltage: and sense for power switches and feed-forward ramp. |
| VS1 | Block 4 | Switching Node: and ZVS sense for power switches. |
| PWRGD | A1 | Power Good: High impedance when regulator is operating and V _{OUT} is in regulation. Otherwise pulls to SGND. Also can be used for parallel timing management intended for lead regulator. |
| EAO | A2 | Error Amp Output: External connection for additional compensation and current sharing. |
| EN | A3 | Enable Input: Regulator enable control. Asserted high or left floating – regulator enabled; Asserted low, regulator output disabled. Polarity is programmable via I ² C interface. |
| REM | A5 | Remote Sense: High-side connection. Connect to output regulation point. |
| ADJ | B1 | Adjust Input: An external resistor may be connected between ADJ pin and SGND or VOUT to trim the output voltage up or down. |
| TRK | C1 | Soft-Start and Track Input: An external capacitor may be connected between TRK pin and SGND to decrease the rate of rise during soft start. |
| NC | A4 | No Connect: Leave pins floating. |
| VDR | K3 | VDR can only be used for ADR0 and ADR1 pull-up reference voltage. No other external loading is permitted |
| SYNCO | K4 | Synchronization Output: Outputs a low signal for ½ of the minimum period for synchronization of other converters. |
| SYNCI | K5 | Synchronization Input: Synchronize to the falling edge of external clock frequency. SYNCI is a high-impedance digital input node and should always be connected to SGND when not in use. |
| SDA | D1 | Data Line: Connect to SGND for I ² C applications. |
| SCL | E1 | Clock Line: Connect to SGND for I ² C applications. |
| ADR1 | H1 | Tri-state Address: No connect for I ² C applications. |
| ADR0 | G1 | Tri-state Address: No connect for I ² C applications. |

Package Pinout



TOP THROUGH VIEW OF PRODUCT

| Pin Block Name | Group of pins |
|----------------|--|
| SGND | B2-4, C2-4, D2-3, E2-3, F1-3, G2-3, H2-3, J1-3, K1-2 |
| PGND | A8-10, B8-10, C8-10, D8-10, E4-10, F4-10, G4-10, H4-10, J4-10, K6-10 |
| VIN | G12-14, H12-14, J12-14, K12-14 |
| VS1 | A12-14, B12-14, C12-14, D12-14, E12-14 |
| VOUT | A6-7, B6-7, C6-7, D6-7 |

PI3301-01-LGIZ (3.3V_{OUT}) Electrical Characteristics

Unless otherwise specified: $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $V_{IN} = 24\text{V}$, $L1 = 155\text{nH}$ [a]

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|-----------------------------------|---|----------|------|------|--------------------|
| Input Specifications | | | | | | |
| Input Voltage | V_{IN_DC} | [g] | 8 | 24 | 36 | V |
| Input Current | I_{IN_DC} | $V_{IN} = 24\text{V}$, $T_C = 25^{\circ}\text{C}$, $I_{OUT} = 15\text{A}$ | | 2.25 | | A |
| Input Current At Output Short (fault condition duty cycle) | I_{IN_Short} | [b] | | | 75 | mA |
| Input Quiescent Current | I_{Q_VIN} | Disabled | | 2.0 | | mA |
| | | Enabled (no load) | | 2.5 | | |
| Input Voltage Slew Rate | V_{IN_SR} | [b] | | | 1 | V / μs |
| Output Specifications | | | | | | |
| Output Voltage Total Regulation | V_{OUT_DC} | [b] | 3.25 | 3.30 | 3.36 | V |
| Output Voltage Trim Range | V_{OUT_DC} | [c] [g] | 2.3 | 3.3 | 4.1 | V |
| Line Regulation | $\Delta V_{OUT} (\Delta V_{IN})$ | At 25°C , $8\text{V} < V_{IN} < 36\text{V}$ | | 0.10 | | % |
| Load Regulation | $\Delta V_{OUT} (\Delta I_{OUT})$ | At 25°C , $0.5\text{A} < I_{OUT} < 15\text{A}$ | | 0.10 | | % |
| Output Voltage Ripple | V_{OUT_AC} | $I_{OUT} = 5\text{A}$, $C_{OUT} = 4 \times 100\mu\text{F}$, 20MHz BW [d] | | 37.5 | | mV _{P-P} |
| Continuous Output Current Range | I_{OUT_DC} | [e] [g] | 0 | | 15 | A |
| Current Limit | I_{OUT_CL} | | | 18.0 | | A |
| Protection | | | | | | |
| V_{IN} UVLO Start Threshold | V_{UVLO_START} | | 7.10 | 7.60 | 8.00 | V |
| V_{IN} UVLO Stop Threshold | V_{UVLO_STOP} | | 6.80 | 7.25 | 7.60 | V |
| V_{IN} UVLO Hysteresis | V_{UVLO_HYS} | | | 0.35 | | V |
| V_{IN} OVLO Start Threshold | V_{OVLO_START} | | 36.1 | 37.6 | | V |
| V_{IN} OVLO Stop Threshold | V_{OVLO_STOP} | | 37.0 | 38.4 | | V |
| V_{IN} OVLO Hysteresis | V_{OVLO_HYS} | | | 0.8 | | V |
| V_{IN} UVLO/OVLO Fault Delay Time | t_{f_DLY} | Number of the switching frequency cycles | | | 128 | Cycles |
| V_{IN} UVLO/OVLO Response Time | t_f | 1% overdrive | | 500 | | ns |
| Output Overvoltage Protection | V_{OVP} | Above V_{OUT} | | 20 | | % |
| Overtemperature Fault Threshold | T_{OTP} | [b] | 130 | 135 | 140 | $^{\circ}\text{C}$ |
| Overtemperature Restart Hysteresis | T_{OTP_HYS} | | | 30 | | $^{\circ}\text{C}$ |

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

[c] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

[d] Refer to Output Ripple plots.

[e] Refer to Load Current vs. Ambient Temperature curves.

[f] Refer to Switching Frequency vs. Load current curves.

[g] Minimum 5V between $V_{IN} - V_{OUT}$ must be maintained or a minimum load of 1mA required.

PI3301-01-LGIZ (3.3V_{OUT}) Electrical Characteristics (Cont.)

Unless otherwise specified: $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $V_{IN} = 24\text{V}$, $L1 = 155\text{nH}$ ^[a]

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|--------------------|--|-----|-----|------|---------------|
| Timing | | | | | | |
| Switching Frequency | f_S | ^[f] | | 650 | | kHz |
| Fault Restart Delay | t_{FR_DLY} | | | 30 | | ms |
| Sync In (SYNCI) | | | | | | |
| Synchronization Frequency Range | Δf_{SYNCI} | Relative to set switching frequency ^[c] | 50 | | 110 | % |
| SYNCI Threshold | V_{SYNCI} | | | 2.5 | | V |
| Sync Out (SYNCO) | | | | | | |
| SYNCO High | V_{SYNCO_HI} | Source 1mA | 4.5 | | | V |
| SYNCO Low | V_{SYNCO_LO} | Sink 1mA | | | 0.5 | V |
| SYNCO Rise Time | t_{SYNCO_RT} | 20pF load | | 10 | | ns |
| SYNCO Fall Time | t_{SYNCO_FT} | 20pF load | | 10 | | ns |
| Soft Start And Tracking | | | | | | |
| TRK Active Input Range | V_{TRK} | Internal reference tracking range | 0 | | 1.04 | V |
| TRK Max Output Voltage | V_{TRK_MAX} | | | 1.2 | | V |
| TRK Disable Threshold | V_{TRK_OV} | | 20 | 40 | 62 | mV |
| Charge Current (Soft Start) | I_{TRK} | | 70 | 50 | 25 | μA |
| Discharge Current (Fault) | I_{TRK_DIS} | | | 6.8 | | mA |
| Soft-Start Time | t_{SS} | $C_{TRK} = 0\mu\text{F}$ | | 2.2 | | ms |
| Enable | | | | | | |
| High Threshold | V_{EN_HI} | | 0.9 | 1 | 1.1 | V |
| Low Threshold | V_{EN_LO} | | 0.7 | 0.8 | 0.9 | V |
| Threshold Hysteresis | V_{EN_HYS} | | 100 | 200 | 300 | mV |
| Enable Pull-Up Voltage (floating, unfaulted) | V_{EN_PU} | | | 2 | | V |
| Enable Pull-Down Voltage (floating, faulted) | V_{EN_PD} | | | 0 | | V |
| Source Current | I_{EN_SO} | | | -50 | | μA |
| Sink Current | I_{EN_SK} | | | 50 | | μA |

^[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

^[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

^[c] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

^[d] Refer to Output Ripple plots.

^[e] Refer to Load Current vs. Ambient Temperature curves.

^[f] Refer to Switching Frequency vs. Load current curves.

^[g] Minimum 5V between $V_{IN} - V_{OUT}$ must be maintained or a minimum load of 1mA required.

PI3301-01-LGIZ (3.3V_{OUT}) Electrical Characteristics (Cont.)

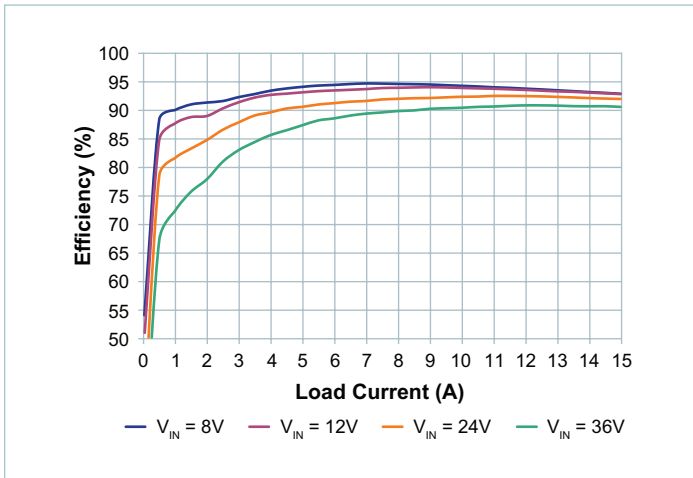


Figure 1 — Efficiency at 25°C

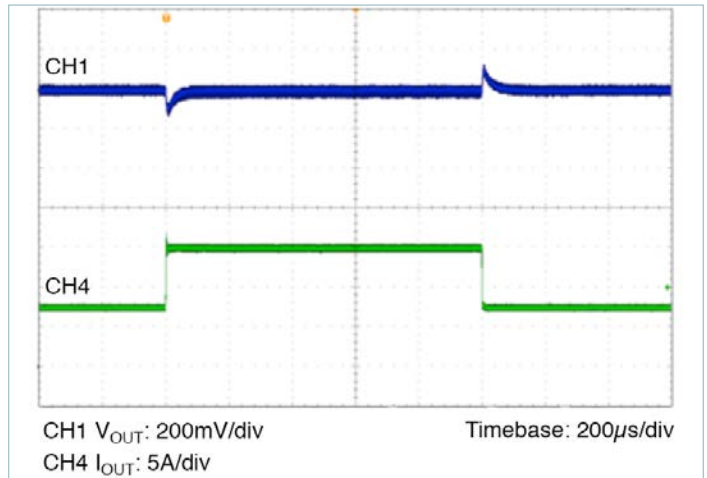


Figure 4 — Transient response 7.5A to 15A, at 5A/µs
24V_{IN} to 3.3V_{OUT}, C_{OUT} = 8 x 100µF ceramic

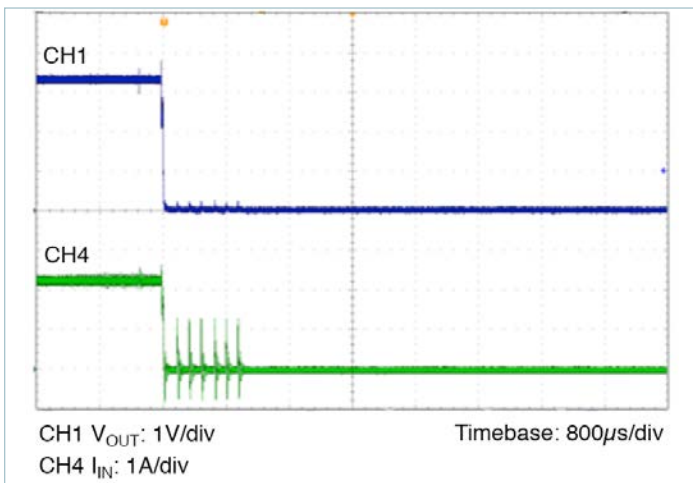


Figure 2 — Short circuit test

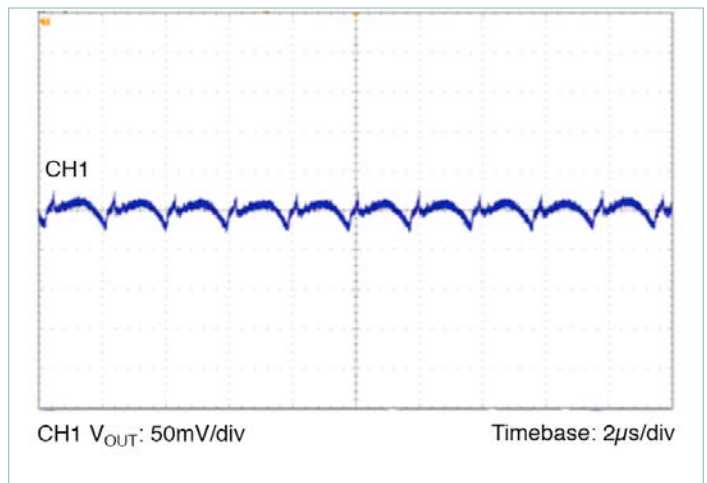


Figure 5 — Output ripple 24V_{IN}, 3.3V_{OUT} at 15A
C_{OUT} = 8 x 100µF ceramic

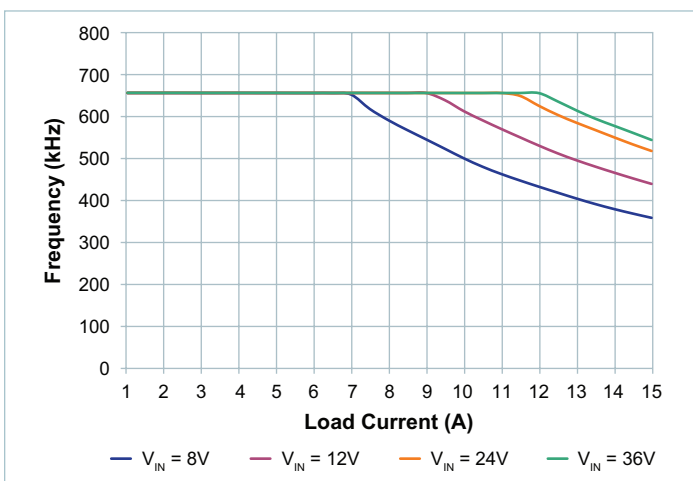


Figure 3 — Switching frequency vs. load current

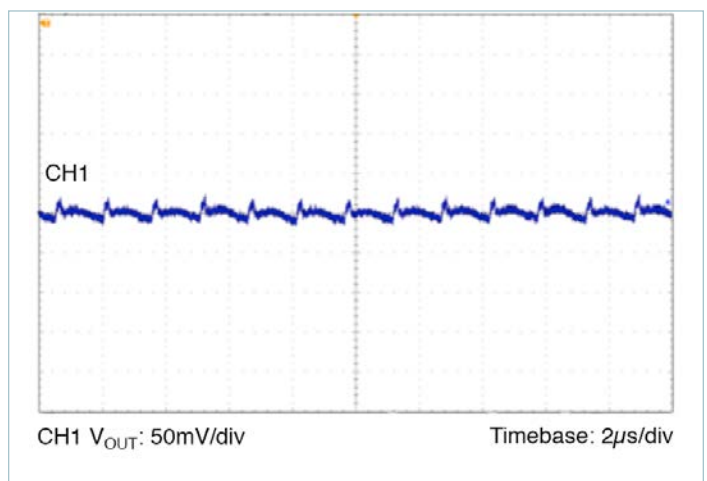


Figure 6 — Output ripple 24V_{IN}, 3.3V_{OUT} at 7.5A
C_{OUT} = 8 x 100µF ceramic

PI3301-00-LGIZ (3.3V_{OUT}) Electrical Characteristics

Unless otherwise specified: $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $V_{IN} = 24\text{V}$, $L1 = 200\text{nH}$ ^[a]

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|-----------------------------------|---|------|------|------|--------------------|
| Input Specifications | | | | | | |
| Input Voltage | V_{IN_DC} | [g] | 8 | 24 | 36 | V |
| Input Current | I_{IN_DC} | $V_{IN} = 24\text{V}$, $T_C = 25^{\circ}\text{C}$, $I_{OUT} = 10\text{A}$ | | 1.49 | | A |
| Input Current at Output Short (Fault Condition Duty Cycle) | I_{IN_Short} | [b] | | | 20 | mA |
| Input Quiescent Current | I_{Q_VIN} | Disabled | | 2.0 | | mA |
| | | Enabled (no load) | | 2.5 | | mA |
| Input Voltage Slew Rate | V_{IN_SR} | [b] | | | 1 | V/ μs |
| Output Specifications | | | | | | |
| Output Voltage Total Regulation | V_{OUT_DC} | [b] | 3.25 | 3.30 | 3.36 | V |
| Output Voltage Trim Range | V_{OUT_DC} | [c] [g] | 2.3 | 3.3 | 4.1 | V |
| Line Regulation | $\Delta V_{OUT} (\Delta V_{IN})$ | At 25°C , $8\text{V} < V_{IN} < 36\text{V}$ | | 0.10 | | % |
| Load Regulation | $\Delta V_{OUT} (\Delta I_{OUT})$ | At 25°C , $0.5\text{A} < I_{OUT} < 10\text{A}$ | | 0.10 | | % |
| Output Voltage Ripple | V_{OUT_AC} | $I_{OUT} = 5\text{A}$, $C_{OUT} = 4 \times 100\mu\text{F}$, 20MHz BW ^[d] | | 37.5 | | mV _{P-P} |
| Continuous Output Current Range | I_{OUT_DC} | [e] | | | 10 | A |
| Current Limit | I_{OUT_CL} | | | 12 | | A |
| Protection | | | | | | |
| V_{IN} UVLO Start Threshold | V_{UVLO_START} | | 7.10 | 7.60 | 8.00 | V |
| V_{IN} UVLO Stop Threshold | V_{UVLO_STOP} | | 6.80 | 7.25 | 7.60 | V |
| V_{IN} UVLO Hysteresis | V_{UVLO_HYS} | | | 0.33 | | V |
| V_{IN} OVLO Start Threshold | V_{OVLO_START} | | 36.1 | | | V |
| V_{IN} OVLO Stop Threshold | V_{OVLO_STOP} | | 37.0 | 38.4 | | V |
| V_{IN} OVLO Hysteresis | V_{OVLO_HYS} | | | 0.77 | | V |
| V_{IN} UVLO/OVLO Response Time | t_f | 1% overdrive | | 500 | | ns |
| Output Overvoltage Protection | V_{OVP} | Above V_{OUT} | | 20 | | % |
| Overtemperature Fault Threshold | T_{OTP} | | 130 | 135 | 140 | $^{\circ}\text{C}$ |
| Overtemperature Restart Hysteresis | T_{OTP_HYS} | | | 30 | | $^{\circ}\text{C}$ |

^[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

^[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

^[c] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

^[d] Refer to Output Ripple plots.

^[e] Refer to load current vs. ambient temperature curves.

^[f] Refer to switching frequency vs. load current curves.

^[g] Minimum 5V between V_{IN} - V_{OUT} must be maintained or a minimum load of 1mA required.

PI3301-00-LGIZ (3.3V_{OUT}) Electrical Characteristics (Cont.)

Unless otherwise specified: $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $V_{IN} = 24\text{V}$, $L1 = 200\text{nH}$ ^[a]

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|--------------------|--|-----|-----|------|---------------|
| Timing | | | | | | |
| Switching Frequency | f_S | ^[f] | | 650 | | kHz |
| Fault Restart Delay | t_{FR_DLY} | | | 30 | | ms |
| Sync In (SYNCI) | | | | | | |
| Synchronization Frequency Range | Δf_{SYNCI} | Relative to set switching frequency ^[c] | 50 | | 110 | % |
| SYNCI Threshold | V_{SYNCI} | | | 2.5 | | V |
| SYNCI Input Impedance | Z_{SYNCI} | | | 100 | | k Ω |
| Sync Out (SYNCO) | | | | | | |
| SYNCO High | V_{SYNCO_HI} | Source 1mA | 4.5 | | | V |
| SYNCO Low | V_{SYNCO_LO} | Sink 1mA | | | 0.5 | V |
| SYNCO Rise Time | t_{SYNCO_RT} | 20pF load | | 10 | | ns |
| SYNCO Fall Time | t_{SYNCO_FT} | 20pF load | | 10 | | ns |
| Soft Start And Tracking | | | | | | |
| TRK Active Input Range | V_{TRK} | Internal reference tracking range | 0 | | 1.04 | V |
| TRK Max Output Voltage | | | | 1.2 | | V |
| TRK Disable Threshold | V_{TRK_OV} | | 20 | 40 | 62 | mV |
| Charge Current (Soft-Start) | I_{TRK} | | 70 | 50 | 25 | μA |
| Discharge Current (Fault) | I_{TRK_DIS} | $V_{TRK} = 0.5\text{V}$ | | 6.8 | | mA |
| Soft-Start Time | t_{SS} | $C_{TRK} = 0\mu\text{F}$ | | 2.2 | | ms |
| Enable | | | | | | |
| High Threshold | V_{EN_HI} | | 0.9 | 1 | 1.1 | V |
| Low Threshold | V_{EN_LO} | | 0.7 | 0.8 | 0.9 | V |
| Threshold Hysteresis | V_{EN_HYS} | | 100 | 200 | 300 | mV |
| Enable Pull-Up Voltage (Floating) | V_{EN_PU} | With positive logic EN polarity | | 2 | | V |
| Enable Pull-Down Voltage (Floating) | V_{EN_PD} | With negative logic EN polarity | | 0 | | V |
| Source Current | I_{EN_SO} | With positive logic EN polarity | | 50 | | μA |
| Sink Current | I_{EN_SK} | With negative logic EN polarity | | 50 | | μA |

^[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

^[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

^[c] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

^[d] Refer to Output Ripple plots.

^[e] Refer to load current vs. ambient temperature curves.

^[f] Refer to switching frequency vs. load current curves.

^[g] Minimum 5V between V_{IN} - V_{OUT} must be maintained or a minimum load of 1mA required.

PI3301-00-LGIZ (3.3V_{OUT}) Electrical Characteristics (Cont.)

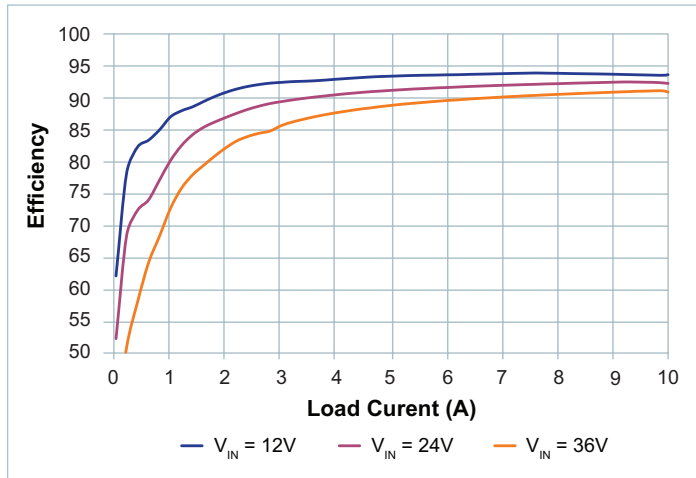


Figure 7 — Efficiency at 25°C

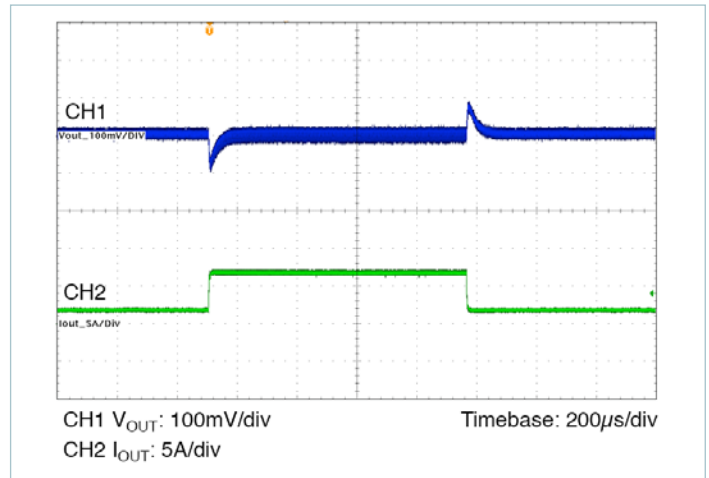


Figure 10 — Transient response 2A to 7A, at 5A/μs

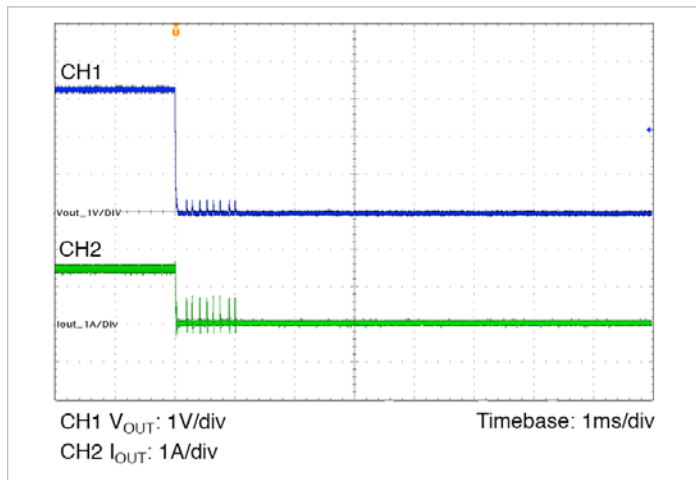


Figure 8 — Short circuit test

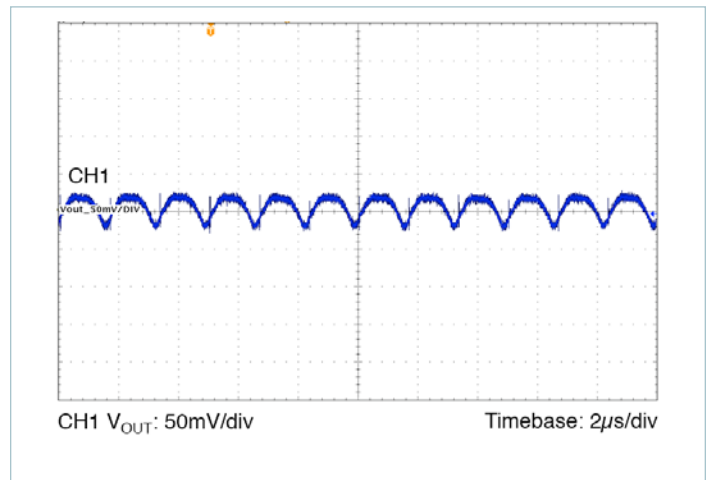


Figure 11 — Output ripple 24V_{IN}, 3.3V_{OUT} at 10A

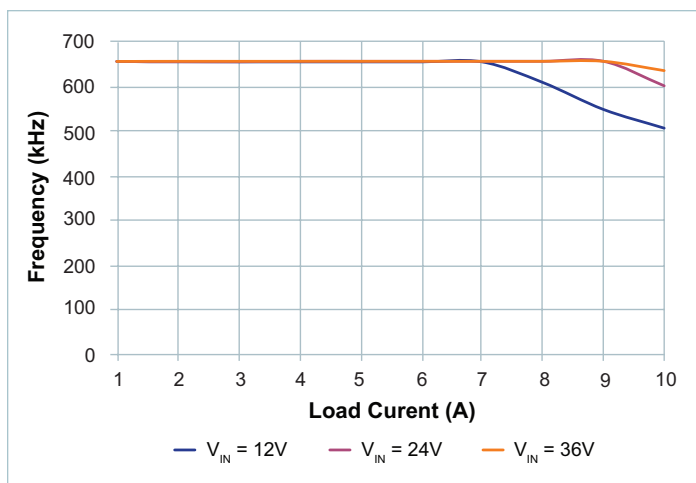


Figure 9 — Switching frequency vs. load current

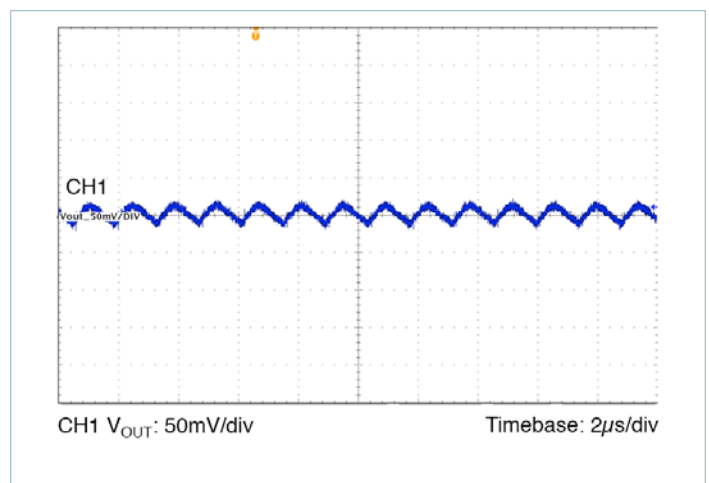


Figure 12 — Output ripple 24V_{IN}, 3.3V_{OUT} at 5A

PI3301-00-LGIZ (3.3V_{OUT}) Electrical Characteristics (Cont.)

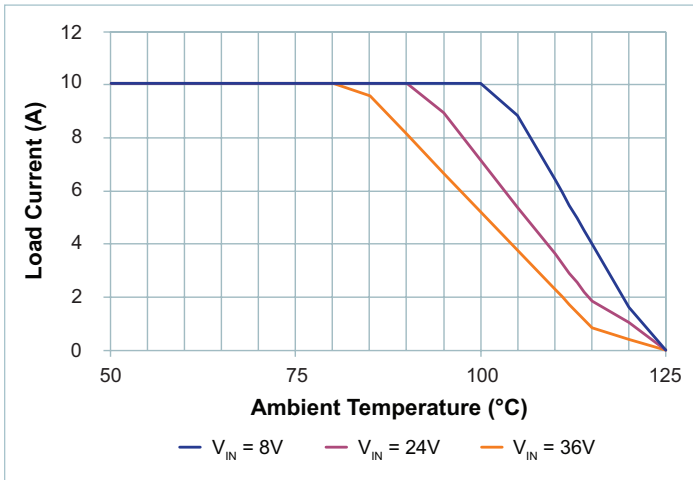


Figure 13 — Load current vs. ambient temperature, 0LFM

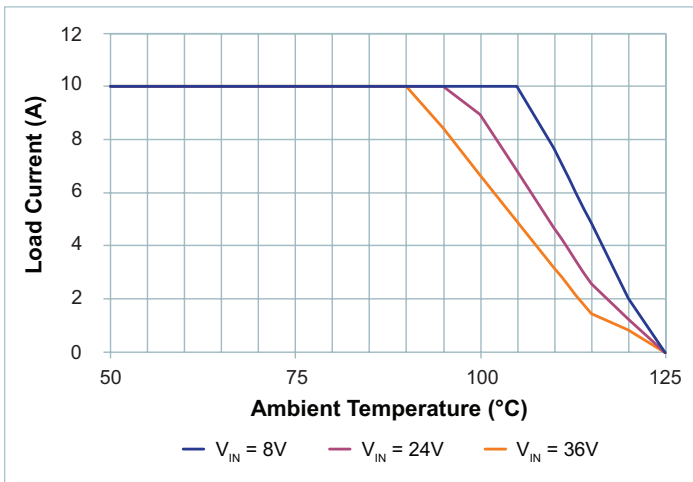


Figure 14 — Load current vs. ambient temperature, 200LFM

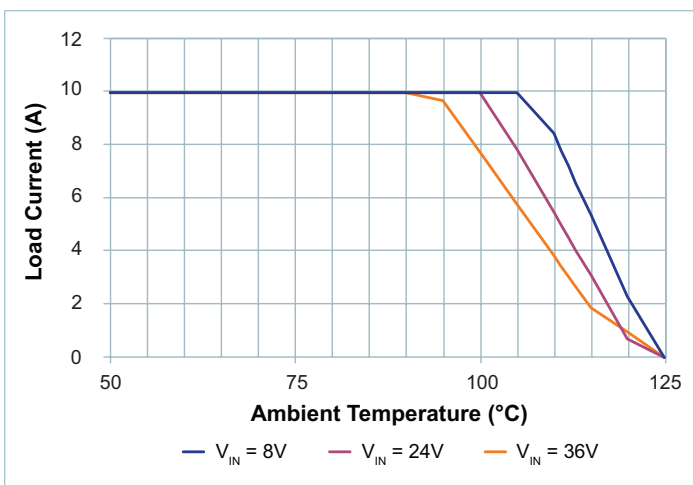


Figure 15 — Load current vs. ambient temperature, 400LFM

PI3302-00-LGIZ (5.0V_{OUT}) Electrical Characteristics

Unless otherwise specified: $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $V_{IN} = 24\text{V}$, $L1 = 200\text{nH}$ ^[a]

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|-----------------------------------|--|------|------|------|--------------------|
| Input Specifications | | | | | | |
| Input Voltage | V_{IN_DC} | [g] | 8 | 24 | 36 | V |
| Input Current | I_{IN_DC} | $V_{IN} = 24\text{V}$, $T_C = 25^{\circ}\text{C}$, $I_{OUT} = 10\text{A}$ | | 2.23 | | A |
| Input Current at Output Short (Fault Condition Duty Cycle) | I_{IN_Short} | [b] | | | 20 | mA |
| Input Quiescent Current | I_{Q_VIN} | Disabled | | 2.0 | | mA |
| | | Enabled (no load) | | 2.5 | | mA |
| Input Voltage Slew Rate | V_{IN_SR} | [b] | | | 1 | V/ μs |
| Output Specifications | | | | | | |
| Output Voltage Total Regulation | V_{OUT_DC} | [b] | 4.93 | 5.00 | 5.07 | V |
| Output Voltage Trim Range | V_{OUT_DC} | [c] [g] | 3.3 | | 6.5 | V |
| Line Regulation | $\Delta V_{OUT} (\Delta V_{IN})$ | At 25°C , $8\text{V} < V_{IN} < 36\text{V}$ | | 0.10 | | % |
| Load Regulation | $\Delta V_{OUT} (\Delta I_{OUT})$ | At 25°C , $0.5\text{A} < I_{OUT} < 10\text{A}$ | | 0.10 | | % |
| Output Voltage Ripple | V_{OUT_AC} | $I_{OUT} = 5\text{A}$, $C_{OUT} = 4 \times 47\mu\text{F}$, 20MHz BW ^[d] | | 30 | | mV _{P-P} |
| Continuous Output Current Range | I_{OUT_DC} | [e] [g] | | | 10 | A |
| Current Limit | I_{OUT_CL} | | | 12 | | A |
| Protection | | | | | | |
| V_{IN} UVLO Start Threshold | V_{UVLO_START} | | 7.10 | 7.60 | 8.00 | V |
| V_{IN} UVLO Stop Threshold | V_{UVLO_STOP} | | 6.80 | 7.25 | 7.60 | V |
| V_{IN} UVLO Hysteresis | V_{UVLO_HYS} | | | 0.33 | | V |
| V_{IN} OVLO Start Threshold | V_{OVLO_START} | | 36.1 | | | V |
| V_{IN} OVLO Stop Threshold | V_{OVLO_STOP} | | 37.0 | 38.4 | | V |
| V_{IN} OVLO Hysteresis | V_{OVLO_HYS} | | | 0.77 | | V |
| V_{IN} UVLO/OVLO Response Time | t_f | 1% overdrive | | 500 | | ns |
| Output Overvoltage Protection | V_{OVP} | Above V_{OUT} | | 20 | | % |
| Overtemperature Fault Threshold | T_{OTP} | | 130 | 135 | 140 | $^{\circ}\text{C}$ |
| Overtemperature Restart Hysteresis | T_{OTP_HYS} | | | 30 | | $^{\circ}\text{C}$ |

^[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

^[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

^[c] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

^[d] Refer to Output Ripple plots.

^[e] Refer to load current vs. ambient temperature curves.

^[f] Refer to switching frequency vs. load current curves.

^[g] Minimum 5V between V_{IN} - V_{OUT} must be maintained or a minimum load of 1mA required.

PI3302-00-LGIZ (5.0V_{OUT}) Electrical Characteristics (Cont.)

Unless otherwise specified: $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $V_{IN} = 24\text{V}$, $L1 = 200\text{nH}$ ^[a]

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|--------------------|--|-----|-----|------|---------------|
| Timing | | | | | | |
| Switching Frequency | f_S | ^[f] | | 1.0 | | MHz |
| Fault Restart Delay | t_{FR_DLY} | | | 30 | | ms |
| Sync In (SYNCI) | | | | | | |
| Synchronization Frequency Range | Δf_{SYNCI} | Relative to set switching frequency ^[c] | 50 | | 110 | % |
| SYNCI Threshold | V_{SYNCI} | | | 2.5 | | V |
| SYNCI Input Impedance | Z_{SYNCI} | | | 100 | | k Ω |
| Sync Out (SYNCO) | | | | | | |
| SYNCO High | V_{SYNCO_HI} | Source 1mA | 4.5 | | | V |
| SYNCO Low | V_{SYNCO_LO} | Sink 1mA | | | 0.5 | V |
| SYNCO Rise Time | t_{SYNCO_RT} | 20pF load | | 10 | | ns |
| SYNCO Fall Time | t_{SYNCO_FT} | 20pF load | | 10 | | ns |
| Soft Start And Tracking | | | | | | |
| TRK Active Input Range | V_{TRK} | | 0 | | 1.04 | V |
| TRK Max Output Voltage | | | | 1.2 | | V |
| TRK Disable Threshold | V_{TRK_OV} | | 20 | 40 | 62 | mV |
| Charge Current (Soft-Start) | I_{TRK} | | 70 | 50 | 25 | μA |
| Discharge Current (Fault) | I_{TRK_DIS} | $V_{TRK} = 0.5\text{V}$ | | 6.8 | | mA |
| Soft-Start Time | t_{SS} | $C_{TRK} = 0\mu\text{F}$ | | 2.2 | | ms |
| Enable | | | | | | |
| High Threshold | V_{EN_HI} | | 0.9 | 1 | 1.1 | V |
| Low Threshold | V_{EN_LO} | | 0.7 | 0.8 | 0.9 | V |
| Threshold Hysteresis | V_{EN_HYS} | | 100 | 200 | 300 | mV |
| Enable Pull-Up Voltage (Floating) | V_{EN_PU} | With positive logic EN polarity | | 2 | | V |
| Enable Pull-Down Voltage (Floating) | V_{EN_PD} | With negative logic EN polarity | | 0 | | V |
| Source Current | I_{EN_SO} | With positive logic EN polarity | | 50 | | μA |
| Sink Current | I_{EN_SK} | With negative logic EN polarity | | 50 | | μA |

^[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

^[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

^[c] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

^[d] Refer to Output Ripple plots.

^[e] Refer to load current vs. ambient temperature curves.

^[f] Refer to switching frequency vs. load current curves.

^[g] Minimum 5V between V_{IN} - V_{OUT} must be maintained or a minimum load of 1mA required.

PI3302-00-LGIZ (5.0V_{OUT}) Electrical Characteristics (Cont.)

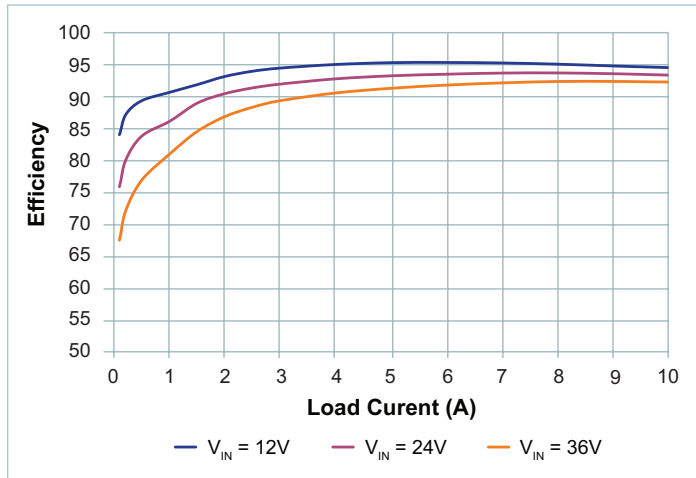


Figure 16 — Efficiency at 25°C

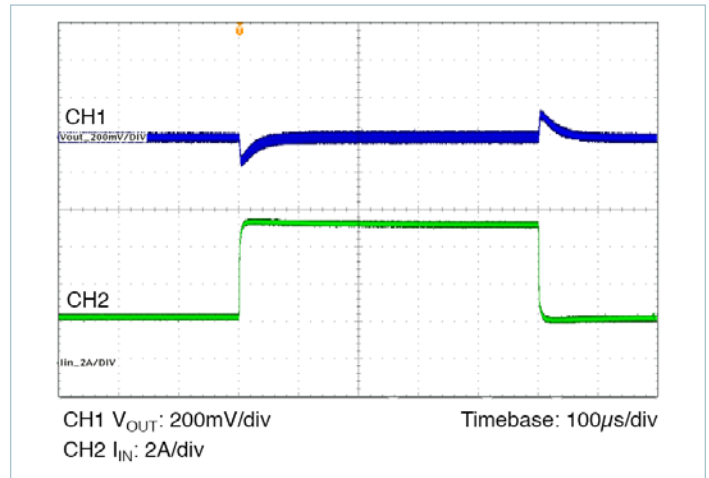


Figure 19 — Transient response 2A to 7A, at 5A/μs

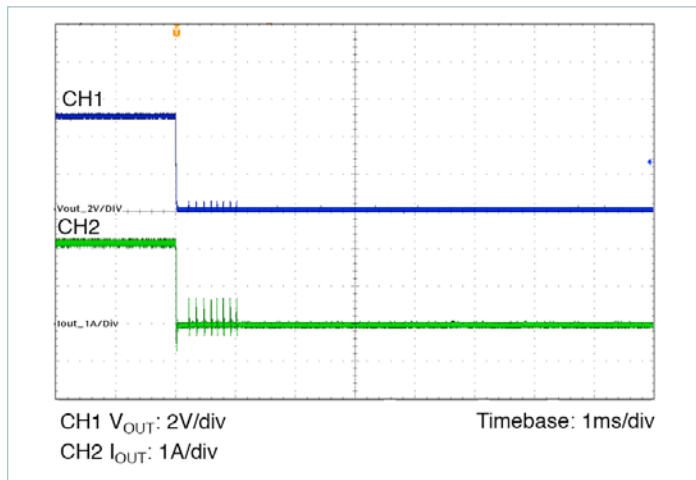


Figure 17 — Short circuit test

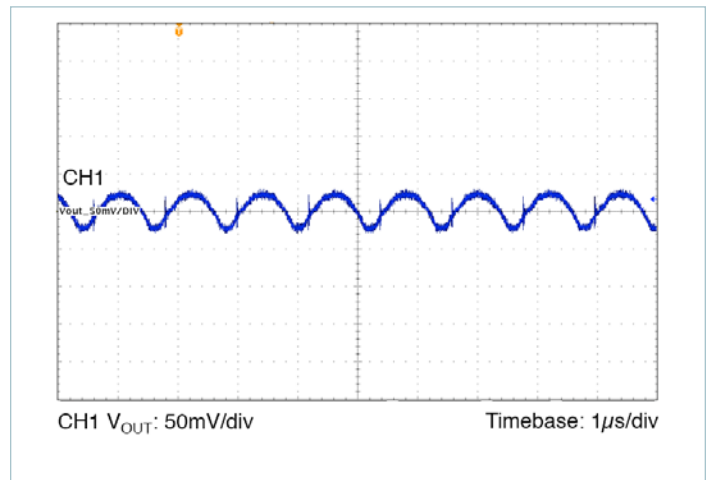


Figure 20 — Output ripple 24V_{IN}, 5.0V_{OUT} at 10A

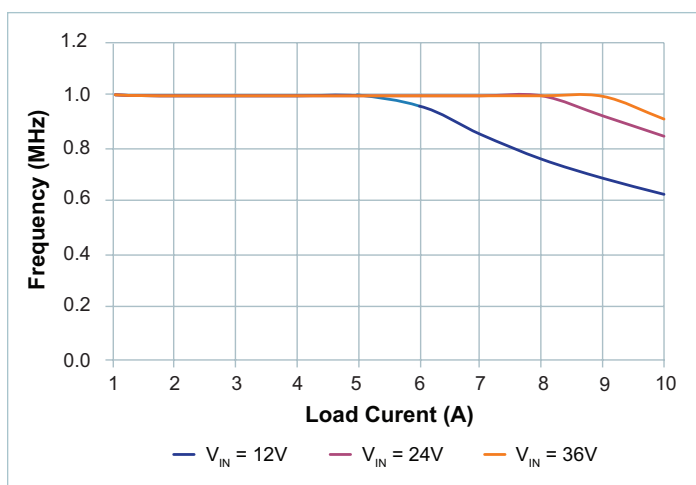


Figure 18 — Switching frequency vs. load current

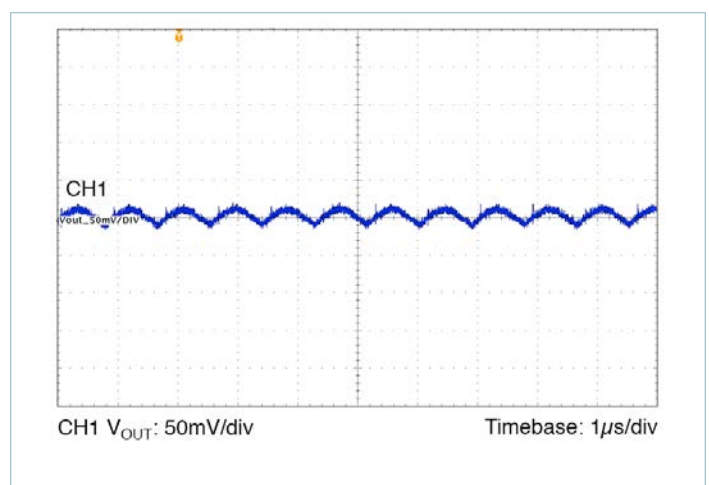


Figure 21 — Output ripple 24V_{IN}, 5.0V_{OUT} at 5A

PI3302-00-LGIZ (5.0V_{OUT}) Electrical Characteristics (Cont.)

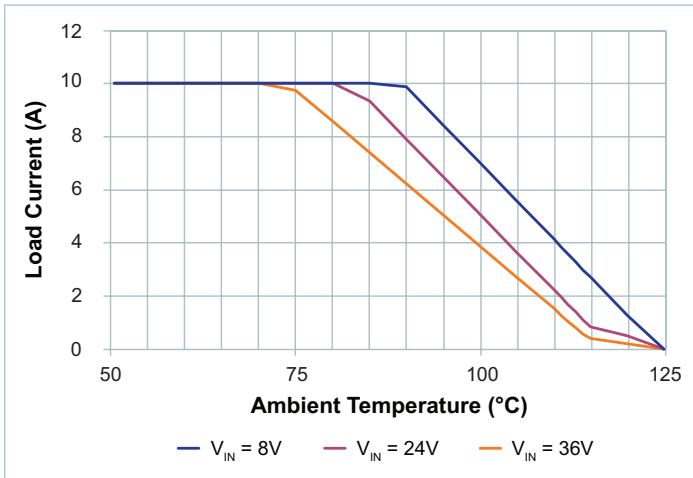


Figure 22 — Load current vs. ambient temperature, 0LFM

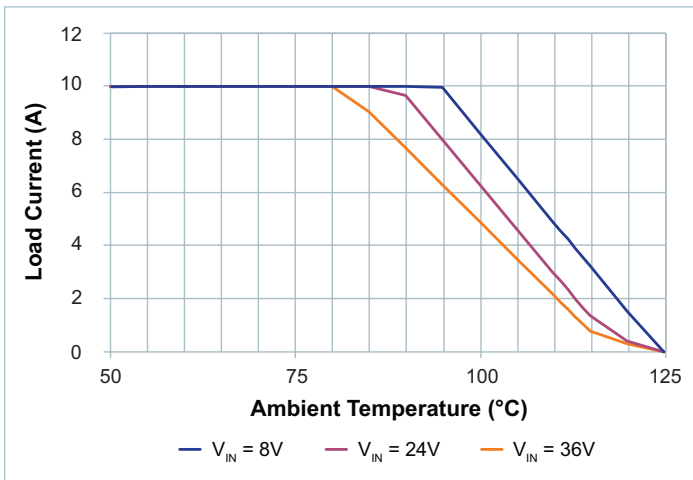


Figure 23 — Load current vs. ambient temperature, 200LFM

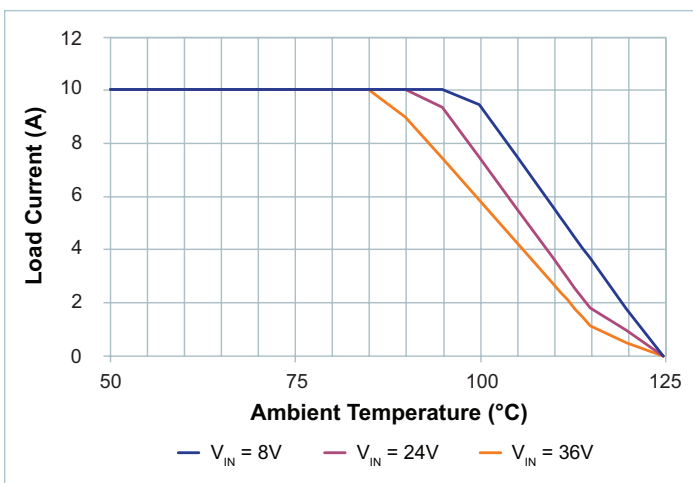


Figure 24 — Load current vs. ambient temperature, 400LFM

PI3303-00-LGIZ (12.0V_{OUT}) Electrical Characteristics

Unless otherwise specified: $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $V_{IN} = 24\text{V}$, $L1 = 230\text{nH}$ ^[a]

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|-----------------------------------|--|-------|-------|-------|--------------------|
| Input Specifications | | | | | | |
| Input Voltage | V_{IN_DC} | [g] | 17.4 | 24 | 36 | V |
| Input Current | I_{IN_DC} | $V_{IN} = 24\text{V}$, $T_C = 25^{\circ}\text{C}$, $I_{OUT} = 8\text{A}$ | | 4.15 | | A |
| Input Current at Output Short (Fault Condition Duty Cycle) | I_{IN_Short} | [b] | | | 20 | mA |
| Input Quiescent Current | I_{Q_VIN} | Disabled | | 2.0 | | mA |
| | | Enabled (no load) | | 2.5 | | mA |
| Input Voltage Slew Rate | V_{IN_SR} | [b] | | | 1 | V/ μs |
| Output Specifications | | | | | | |
| Output Voltage Total Regulation | V_{OUT_DC} | [b] | 11.82 | 12.0 | 12.18 | V |
| Output Voltage Trim Range | V_{OUT_DC} | [c] [g] | 6.5 | 12 | 13.0 | V |
| Line Regulation | $\Delta V_{OUT} (\Delta V_{IN})$ | At 25°C , $8\text{V} < V_{IN} < 36\text{V}$ | | 0.10 | | % |
| Load Regulation | $\Delta V_{OUT} (\Delta I_{OUT})$ | At 25°C , $0.5\text{A} < I_{OUT} < 8\text{A}$ | | 0.10 | | % |
| Output Voltage Ripple | V_{OUT_AC} | $I_{OUT} = 4\text{A}$, $C_{OUT} = 4 \times 22\mu\text{F}$, 20MHz BW ^[d] | | 60 | | mV _{P-P} |
| Continuous Output Current Range | I_{OUT_DC} | [e] | | | 8 | A |
| Current Limit | I_{OUT_CL} | | | 9 | | A |
| Protection | | | | | | |
| V_{IN} UVLO Start Threshold | V_{UVLO_START} | | 15.80 | 16.60 | 17.40 | V |
| V_{IN} UVLO Stop Threshold | V_{UVLO_STOP} | | 15.00 | 15.80 | 16.60 | V |
| V_{IN} UVLO Hysteresis | V_{UVLO_HYS} | | | 0.77 | | V |
| V_{IN} OVLO Start Threshold | V_{OVLO_START} | | 36.1 | | | V |
| V_{IN} OVLO Stop Threshold | V_{OVLO_STOP} | | 37.0 | 38.4 | | V |
| V_{IN} OVLO Hysteresis | V_{OVLO_HYS} | | | 0.77 | | V |
| V_{IN} UVLO/OVLO Response Time | t_f | 1% overdrive | | 500 | | ns |
| Output Overvoltage Protection | V_{OVP} | Above V_{OUT} | | 20 | | % |
| Overtemperature Fault Threshold | T_{OTP} | | 130 | 135 | 140 | $^{\circ}\text{C}$ |
| Overtemperature Restart Hysteresis | T_{OTP_HYS} | | | 30 | | $^{\circ}\text{C}$ |

^[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

^[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

^[c] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

^[d] Refer to Output Ripple plots.

^[e] Refer to load current vs. ambient temperature curves.

^[f] Refer to switching frequency vs. load current curves.

^[g] Minimum 5V between V_{IN} - V_{OUT} must be maintained or a minimum load of 1mA required.

PI3303-00-LGIZ (12.0V_{OUT}) Electrical Characteristics (Cont.)

Unless otherwise specified: $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $V_{IN} = 24\text{V}$, $L1 = 230\text{nH}$ ^[a]

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|--------------------|--|-----|-----|------|---------------|
| Timing | | | | | | |
| Switching Frequency | f_S | ^[f] | | 1.4 | | MHz |
| Fault Restart Delay | t_{FR_DLY} | | | 30 | | ms |
| Sync In (SYNCI) | | | | | | |
| Synchronization Frequency Range | Δf_{SYNCI} | Relative to set switching frequency ^[c] | 50 | | 110 | % |
| SYNCI Threshold | V_{SYNCI} | | | 2.5 | | V |
| SYNCI Input Impedance | Z_{SYNCI} | | | 100 | | k Ω |
| Sync Out (SYNCO) | | | | | | |
| SYNCO High | V_{SYNCO_HI} | Source 1mA | 4.5 | | | V |
| SYNCO Low | V_{SYNCO_LO} | Sink 1mA | | | 0.5 | V |
| SYNCO Rise Time | t_{SYNCO_RT} | 20pF load | | 10 | | ns |
| SYNCO Fall Time | t_{SYNCO_FT} | 20pF load | | 10 | | ns |
| Soft Start And Tracking | | | | | | |
| TRK Active Input Range | V_{TRK} | | 0 | | 1.04 | V |
| TRK Max Output Voltage | | | | 1.2 | | V |
| TRK Disable Threshold | V_{TRK_OV} | | 20 | 40 | 62 | mV |
| Charge Current (Soft-Start) | I_{TRK} | | 70 | 50 | 25 | μA |
| Discharge Current (Fault) | I_{TRK_DIS} | $V_{TRK} = 0.5\text{V}$ | | 6.8 | | mA |
| Soft-Start Time | t_{SS} | $C_{TRK} = 0\mu\text{F}$ | | 2.2 | | ms |
| Enable | | | | | | |
| High Threshold | V_{EN_HI} | | 0.9 | 1 | 1.1 | V |
| Low Threshold | V_{EN_LO} | | 0.7 | 0.8 | 0.9 | V |
| Threshold Hysteresis | V_{EN_HYS} | | 100 | 200 | 300 | mV |
| Enable Pull-Up Voltage (Floating) | V_{EN_PU} | With positive logic EN polarity | | 2 | | V |
| Enable Pull-Down Voltage (Floating) | V_{EN_PD} | With negative logic EN polarity | | 0 | | V |
| Source Current | I_{EN_SO} | With positive logic EN polarity | | 50 | | μA |
| Sink Current | I_{EN_SK} | With negative logic EN polarity | | 50 | | μA |

^[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

^[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

^[c] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

^[d] Refer to Output Ripple plots.

^[e] Refer to load current vs. ambient temperature curves.

^[f] Refer to switching frequency vs. load current curves.

^[g] Minimum 5V between V_{IN} - V_{OUT} must be maintained or a minimum load of 1mA required.

PI3303-00-LGIZ (12.0V_{OUT}) Electrical Characteristics (Cont.)

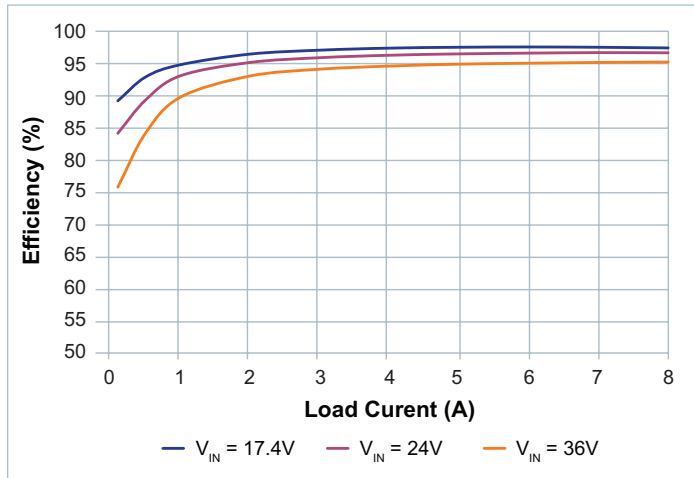


Figure 25 — Efficiency at 25°C

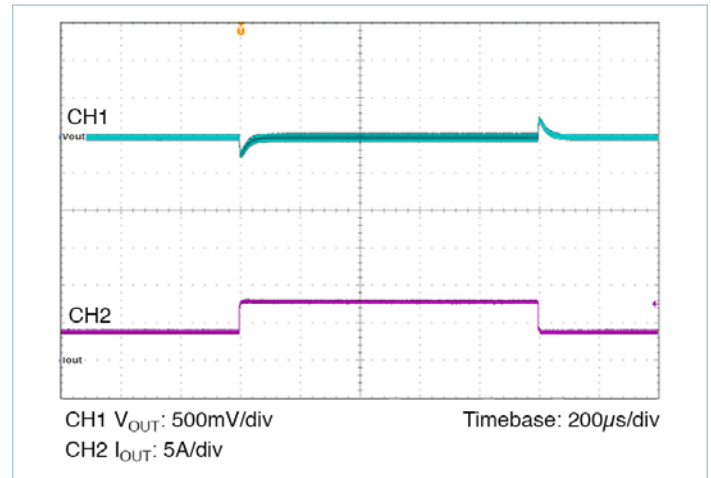


Figure 28 — Transient response 4A to 8A, at 5A/μs

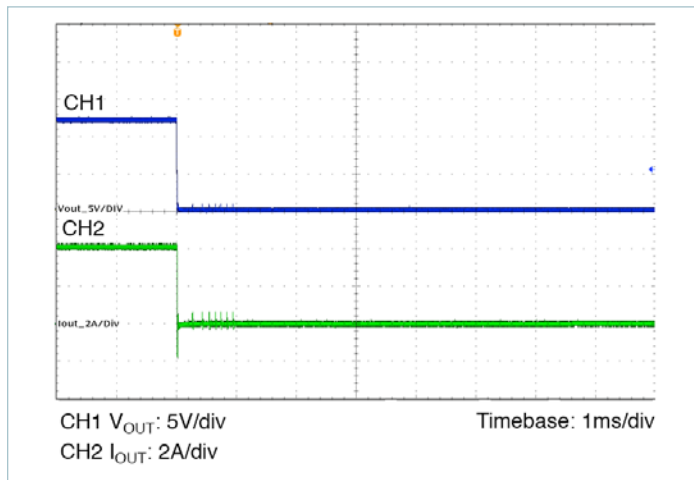


Figure 26 — Short circuit test

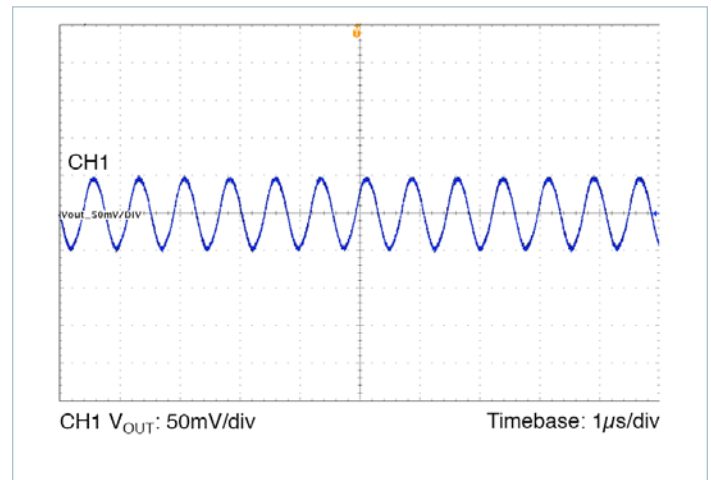


Figure 29 — Output ripple 24V_{IN}, 12.0V_{OUT} at 8A

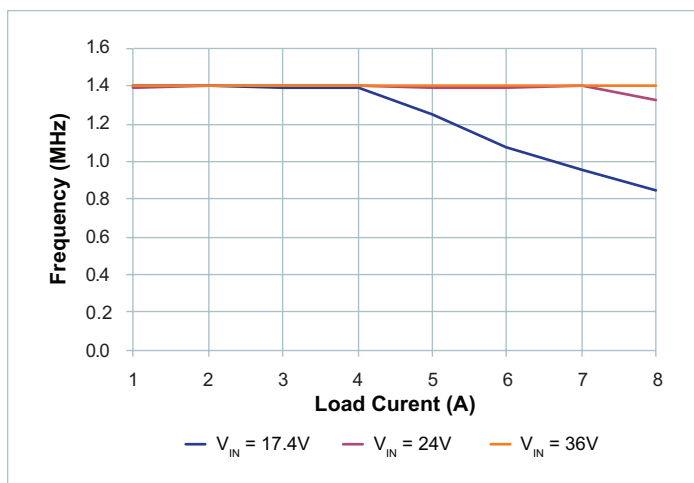


Figure 27 — Switching frequency vs. load current

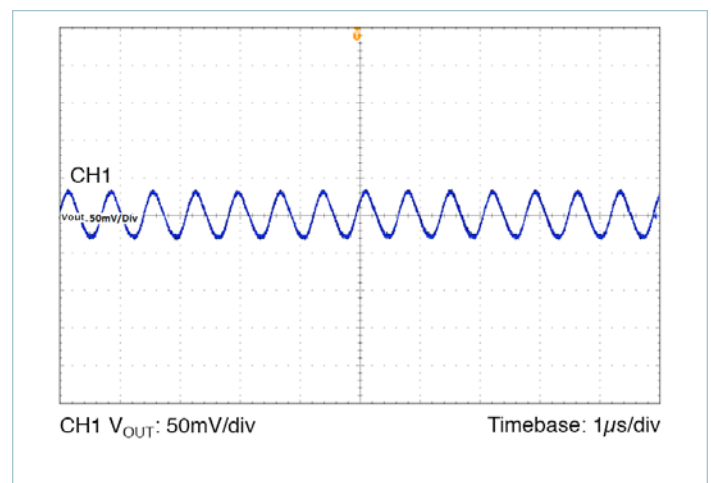


Figure 30 — Output ripple 24V_{IN}, 12.0V_{OUT} at 4A

PI3303-00-LGIZ (12.0V_{OUT}) Electrical Characteristics (Cont.)

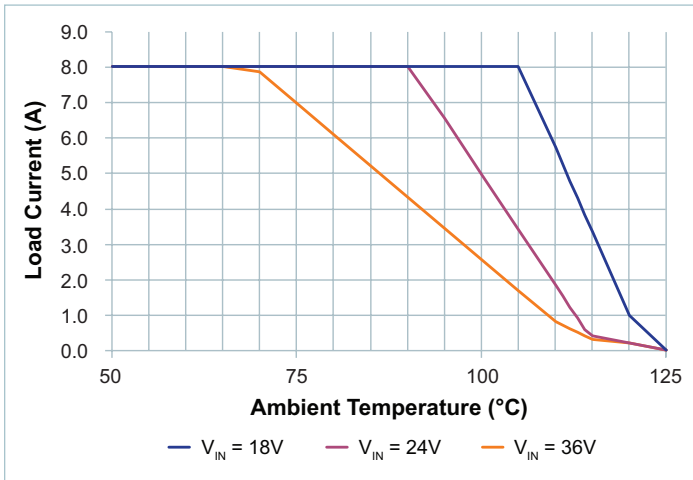


Figure 31 — Load current vs. ambient temperature, 0LFM

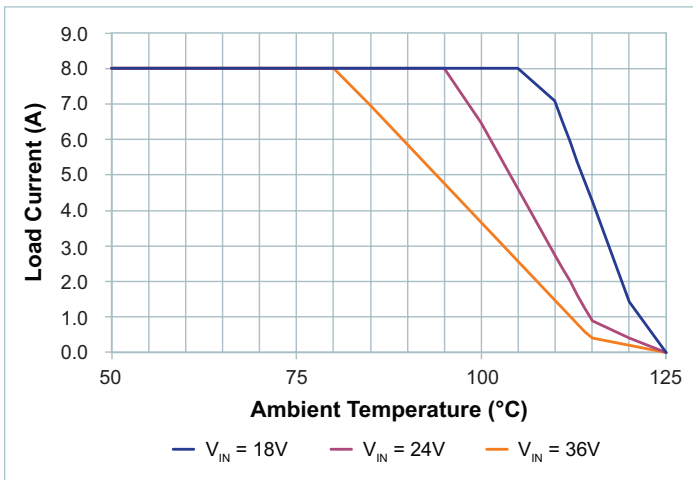


Figure 32 — Load current vs. ambient temperature, 200LFM

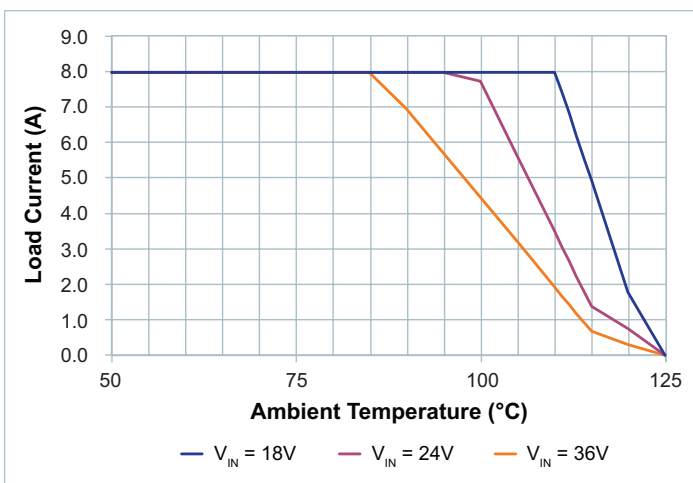


Figure 33 — Load current vs. ambient temperature, 400LFM

PI3305-00-LGIZ (15.0V_{OUT}) Electrical Characteristics

Unless otherwise specified: $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $V_{IN} = 24\text{V}$, $L1 = 230\text{nH}$ ^[a]

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|-----------------------------------|--|-------|------|-------|--------------------|
| Input Specifications | | | | | | |
| Input Voltage | V_{IN_DC} | [g] | 20.4 | 24 | 36 | V |
| Input Current | I_{IN_DC} | $V_{IN} = 24\text{V}$, $T_C = 25^{\circ}\text{C}$, $I_{OUT} = 8\text{A}$ | | 5.15 | | A |
| Input Current at Output Short (Fault Condition Duty Cycle) | I_{IN_Short} | [b] | | | 20 | mA |
| Input Quiescent Current | I_{Q_VIN} | Disabled | | 2.0 | | mA |
| | | Enabled (no load) | | 2.5 | | mA |
| Input Voltage Slew Rate | V_{IN_SR} | [b] | | | 1 | V/ μs |
| Output Specifications | | | | | | |
| Output Voltage Total Regulation | V_{OUT_DC} | [b] | 14.78 | 15.0 | 15.23 | V |
| Output Voltage Trim Range | V_{OUT_DC} | [c] [g] | 10.0 | 15 | 16 | V |
| Line Regulation | $\Delta V_{OUT} (\Delta V_{IN})$ | At 25°C , $8\text{V} < V_{IN} < 36\text{V}$ | | 0.1 | | % |
| Load Regulation | $\Delta V_{OUT} (\Delta I_{OUT})$ | At 25°C , $0.5\text{A} < I_{OUT} < 8\text{A}$ | | 0.1 | | % |
| Output Voltage Ripple | V_{OUT_AC} | $I_{OUT} = 4\text{A}$, $C_{OUT} = 4 \times 22\mu\text{F}$, 20MHz BW ^[d] | | 60 | | mV _{P-P} |
| Continuous Output Current Range | I_{OUT_DC} | [e] [g] | | | 8 | A |
| Current Limit | I_{OUT_CL} | | | 9 | | A |
| Protection | | | | | | |
| V_{IN} UVLO Start Threshold | V_{UVLO_START} | | 18.4 | 19.4 | 20.4 | V |
| V_{IN} UVLO Stop Threshold | V_{UVLO_STOP} | | 17.4 | 18.4 | 19.4 | V |
| V_{IN} UVLO Hysteresis | V_{UVLO_HYS} | | | 0.90 | | V |
| V_{IN} OVLO Start Threshold | V_{OVLO_START} | | 36.1 | | | V |
| V_{IN} OVLO Stop Threshold | V_{OVLO_STOP} | | 37.0 | 38.4 | | V |
| V_{IN} OVLO Hysteresis | V_{OVLO_HYS} | | | 0.77 | | V |
| V_{IN} UVLO/OVLO Response Time | t_f | 1% overdrive | | 500 | | ns |
| Output Overvoltage Protection | V_{OVP} | Above V_{OUT} | | 20 | | % |
| Overtemperature Fault Threshold | T_{OTP} | | 130 | 135 | 140 | $^{\circ}\text{C}$ |
| Overtemperature Restart Hysteresis | T_{OTP_HYS} | | | 30 | | $^{\circ}\text{C}$ |

^[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

^[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

^[c] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

^[d] Refer to Output Ripple plots.

^[e] Refer to load current vs. ambient temperature curves.

^[f] Refer to switching frequency vs. load current curves.

^[g] Minimum 5V between V_{IN} - V_{OUT} must be maintained or a minimum load of 1mA required.

PI3305-00-LGIZ (15.0V_{OUT}) Electrical Characteristics (Cont.)

Unless otherwise specified: $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $V_{IN} = 24\text{V}$, $L1 = 230\text{nH}$ ^[a]

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|--------------------|--|-----|-----|------|---------------|
| Timing | | | | | | |
| Switching Frequency | f_S | ^[f] | | 1.5 | | MHz |
| Fault Restart Delay | t_{FR_DLY} | | | 30 | | ms |
| Sync In (SYNCI) | | | | | | |
| Synchronization Frequency Range | Δf_{SYNCI} | Relative to set switching frequency ^[c] | 50 | | 110 | % |
| SYNCI Threshold | V_{SYNCI} | | | 2.5 | | V |
| SYNCI Input Impedance | Z_{SYNCI} | | | 100 | | k Ω |
| Sync Out (SYNCO) | | | | | | |
| SYNCO High | V_{SYNCO_HI} | Source 1mA | 4.5 | | | V |
| SYNCO Low | V_{SYNCO_LO} | Sink 1mA | | | 0.5 | V |
| SYNCO Rise Time | t_{SYNCO_RT} | 20pF load | | 10 | | ns |
| SYNCO Fall Time | t_{SYNCO_FT} | 20pF load | | 10 | | ns |
| Soft Start And Tracking | | | | | | |
| TRK Active Input Range | V_{TRK} | | 0 | | 1.04 | V |
| TRK Max Output Voltage | | | | 1.2 | | V |
| TRK Disable Threshold | V_{TRK_OV} | | 20 | 40 | 62 | mV |
| Charge Current (Soft-Start) | I_{TRK} | | 70 | 50 | 25 | μA |
| Discharge Current (Fault) | I_{TRK_DIS} | $V_{TRK} = 0.5\text{V}$ | | 6.8 | | mA |
| Soft-Start Time | t_{SS} | $C_{TRK} = 0\mu\text{F}$ | | 2.2 | | ms |
| Enable | | | | | | |
| High Threshold | V_{EN_HI} | | 0.9 | 1 | 1.1 | V |
| Low Threshold | V_{EN_LO} | | 0.7 | 0.8 | 0.9 | V |
| Threshold Hysteresis | V_{EN_HYS} | | 100 | 200 | 300 | mV |
| Enable Pull-Up Voltage (Floating) | V_{EN_PU} | With positive logic EN polarity | | 2 | | V |
| Enable Pull-Down Voltage (Floating) | V_{EN_PD} | With negative logic EN polarity | | 0 | | V |
| Source Current | I_{EN_SO} | With positive logic EN polarity | | 50 | | μA |
| Sink Current | I_{EN_SK} | With negative logic EN polarity | | 50 | | μA |

^[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

^[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

^[c] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

^[d] Refer to Output Ripple plots.

^[e] Refer to load current vs. ambient temperature curves.

^[f] Refer to switching frequency vs. load current curves.

^[g] Minimum 5V between V_{IN} - V_{OUT} must be maintained or a minimum load of 1mA required.

PI3305-00-LGIZ (15.0V_{OUT}) Electrical Characteristics (Cont.)

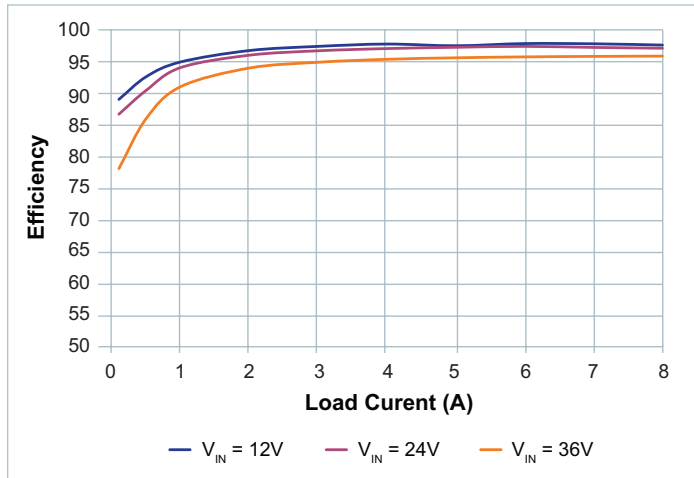


Figure 34 — Efficiency at 25°C

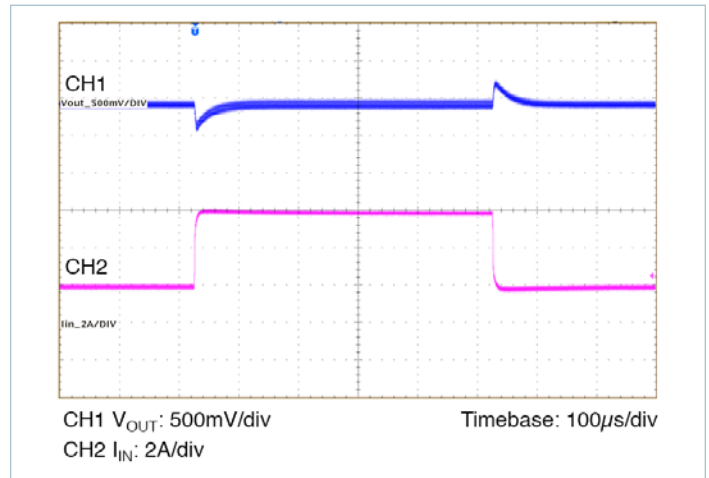


Figure 37 — Transient response 2A to 6A, at 5A/μs

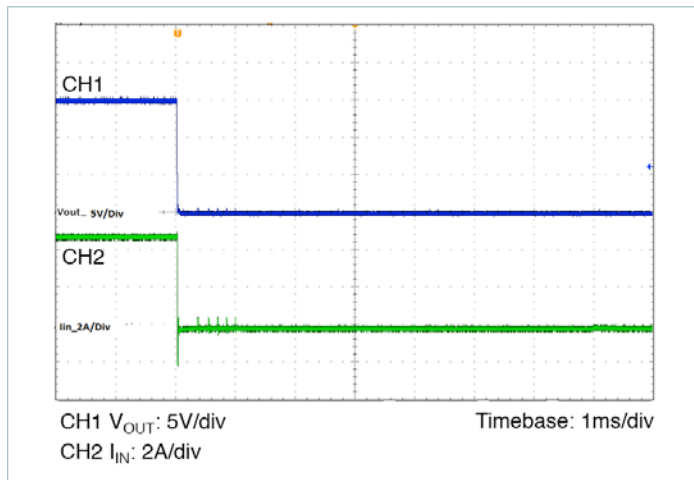


Figure 35 — Short circuit test

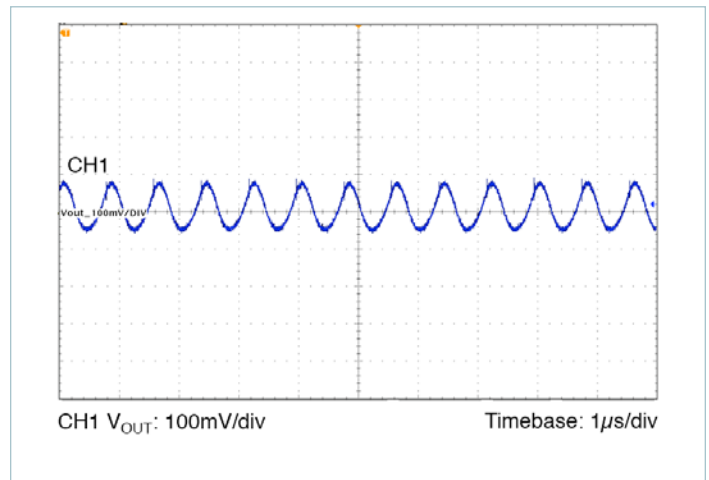


Figure 38 — Output ripple 24V_{IN}, 15.0V_{OUT} at 8A

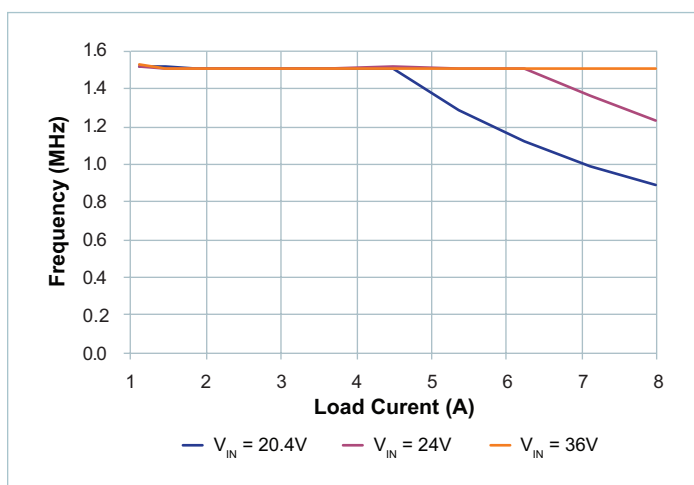


Figure 36 — Switching frequency vs. load current

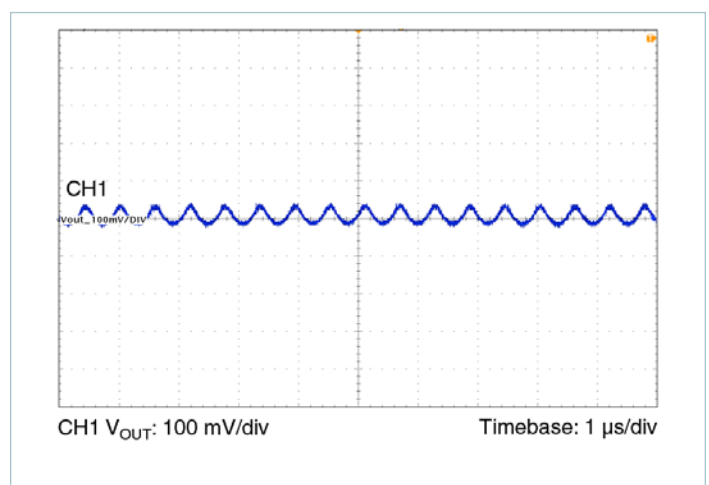


Figure 39 — Output ripple 24V_{IN}, 15.0V_{OUT} at 4A

PI3305-00-LGIZ (15.0V_{OUT}) Electrical Characteristics (Cont.)

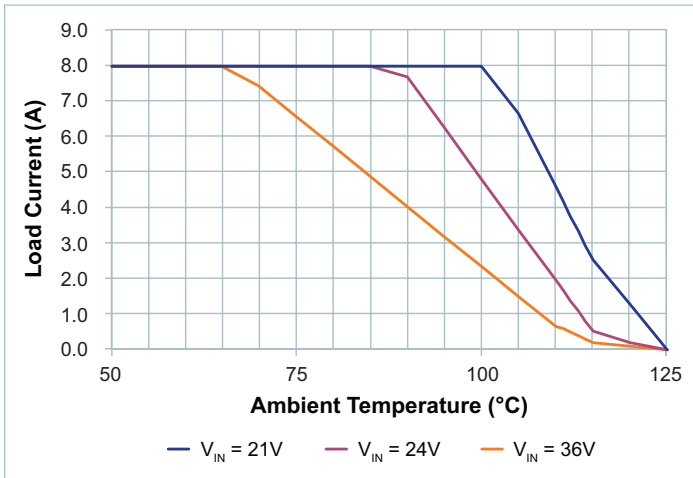


Figure 40 — Load current vs. ambient temperature, 0LFM

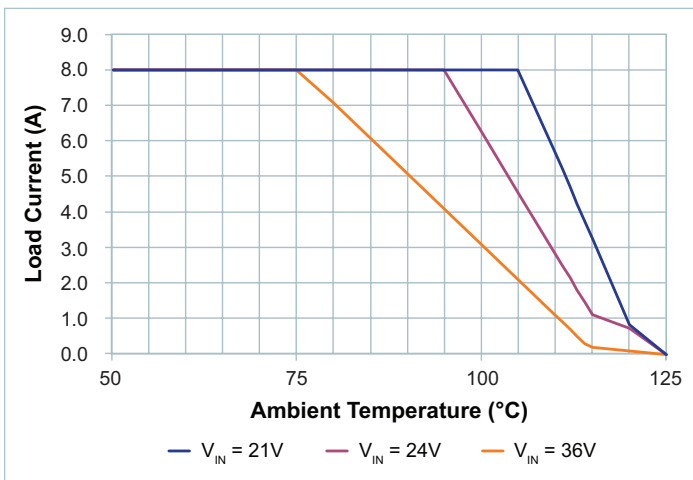


Figure 41 — Load current vs. ambient temperature, 200LFM

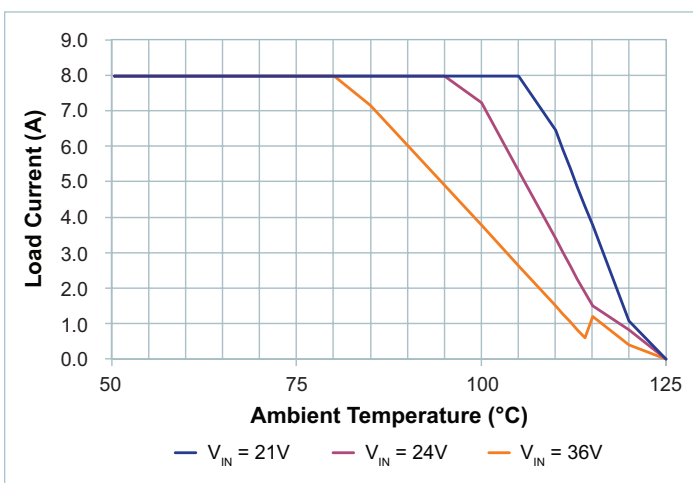


Figure 42 — Load current vs. ambient temperature, 400LFM

Functional Description

The PI33xx is a family of highly integrated ZVS Buck regulators. The PI33xx has a set output voltage that is trimmable within a prescribed range shown in Table 1. Performance and maximum output current are characterized with a specific external power inductor (see Table 4).

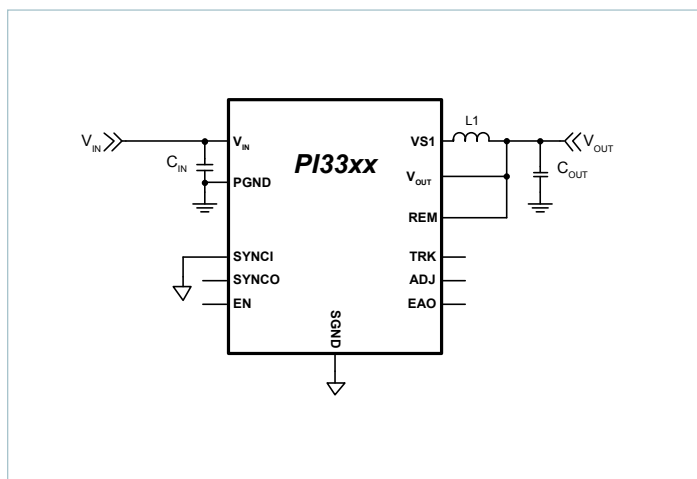


Figure 43 — ZVS Buck with required components

For basic operation, Figure 43 shows the connections and components required. No additional design or settings are required.

ENABLE (EN)

EN is the enable pin of the converter. The EN Pin is referenced to SGND and permits the user to turn the regulator on or off. The EN default polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the converter output is enabled. Pulling EN pin below $0.8V_{DC}$ with respect to SGND will disable the regulator output.

The EN input polarity can be programmed via the I²C™ data bus. When the EN pin polarity is programmed for negative logic assertion; and if the EN pin is left floating, the regulator output is enabled. Pulling the EN pin above $1.0V_{DC}$ with respect to SGND, will disable the regulator output.

Remote Sensing

An internal 100Ω resistor is connected between REM pin and V_{OUT} pin to provide regulation when the REM connection is broken. Referring to Figure 43, it is important to note that L1 and C_{OUT} are the output filter and the local sense point for the power supply output. As such, the REM pin should be connected at C_{OUT} as the default local-sense connection unless remote sensing to compensate additional distribution losses in the system. The REM pin should not be left floating.

Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency by an external clock referenced to SGND. The external clock can synchronize the unit between 50% and 110% of the preset switching frequency (f_s). The phase delay can be programmed via I²C bus with respect to the clock applied at SYNCI pin. Phase delay allows PI33xx regulators to be paralleled and operate in an interleaving mode.

The PI33xx default for SYNCI is to sync with respect to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the paralleling of two PI33xx devices without the need for further user programming or external sync clock circuitry. The user can change the SYNCI polarity to sync with the external clock rising edge via the I²C data bus.

When using the internal oscillator, the SYNCO pin provides a 5V clock that can be used to sync other regulators. Therefore, one PI33xx can act as the lead regulator and have additional PI33xxs running in parallel and interleaved.

Soft Start

The PI33xx includes an internal soft-start capacitor to ramp the output voltage in 2ms from 0V to full output voltage. Connecting an external capacitor from the TRK pin to SGND will increase the start-up ramp period. See, “Soft Start Adjustment and Track,” in the Applications Description section for more details.

Output Voltage Trim

The PI33xx output voltage can be trimmed up from the preset output by connecting a resistor from ADJ pin to SGND and can be trimmed down by connecting a resistor from ADJ pin to V_{OUT}. The Table 1 defines the voltage ranges for the PI33xx family.

| Device | Output Voltage | |
|----------------|----------------|--------------|
| | Set | Range |
| PI3301-01-LGIZ | 3.3V | 2.3 – 4.1V |
| PI3301-00-LGIZ | 3.3V | 2.3 – 4.1V |
| PI3302-00-LGIZ | 5.0V | 3.3 – 6.5V |
| PI3303-00-LGIZ | 12V | 6.5 – 13.0V |
| PI3305-00-LGIZ | 15V | 10.0 – 16.0V |

Table 1 — PI33xx family output voltage range

Output Current Limit Protection

PI33xx has two methods implemented to protect from output short or over current condition.

Slow Current Limit protection: prevents the output load from sourcing current higher than the regulator's maximum rated current. If the output current exceeds the Current Limit (I_{OUT_CL}) for $1024\mu s$, a slow current limit fault is initiated and the regulator is shut down which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Fast Current Limit protection: PI33xx monitors the regulator inductor current pulse-by-pulse to prevent the output from supplying very high current due to sudden low-impedance short (50A typical). If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching until Fault Restart Delay ends and then initiate a soft-start cycle.

Both the Fast and Slow current limit faults are stored in a Fault Register and can be read and cleared via I²C™ data bus.

Input Undervoltage Lockout

If V_{IN} falls below the input Undervoltage Lockout (UVLO) threshold, but remains high enough to power the internal bias supply, the PI33xx will complete the current cycle, stop switching, enter a low-power state and initiate a fault. The system will restart once the input voltage is reestablished and after the Fault Restart Delay. A UVLO fault is stored in a Fault Register and can be read and cleared via I²C data bus.

Input Overvoltage Lockout

If V_{IN} exceeds the input Overvoltage Lockout (OVLO) threshold (V_{OVLO}), while the controller is running, the PI33xx will complete the current cycle, stop switching, enter a low-power state and set an OVLO fault. The system will resume operation when the input voltage falls below 98% of the OVLO threshold and after the Fault Restart Delay. The OVLO fault is stored in a Fault Register and can be read and cleared via I²C data bus.

Output Overvoltage Protection

The PI33xx family is equipped with output Overvoltage Protection (OVP) to prevent damage to input voltage-sensitive devices. If the output voltage exceeds 20% of its set regulated value, the regulator will complete the current cycle, stop switching and issue an OVP fault. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay. The OVP fault is stored in a Fault Register and can be read and cleared via I²C data bus.

Overtemperature Protection

The internal package temperature is monitored to prevent internal components from reaching their thermal maximum. If the Overtemperature Protection Threshold (OTP) is exceeded (T_{OTP}), the regulator will complete the current switching cycle, enter a low-power mode, set a fault flag, and will soft-start when the internal temperature falls below Overtemperature Restart Hysteresis (T_{OTP_HYS}). The OTP fault is stored in a Fault Register and can be read and cleared via I²C data bus.

Pulse Skip Mode (PSM)

PI33xx features a PSM to achieve high efficiency at light loads. The regulators are set up to skip pulses if EAO falls below a PSM threshold. Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Skip Mode threshold.

Variable Frequency Operation

Each PI33xx is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 4), to operate at peak efficiency across line and load variations. At low-line and high-load applications, the base frequency will decrease to accommodate these extreme operating ranges. By stretching the frequency, the ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

Parallel Operation

Paralleling modules can be used to increase the output current capability of a single power rail and reduce output voltage ripple.

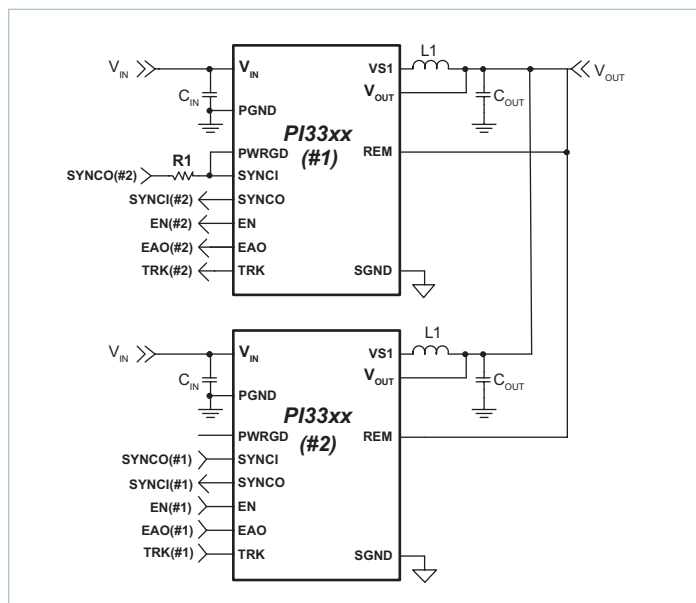


Figure 44 — PI33xx parallel operation

The PI33xx default for SYNCI is to sync with respect to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the paralleling of two PI33xx devices without the need for further user programming or external sync clock circuitry. The user can change the SYNCI polarity to sync with the external clock rising edge via the I²C™ data bus.

By connecting the EAO pins and SGND pins of each module together the units will share the current equally. When the TRK pins of each unit are connected together, the units will track each other during soft-start and all unit EN pins have to be released to allow the units to start (See Figure 44). Also, any fault event in any regulator will disable the other regulators. The two regulators will be out of phase with each other reducing output ripple (refer to Switching Frequency Synchronization).

To provide synchronization between regulators over the entire operational frequency range, the Power Good (PWRGD) pin must be connected to the lead regulator's (#1) SYNCI pin and a 2.5kΩ Resistor, R1, must be placed between SYNCO (#2) return and the lead regulator's SYNCI (#1) pin, as shown in Figure 44. In this configuration, at system soft start, the PWRGD pin pulls SYNCI low forcing the lead regulator to initialize the open-loop start-up synchronization. Once the regulators reach regulation, SYNCI is released and the system is now synchronized in a closed-loop configuration which allows the system to adjust, on the fly, when any of the individual regulators begin to enter variable frequency mode in the loop.

Multi-phasing three regulators is possible with no change to the basic single-phase design. For more information about how to program phase delays within the regulator, please refer to user guide [PI33xx Multi-Phase Design Guide](#).

I²C™ Interface Operation

PI33xx devices provide an I²C digital interface that enables the user to program the EN pin polarity (from high to low assertion) and switching frequency synchronization phase/delay. These are one time programmable options to the device.

Also, the PI33xx devices allow for dynamic V_{OUT} margining via I²C that is useful during development (settings stored in volatile memory only and not retained by the device). The PI33xx also have the option for fault telemetry including:

- Fast/Slow current limit
- Output voltage high
- Input overvoltage
- Input undervoltage
- Overtemperature protection

For more information about how to utilize the I²C interface please refer to Picor user guide [PI33xx I²C Digital Interface Guide](#).

Application Description

Output Voltage Trim

The PI33xx family of Buck Regulators provides seven common output voltages: 3.3, 5.0, 12 and 15V. A post-package trim step is implemented to offset any resistor divider network errors ensuring maximum output accuracy. With a single resistor connected from the ADJ pin to SGND or REM, each device's output can be varied above or below the nominal set voltage.

| Device | Output Voltage | |
|-----------|----------------|--------------|
| | Set | Range |
| PI3301-01 | 3.3V | 2.3 – 4.1V |
| PI3301-00 | 3.3V | 2.3 – 4.1V |
| PI3302-00 | 5.0V | 3.3 – 6.5V |
| PI3303-00 | 12V | 6.5 – 13.0V |
| PI3305-00 | 15V | 10.0 – 16.0V |

Table 2 — PI33xx family output voltage range

The remote pin (REM) should always be connected to the V_{OUT} pin, if not used, to prevent an output voltage offset. Figure 45 shows the internal feedback voltage divider network.

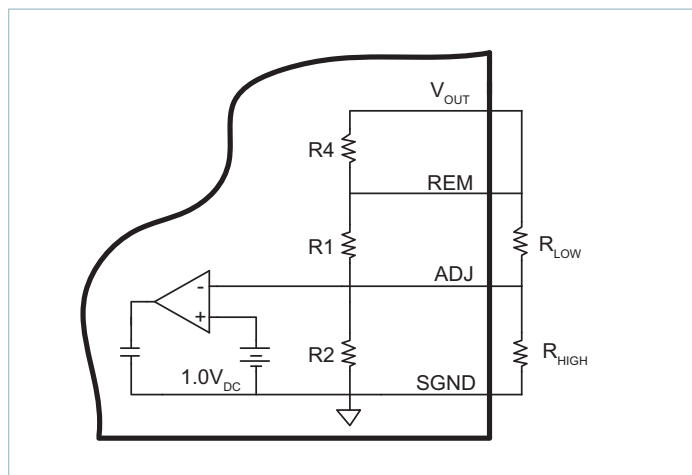


Figure 45 — Internal resistor divider network

R1, R2, and R4 are all internal 1.0% resistors and R_{LOW} and R_{HIGH} are external resistors for which the designer can add to modify V_{OUT} to a desired output. The internal resistor value for each regulator is listed below in Table 3.

| Device | R1 | R2 | R4 |
|----------------|--------|--------|------|
| PI3301-01-LGIZ | 2.61kΩ | 1.13kΩ | 100Ω |
| PI3301-00-LGIZ | 2.61kΩ | 1.13kΩ | 100Ω |
| PI3302-00-LGIZ | 4.53kΩ | 1.13kΩ | 100Ω |
| PI3303-00-LGIZ | 11.0kΩ | 1.0kΩ | 100Ω |
| PI3305-00-LGIZ | 14.0kΩ | 1.0kΩ | 100Ω |

Table 3 — PI33xx internal divider values

By choosing an output voltage value within the ranges stated in Table 2, V_{OUT} can simply be adjusted up or down by selecting the proper R_{HIGH} or R_{LOW} value, respectively. The following equations can be used to calculate R_{HIGH} and R_{LOW} values:

$$R_{HIGH} = \frac{1}{\left(\frac{V_{OUT} - 1}{R1}\right) - \left(\frac{1}{R2}\right)} \quad (1)$$

$$R_{LOW} = \frac{1}{\frac{1}{R2(V_{OUT} - 1)} - \left(\frac{1}{R1}\right)} \quad (2)$$

If, for example, a 4.0V output is needed, the user should choose the regulator with a trim range covering 4.0V from Table 2. For this example, the PI3301 is selected (3.3V set voltage). First step would be to use Equation 1 to calculate R_{HIGH} since the required output voltage is higher than the regulator set voltage. The resistor divider network values for the PI3301 are can be found in Table 3 and are $R1 = 2.61k\Omega$ and $R2 = 1.13k\Omega$. Inserting these values in to Equation 1, R_{HIGH} is calculated as follows:

$$3.78k\Omega = \frac{1}{\left(\frac{4.0 - 1}{2.61k\Omega}\right) - \left(\frac{1}{1.13k\Omega}\right)} \quad (3)$$

Resistor R_{HIGH} should be connected as shown in Figure 45 to achieve the desired 4.0V regulator output. No external R_{LOW} resistor is need in this design example since the trim is above the regulator set voltage.

Soft-Start Adjust and Tracking

The TRK pin offers a means to increase the regulator’s soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal 100nF and a fixed charge current to provide a minimum start-up time of 2ms (typical) for all PI33xx regulators. By adding an additional external capacitor to the TRK

pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

$$C_{TRK} = (t_{TRK} \cdot I_{TRK}) - 100 \cdot 10^{-9} \quad (4)$$

Where t_{TRK} is the soft-start time and I_{TRK} is a 50μA internal charge current (see Electrical Characteristics for limits).

There is typically either proportional or direct tracking implemented within a design. For proportional tracking between several regulators at start up, simply connect all devices TRK pins together. This type of tracking will force all connected regulators to start up and reach regulation at the same time (see Figure 46(a)).

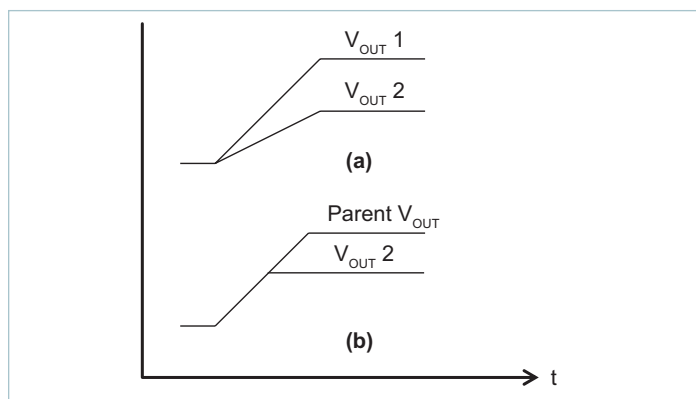


Figure 46 — PI33xx tracking methods

For Direct Tracking, choose the regulator with the highest output voltage as the parent and connect the parent to the TRK pin of the other regulators through a divider (Figure 47) with the same ratio as the child’s feedback divider (see Table 3 for values).

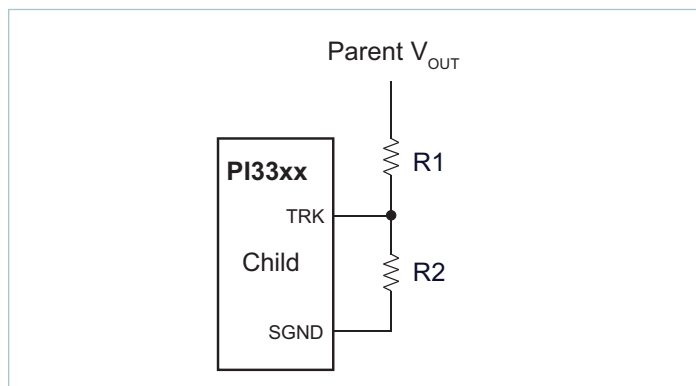


Figure 47 — Voltage divider connections for direct tracking

All connected regulators’ soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 46(b). All tracking regulators should have their Enable (EN) pins connected together to work properly.

Inductor Pairing

The PI33xx utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. Table 4 details the specific inductor value and part number utilized for each PI33xx device which are available from Eaton and Pulse. Data sheets are available at:

<https://www.eaton.com/>

<https://www.power.pulseelectronics.com/>

| Device | Inductor [nH] | Inductor Part Number | Manufacturer |
|-----------|---------------|----------------------|--------------|
| PI3301-01 | 150 | FPV1006-150-R | Eaton |
| PI3301-00 | 200 | FPT705-200-R | Eaton |
| | | PA5121.201HLT | Pulse |
| PI3302-00 | 200 | FPT705-200-R | Eaton |
| | | PA5121.201HLT | Pulse |
| PI3303-00 | 230 | FPT705-230-R | Eaton |
| PI3305-00 | 230 | FPT705-230-R | Eaton |

Table 4 — PI33xx inductor pairing

Thermal De-Rating

Thermal de-rating curves are provided that are based on component temperature changes versus load current, input voltage and air flow. It is recommended to use these curves as a guideline for proper thermal de-rating. These curves represent the entire

system and are inclusive to both the PI33xx regulator and the external inductor. Maximum thermal operation is limited by either the MOSFETs or inductor depending upon line and load conditions. Thermal measurements were made using a standard PI33xx evaluation board which is 3 x 4 inches in area and uses 4-layer, 2oz copper. Thermal measurements were made on the three main power devices, the two internal MOSFETs and the external inductor, with air flows of 0, 200 and 400LFM.

Filter Considerations

The PI33xx requires input bulk storage capacitance as well as low-impedance ceramic X5R input capacitors to ensure proper start up and high-frequency decoupling for the power stage. The PI33xx will draw nearly all of the high-frequency current from the low-impedance ceramic capacitors when the main high-side MOSFET is conducting. During the time the high-side MOSFET is off, they are replenished from the bulk capacitor. If the input impedance is high at the switching frequency of the converter, the bulk capacitor must supply all of the average current into the converter, including replenishing the ceramic capacitors. This value has been chosen to be 100 μ F so that the PI33xx can start up into a full resistive load and supply the output capacitive load with the default minimum soft start capacitor when the input source impedance is 50 Ω at 1MHz. The ESR for this capacitor should be approximately 20m Ω . The RMS ripple current in this capacitor is small, so it should not be a concern if the input recommended ceramic capacitors are used. Table 5 shows the recommended input and output capacitors to be used for the various models as well as expected transient response, RMS ripple currents per capacitor, and input and output ripple voltages. Table 6 includes the recommended input and output ceramic capacitors.

| Device | V _{IN} (V) | I _{LOAD} (A) | C _{INPUT} Ceramic X5R | C _{INPUT} Bulk Elec. | C _{OUTPUT} Ceramic X5R | C _{INPUT} Ripple Current (I _{RMS}) | C _{OUTPUT} Ripple Current (I _{RMS}) | Input Ripple (mV _{p-p}) | Output Ripple (mV _{p-p}) | Output Ripple (mV _{p-p}) | Recovery Time (μ s) | Load Step (A) (Slew/ μ s) |
|-----------|---------------------|-----------------------|--------------------------------|-------------------------------|---|---|--|-----------------------------------|------------------------------------|------------------------------------|--------------------------|-------------------------------|
| PI3301-01 | 24 | 10 | 4 x 4.7 μ F | 100 μ F 50V | 4 X 100 μ F 2 X 1 μ F 1 X 0.1 μ F | 1.05 | 1.625 | 200 | 40 | \pm 100 | 20 | 5 (10A/ μ s) |
| | | 125 | | | | | | 33 | | | | |
| PI3301-00 | 24 | 10 | 4 x 4.7 μ F | 100 μ F 50V | 4 X 100 μ F 2 X 1 μ F 1 X 0.1 μ F | 1.05 | 1.625 | 200 | 40 | \pm 100 | 20 | 5 (10A/ μ s) |
| | | 125 | | | | | | 33 | | | | |
| PI3302 | 24 | 10 | 4 x 4.7 μ F | 100 μ F 50V | 4 X 47 μ F 2 X 1 μ F 1 X 0.1 μ F | 1.2 | 1.5 | 220 | 50 | \pm 170 | 30 | 5 (5A/ μ s) |
| | | 140 | | | | | | 30 | | | | |
| PI3303 | 24 | 8 | 4 x 4.7 μ F | 100 μ F 50V | 4 X 22 μ F 2 X 1 μ F 1 X 0.1 μ F | 1.3 | 1.36 | 275 | 100 | \pm 300 | 30 | 4 (10A/ μ s) |
| | | 150 | | | | | | 60 | | | | |
| PI3305 | 24 | 8 | 4 x 4.7 μ F | 100 μ F 50V | 4 X 22 μ F 2 X 1 μ F 1 X 0.1 μ F | 1.38 | 1.2 | 280 | 150 | \pm 400 | 30 | 4 (10A/ μ s) |
| | | 160 | | | | | | 75 | | | | |

Table 5 — Recommended input and output capacitance

| Murata Part Number | Description |
|--------------------|---------------------------|
| GRM188R71C105KA12D | 1 μ F 16V 0603 X7R |
| GRM319R71H104KA01D | 0.1 μ F 50V 1206 X7R |
| GRM31CR60J107ME39L | 100 μ F 6.3V 1206 X5R |
| GRM31CR71H475KA12K | 4.7 μ F 50V 1206 X7R |
| GRM31CR61A476ME15L | 47 μ F 10V 1206 X5R |
| GRM31CR61E226KE15L | 22 μ F 25V 1206 X5R |

Table 6 — Capacitor manufacturer part numbers

Layout Guidelines

To optimize maximum efficiency and low-noise performance from a PI33xx design, layout considerations are necessary. Reducing trace resistance and minimizing high current loop returns along with proper component placement will contribute to optimized performance.

A typical buck converter circuit is shown in Figure 48. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

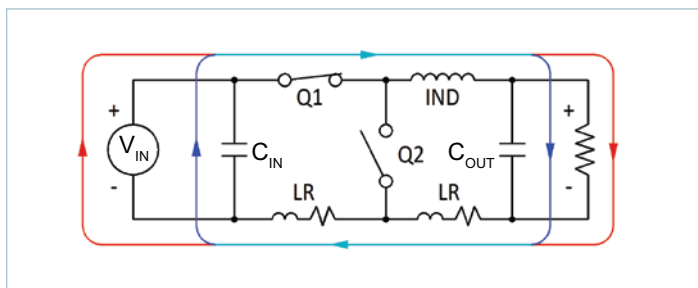


Figure 48 — Typical Buck Converter

The path between the C_{OUT} and C_{IN} capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on.

Figure 49, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI33xx performance.

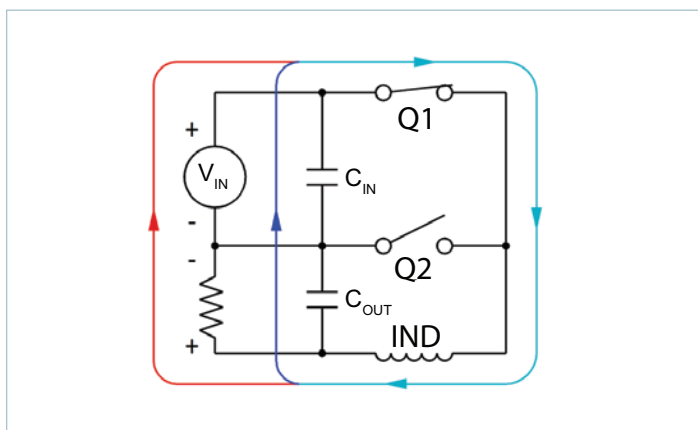


Figure 49 — Current flow: Q1 closed

When Q1 is on and Q2 is off, the majority of C_{IN} 's current is used to satisfy the output load and to recharge the C_{OUT} capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the C_{OUT} capacitor as shown in Figure 50. During this period C_{IN} is also being recharged by the V_{IN} . Minimizing C_{IN} loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the C_{IN} loop and C_{OUT} loop is vital to minimize switching and GND noise.

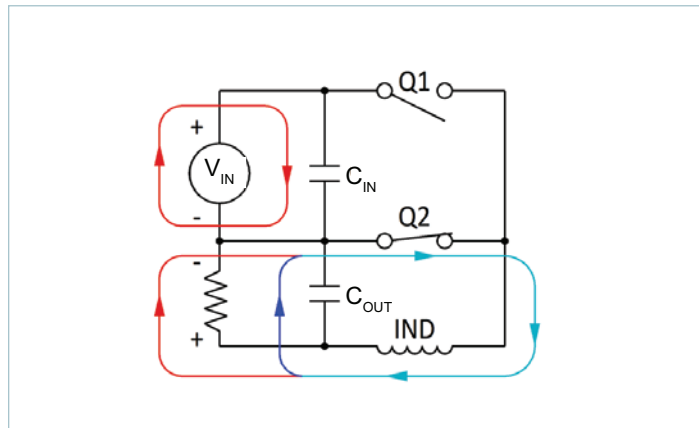


Figure 50 — Current flow: Q2 closed

The recommended component placement, shown in Figure 51, illustrates the tight path between C_{IN} and C_{OUT} (and V_{IN} and V_{OUT}) for the high AC return current. This optimized layout is used on the PI33xx evaluation board.

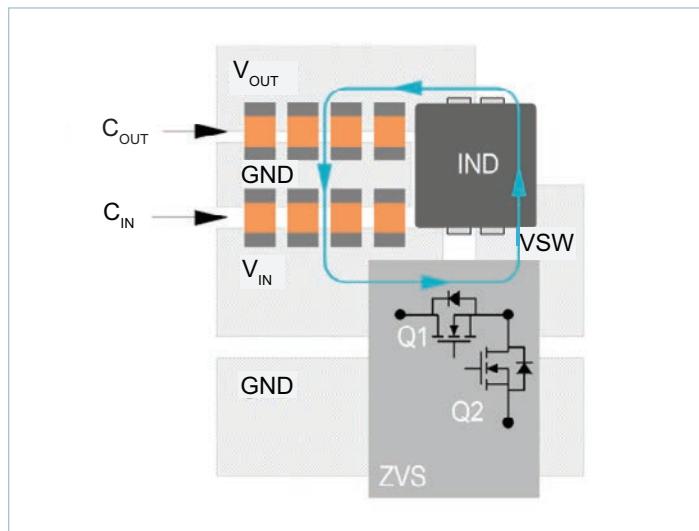
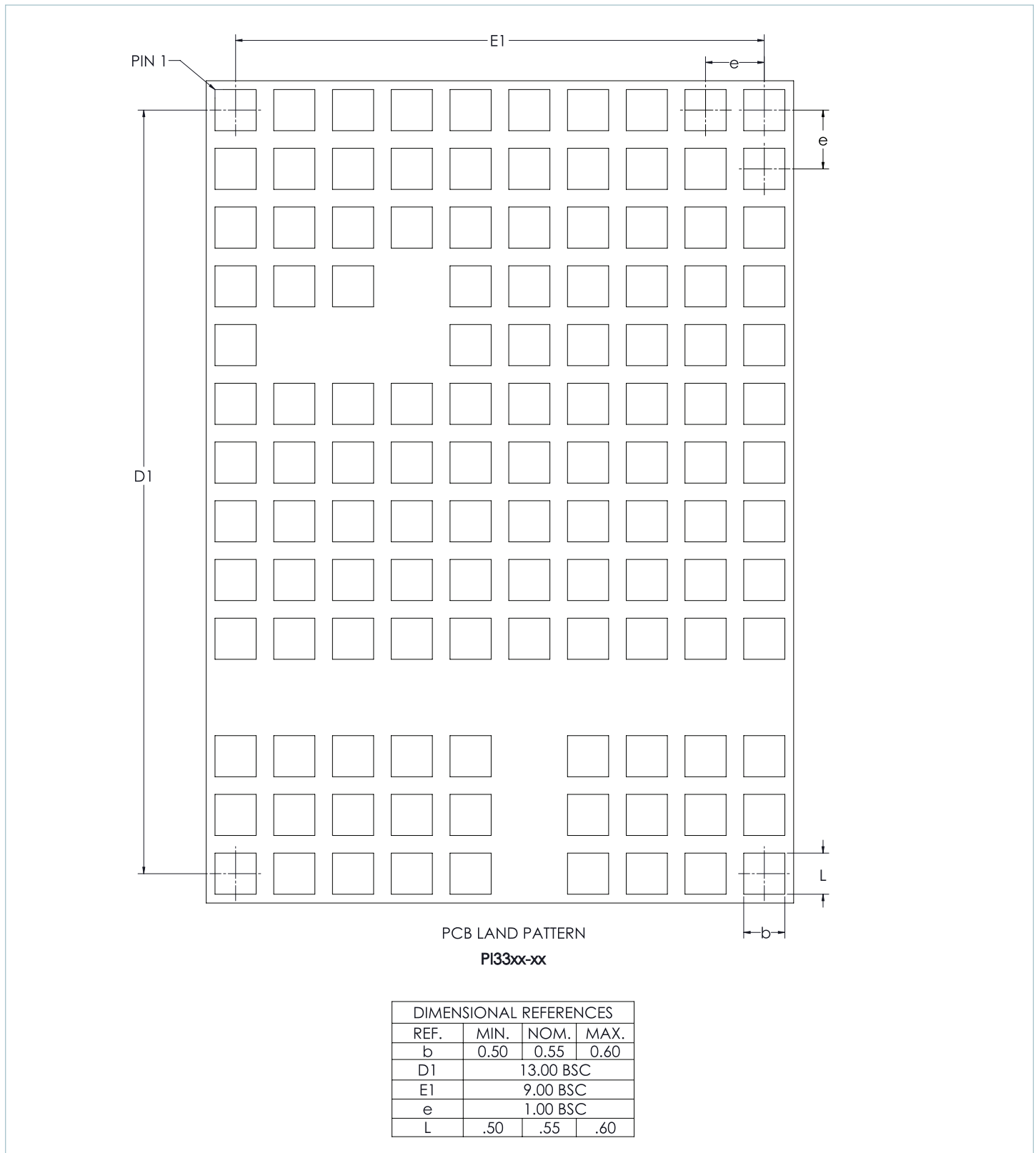


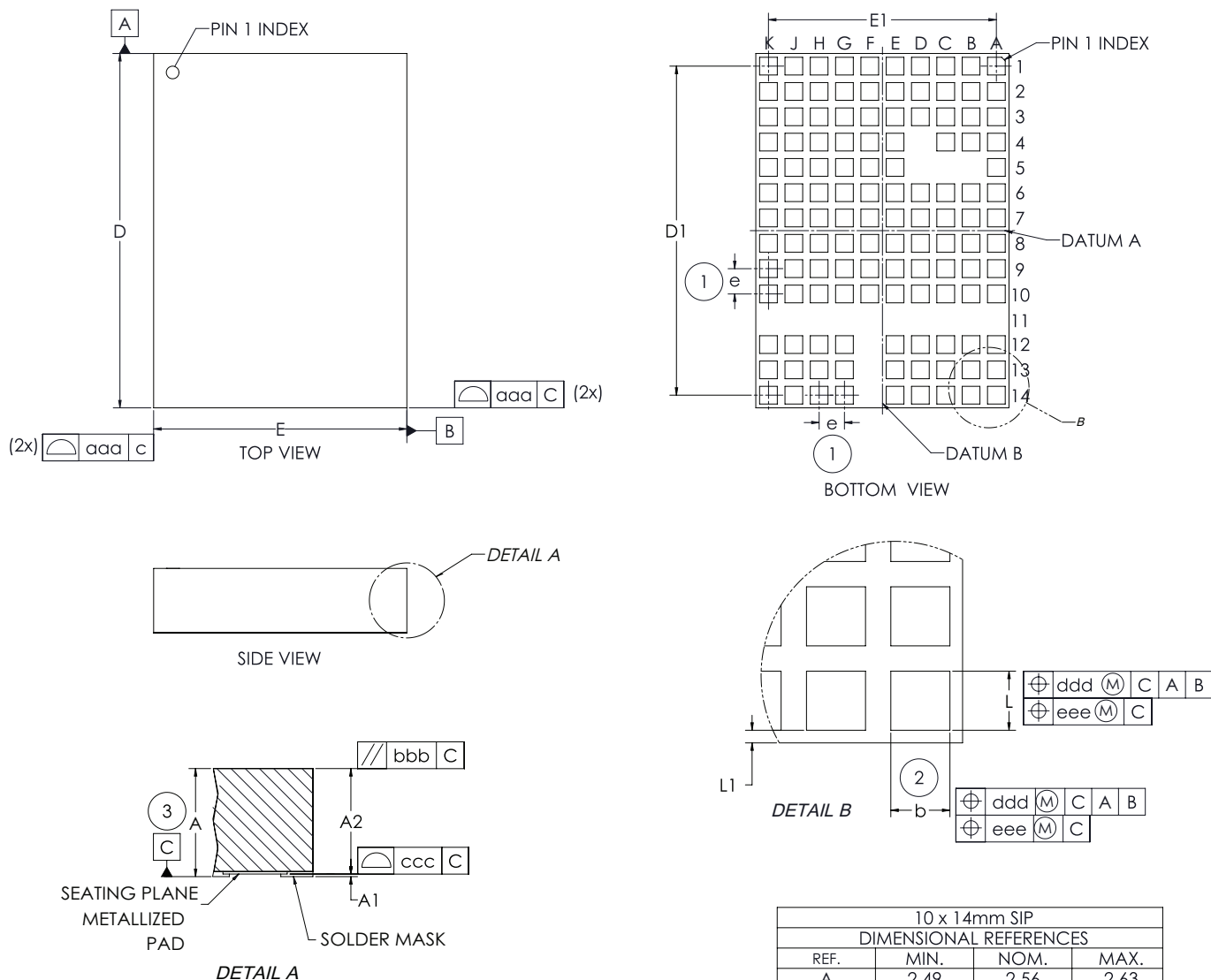
Figure 51 — Recommended component placement and metal routing

Recommended PCB Footprint and Stencil



Recommended receiving footprint for PI33x-x0 10 x 14mm package. All pads should have a final copper size of 0.55 x 0.55mm, whether they are solder-mask defined or copper defined, on a 1 x 1mm grid. All stencil openings are 0.45mm when using either a 5 or 6mil stencil.

Package Drawings



| 10 x 14mm SIP | | | |
|------------------------|-----------|-------|-------|
| DIMENSIONAL REFERENCES | | | |
| REF. | MIN. | NOM. | MAX. |
| A | 2.49 | 2.56 | 2.63 |
| A1 | -- | -- | 0.04 |
| A2 | -- | -- | 2.59 |
| b | 0.50 | 0.55 | 0.60 |
| L | 0.50 | 0.55 | 0.60 |
| D | 14.00 BSC | | |
| E | 10.00 BSC | | |
| D1 | 13.00 BSC | | |
| E1 | 9.00 BSC | | |
| e | 1.00 BSC | | |
| L1 | 0.175 | 0.225 | 0.250 |

| DIMENSIONAL REFERENCES | |
|------------------------|--------------------------------|
| REF. | TOLERANCE OF FORM AND POSITION |
| aaa | 0.10 |
| bbb | 0.10 |
| ccc | 0.08 |
| ddd | 0.10 |
| eee | 0.08 |

NOTES:

- 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
- DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
- DIMENSION 'A' INCLUDES PACKAGE WARPAGE
- EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
- ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.
- RoHS COMPLIANT PER CST-0001 LATEST REVISION.

Revision History

| Revision | Date | Description | Page Number(s) |
|----------|----------|---|--|
| 1.5 | 06/13 | Last release in old format | n/a |
| 1.6 | 08/03/15 | Reformatted in new template | n/a |
| 1.7 | 08/21/15 | Formatting edits | 6, 21, 22, 25, 26, 29, 30 & 36 |
| 1.8 | 09/18/15 | Formatting edits | all |
| 1.9 | 01/06/16 | Clarifications made in Enable Pin Conditions BGA package added | 7, 18, 22, 26 & 30 1, 3, 20–23, 34 & 40 |
| 2.0 | 02/22/16 | Corrected Input Current spec unit of measure from mA to A | 12, 16, 20, 24 & 28 |
| 2.1 | 05/27/16 | Revised Output Voltage Total Regulation | 12 |
| 2.2 | 08/22/16 | Corrected typo in temp range for Electrical Characteristics tables | 7, 9, 10, 12, 13, 16, 17, 20, 21, 24, 25, 28 & 29 |
| 2.3 | 11/21/16 | Clarified VS1 rating in Absolute Maximum Ratings Table Updated pin description table and package pin-out labels to show VDR capability | 4 5 |
| 2.4 | 02/10/17 | Block diagram typo corrected, VS1 Spec expanded PWRGD Pin Description updated Specification conditions clarified | 4 5 6, 9 |
| 2.5 | 06/01/17 | Move BGA package to separate data sheet Corrections | 1, 3, 20-23, 40 1, 6-7, 9-31, 35 |
| 2.6 | 04/03/20 | Updated mechanical drawings and pinout format (no mechanical changes) | 40 |
| 2.7 | 05/14/20 | Corrected REM absolute maximum rating Updated to add recommended Pulse Electronics inductors | 3 37 |
| 2.8 | 08/11/20 | Updated terminology | 36 |
| 2.9 | 12/21/20 | Separated end-of-life part numbers from main data sheet, added PI3301-01. (for PI3311-00, PI3318-00, PI3312-00, PI3311-20, PI3318-20, PI3312-20, PI3301-20, PI3302-20, PI3303-20, PI3305-20 data, see separate document) Updated ESD rating | All 3 |
| 3.0 | 02/24/21 | Revised input voltage slew rate, VIN UVLO/OVLO response time Revised TRK disable threshold and charge current (soft-start) | 7, 10, 14, 18, 22 8, 11, 15, 19, 23 |
| 3.1 | 04/23/21 | Updated internal divider values R1, R2 for PI3301-01-LGIZ | 29 |

Note: page removed in Revision 2.5; pages removed in Revision 2.9.

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