# PI3741-0x-EVAL1 <br> ZVS Regulators Buck-Boost Evaluation Board 

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## Introduction

The PI3741-0x-EVAL1 evaluation board demonstrates the features and benefits of the Vicor ZVS Buck-Boost regulator; pre-configured for either a 24 or 48 V output voltage and rated for up to 150W. Please refer to the corresponding PI3741-0x-LGIZ data sheet for all power specifications. The PI3741-0x-EVAL1 evaluation board is used with the following ZVS buck-boost products: PI3741-00-LGIZ, PI3741-01-LGIZ.

The evaluation board provides several options for applying input power (VIN and GND) and output load (VOUT and GND). The user can solder tab-style banana jacks or wire, use threaded connectors with retaining nuts or solder turret pins for clip-on connections.
The evaluation board comes with all of the PI3741-0x-LGIZ's features accessible to the user. The current-monitor function (IMON) is set up to monitor the PI3741-0x-LGIZ's output current, sensed across a $5 \mathrm{~m} \Omega$ resistor. The general purpose amplifier (VDIFF) comes pre-set with a gain of 2 , but can be easily reconfigured for differential measurements by adding extra 0603 resistors.
The I/O pins are brought out to the right edge of the evaluation board to allow for easy monitoring or for adding additional circuitry. The status of the PGD pin is indicated by a dual-colored LED; red indicating a fault and green indicating no faults. The SYNCO (sync out) and SYNCI (sync in) pins are accessible to allow for paralleling or for synchronizing to an external clock. Shorting J5 between IMON and VSP on the board will connect the output of IMON to the positive input of the general purpose amplifier, allowing for user-designed signal scaling and conditioning.
A footprint for an external Soft-Start capacitor (0603) is available to tailor the start-up profile of the converter. The error amplifier's output (EAO) is brought to a pin and in conjunction with the soft-start pin can be used for paralleling converters. The error amplifier's input (EAIN) is not directly connected to a pin, but connects to the pin EXT_VREF via a $10 \mathrm{k} \Omega$ series resistor. Applying a DC voltage to this pin will allow the user to change the regulated output voltage without changing the feedback network.
The board is designed with an edge connector to facilitate testing at the factory, but this connection can also be used for board evaluation. The PCB is 4-layer FR-4 170Tg material with 2 oz copper per layer, ENIG pad finish and a board thickness of 0.062in.

Bill of Materials


## Non-Populated Components

| Table 2 <br> Non-populated components | Qty | Reference Designator | Description |
| :---: | :---: | :---: | :---: |
|  | 3 | REA2, RIMON, RZ2 | Resistor, 1\%, 0.1W, 0603 |
|  | 4 | R1, R2, R3, R4 | Factory Use Only |
|  | 14 | EAO, EXT_VREF, PGD, IMON, SGND1, SGND2, SS/TRK, SYNCI, SYNCO, VDIFF, VDR, VIN, VSN, VSP | Thru-hole test points, Vector K24C |
|  | 3 | CEAIN1, CEAO, CTRK | Ceramic Cap, 50V, 0603 |
|  | 1 | CIN2 | Bi-Polar Capacitor, Nichicon UPW2A330MPD or equivalent |
|  | 2 | JVIN, JVOUT | Johnson Jack, Tektronix 131503100 |
|  | 3 | ENABLE, FT3, FT4 | SM Test point, Keystone 5015 |
|  | 1 | JGP | 0.1 in Header Jumper |
|  | 1 | C6 | Capacitor, Ceramic, 1206 |
|  | 1 | H1 | Factory Test Header |

Figure 1
Evaluation board schematic


Figure 2
Evaluation board details


## Typical Connections

Figure 4 illustrates the typical input supply and output load connections required to power the PI3741-x0 evaluation board. The test points on the right side of the board provide access to key nodes used to assess the board's performance. The jumper "JGP" provides an access point that allows the user to add a small signal in the feedback loop to make Gain/Phase measurements. The jumper J5 will connect the IMON output signal to the positive input of the general purpose amplifier, allowing this signal to be scaled. The J6 jumper will disable the converter when connected.

JVIN is an unpopulated "Johnson Jack" location that may be used to measure input ripple voltage.

Figure 3
Typical input and output connections


## Vicor PCB Edge Connector Description

SAMTEC Reference Mechanical Drawings: based on EXTreme LPHPower™ Socket Assembly series, available from Samtec's website PCB Dimensions:

- Recommended PCB layout for LPHS-XX-XX-X-VXX-XX PCB Layout.pdf
- Right-angle Socket: LPHS-XX-XX-X-RTX-XX-MKT.pdf

■ Vertical Socket: LPHS-XX-XX-X-VXX-XX-MKT.pdf

Figure 4
Edge connector details

## PAD Numbering

Figure 5
Top (component) view

Figure 6 Bottom view



## Schematic Symbol

Figure 7 Schematic of edge connector

NABLE
SDA
SCL

ADR1


## PAD Definitions

Table 3
PAD Definitions

| PAD | Name | Descirption |
| :---: | :---: | :---: |
| P1, P2 | PGND | Power ground connection for the input supply and output load |
| P3 | VOUT | Output voltage connection |
| P4 | VIN | Input voltage connection |
| 1, 2, 6, 7, 8, 10 | SGND | Signal ground used as reference for I/O measurements |
| 11, 12 | PGND | Power ground used as reference for input and output voltage measurements |
| 3 | ENABLE | Enable |
| 4 | SDA | Factory use only |
| 5 | SCL | Factory use only |
| 9 | ADR1 | Factory use only |
| 13 | DAC | External voltage node to adjust regulated output voltage (EXT_VREF) |
| 14 | EAO | Error amplifier output |
| 15 | VDIFF | Differential amplifier output |
| 16 | VSN | Differential amplifier inverting input |
| 17 | VPN | Differential amplifier non-inverting input |
| 18 | SYNCO | Sync output pin |
| 19 | SYNCI | Sync input pin |
| 20 | PGD | Power good status pin |
| 21 | ADRO | Factory use only |
| 22 | VDR | Internal generated 5.1V supply for gate drivers and internal logic |
| 23 | ISN | Remote-sensed output voltage, after the IMON resistor |
| 24 | VIN | Input supply voltage measured at SiP's input |

## PCB Design Files

ODB++ evaluation board design files are available for download on the Vicor website.

| Table 4 |  |  |  |
| :---: | :---: | :---: | :--- |
| Design files | Product | Deisgn <br> File Format | Link to Download |
|  | PI3741-Ox-EVAL1 | ODB++ | $\underline{\text { PI3741-Ox Eval ODB++.zip }}$ |

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