AdvancedTCA™ Hot-Swap with Active EMI Filter

Description:

The QPI-8 incorporates a total hot swap function with an EMI filter for DC/DC converter applications. The product aligns with the AdvancedTCA™ PICMG3.0® requirements for hot insertion and board level conducted noise limitations. The EMI filter provides active conducted common-mode (CM) and differential-mode (DM) noise attenuation from 150 kHz to 30 MHz. The QPI-8 is designed for use on a 48 or 60 volt DC bus (36-76VDC). The in-rush current limit (12A) and circuit breaker (6A) are designed to satisfy the 200W per board PICMG3.0® limit up to 70°C (T_A) before de-rating.

The under and over voltage thresholds can be trimmed separately via the UVEN and OV inputs using external series resistors. The Power Good active low output can be used to disable a converter until its input bulk capacitors are fully charged to the bus voltage. The QPI-8's active filter greatly reduces the amount of board space typically required for EMI filtering.

The QPI-8 is available as a lidded or an open-frame SiP (System-in-Package) with LGA mounting. Evaluation boards are available to allow for quick in-circuit testing of the QPI-8LZ within an existing system design.

Figure 1 *- QPI-8LZ (~1 in² area)*

Features:

- **40 dB CM attenuation at 250 KHz (50Ω)**
- **70 dB DM attenuation at 250 KHz (50Ω)**
- **80 Vdc (max input)**
- **100 Vdc surge 100 ms**
- **1,500 Vdc hipot hold off to shield plane**
- **6 A delayed circuit breaker rating, 12 A current limited**
- **25.3 x 25.3 x 5.2 mm Lidded SiP (System-in-Package)**
- **24.9 x 24.9 x 4.4 mm Open-frame SiP**
- **Low profile LGA package**
- **-40° to +125°C Ambient temperature (see Figure 19)**
- **Efficiency >99%**
- **Connect in series for higher attenuation**
- **TÜV Certified**

Applications

- **ATCA blades**
- **Telecom base stations**
- **IBA & distributed power**
- **Network switches and routers**
- **Optical line-cards**
- **TD-SCMA wireless infrastructure**

Typical Application:

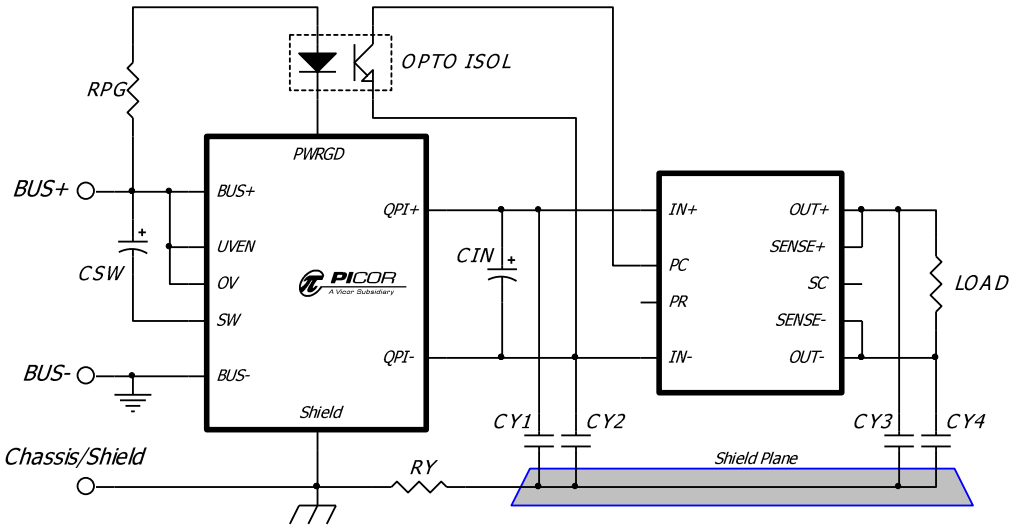


Figure 2 *– Typical QPI-8 application schematic with a Vicor Mini brick converter.* [1]

Note 1: *CSW capacitor, referenced in all schematics, is a 47uF electrolytic; United Chemi-Con EMVE101ARA470MKE0S or equivalent.*
CY1 to CY4, referenced in all schematics, are 4.7nF hi-voltage safety capacitors; Vishay VY1472M63Y5UQ63V0 or equivalent.
CIN is the converter manufacturer's recommended value for input capacitor. OPTO ISOL has a CTR of 200%, CEL PS2561 or equivalent.
The value of RPG is dependent on the selected Opto-isolator and QPI-8's PWRGD current limit.

Absolute Maximum Ratings – Exceeding these parameters may result in permanent damage to the product.

Input Voltage, BUS+ to BUS-, continuous	-80 to 80 Vdc
Input Voltage, BUS+ to BUS-, 100ms transient	-100 to 100 Vdc
BUS+/ BUS- to Shield pads, hi-pot	-1500 to 1500 Vdc
Input to output current, continuous @ 70°C T_A	5.5 Adc
Input to output current, Pulsed @ 25°C T_A	12 Adc
Power Good Sink Current; Power Good asserted low	5mA
Power dissipation, @ 70°C T_A, 5.5 A[(2)]	1.6 W
Operating temperature - T_A	-40 to 125 °C
Thermal resistance[(2)] - $R_{\theta J\text{-}A}$, using PCB layout in Figure 31	20 °C/W
Thermal resistance[(2)] - $R_{\theta J\text{-}PCB}$	8 °C/W
Storage temperature, JEDEC Standard J-STD-033B	-55 to 125 °C
Reflow temperature, 20 s exposure	245 °C
ESD, Human body model (HBM)	-2000 to 2000 V

Electrical Characteristics – Parameter limits apply over the operating temp. range, unless otherwise noted.

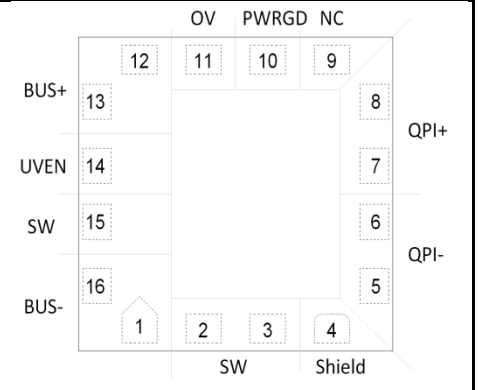
Parameter	Notes	Min	Typ	Max	Units
BUS+ to BUS- input range	Measured at 5.5 A, 70°C ambient temperature[(2)]	UV		80	Vdc
BUS+ to QPI+ voltage drop	Measured at 5.5 A, 70°C ambient temperature[(2)]		100		mVdc
BUS- to QPI- voltage drop	Measured at 5.5 A, 70°C ambient temperature[(2)]		185		mVdc
Common mode attenuation	VBUS = 48 V, Frequency = 250 KHz, line impedance = 50Ω		40		dB
Differential mode attenuation	VBUS = 48 V, Frequency = 250 KHz, line impedance = 50Ω		70		dB
Input bias current at 80 V	Input current from BUS+ to BUS-		15		mA
Load Current Prior to PWRGD	Max load current before inhibiting Hot-Swap start-up.			25	mA
Under-voltage Threshold (UV)	Controller Disabled to Enabled, no external trim-up.		34		V
Under-voltage Hysteresis	Controller Enabled to Disabled, no external trim-up.		UV - 2		V
Over-voltage Threshold (OV)	Controller Enabled to Disabled, no external trim-up.		76		V
Over-voltage Hysteresis	Controller Disabled to Enabled, no external trim-up.		OV - 4		V
Power Good Low Voltage	I_{PWRGD} = 1mA	0.2		0.6	V
Power Good Leakage Current	V_{PWRGD} = 90V			1	µA

Note 2: *See Figure 19 for the current de-rating curve.*

Pad Descriptions

Pad Number	Name	Description
12, 13	BUS+	Positive bus potential
1, 16	BUS-	Negative bus potential
7, 8	QPI+	Positive input to the converter
5, 6	QPI-	Negative input to the converter
4	Shield	Shield connects to the system chassis or to a safety ground.
10	PWRGD	Open drain output that asserts low when power in not good.
11	OV	High-side of Over-voltage resistor divider.
14	UVEN	High-side of Under-voltage resistor divider.
2, 3, 15	SW	Hot-Swap controlled negative rail of EMI filter.
9	NC	No internal connection, not used.

LGA Pattern (Top View)



Ordering Information

Part Number	Description
QPI-8LZ[(3)]	QPI-8 LGA Package, RoHS Compliant
QPI-8LZ-01	QPI-8 LGA Package, RoHS Compliant, Open Frame Package

Note 3: *QPI-8LZ is a non-hermetically sealed package. Please read the "Post Solder Cleaning" section on page 16.*

Applications Information

EMI Sources

Many of the components in today's power conversion modules are sources of high-frequency EMI noise generation. Diodes, high-frequency switching devices, transformers and inductors, and circuit layouts passing high dv/dt or di/dt signals are all potential sources of EMI.

EMI is propagated either by radiated or conductive means. Radiated EMI can be sourced from these components as well as by circuit loops that act like antennas and broadcast the noise signals to neighboring circuit paths. This also means that these loops can act as receivers of a broadcasted signal. This radiated EMI noise can be reduced by proper circuit layout and by shielding potential sources of EMI transmission.

There are two basic forms of conducted EMI that typically need to be filtered; namely common-mode (CM) and differential-mode (DM) EMI. Differential-mode resides in the normal power loop of a power source and its load; where the signal travels from the source to the load and then returns to the source. Common-mode is a signal that travels through both leads of the source and is returned to earth via parasitic pathways, either capacitively or inductively coupled.

Figure 8 and Figure 9 are the resulting EMI plots, after filtering by the QPI-8, of the total noise, both common and differential mode, of a Vicor Brick converter. These converters are mounted on a QPI-8 evaluation board and tested under various loads. The red and blue traces represent the positive and negative branches of total noise, as measured using an industry standard LISN setup, as is shown in Figures 6 and 7.

Differential-mode EMI is typically larger in magnitude than common-mode, since common-mode is produced by the physical imbalances in the differential loop path. Reducing differential EMI will cause a reduction in common-mode EMI.

Passive EMI Filtering

The basic premise of filtering EMI is to insert a high-impedance, at the EMI's base frequency, in both the differential and common-mode paths as it returns to the power source.

Passive filters use common-mode chokes and "Y" capacitors to filter out common-mode EMI. These chokes are designed to present a high-impedance at the EMI frequency in series with the return path, and a low impedance path to the earth signal via the "Y" caps. This network will force the EMI signals to re-circulate within a confined area and not to propagate to the outside world. Often two common-mode networks are required to filter EMI within the frequency span required to pass the EN55022 class B limits.

The other component of the passive filter is the differential LC network. Again, the inductor is chosen such that it will present a high-impedance in the differential EMI loop at the EMI's base frequency. The differential capacitor will then shunt the EMI back to its source. The QPI-8 was specifically designed to work with conventional switching frequency converters like Vicor's Brick products; Micro, Mini and Maxi modules; as well as converters from various vendors.

Active EMI Filtering

PICOR's QPI-8 active EMI filter uses the same basic principles for filtering as the passive approach, but its active common-mode filter can perform as well as a passive filter, when filtering lower frequencies, in much less board area.

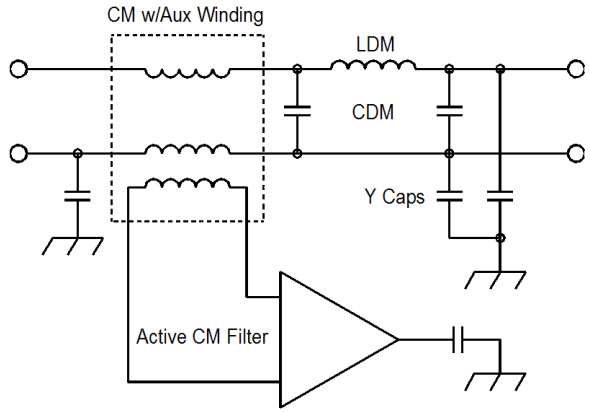


Figure 3 – *Simplified Active EMI filter circuit.*

Typically, the lower the frequency the greater the needed inductance would be to properly filter the EMI signal. This means either a larger core or a greater number of turns on a smaller core. A larger core requires more board space, where a smaller core with more turns has a greater amount of unwanted parasitics that can affect the filters ability to attenuate EMI signals.

Figure 3 is a simplified schematic of the QPI-8's active and passive circuitry used for EMI filtering. The QPI-8's active filter uses a small high-frequency common-mode transformer to filter the higher frequencies and adds a sensing element to it so that the lower frequency common mode signal can be sensed and a correction signal can be generated and inserted into the shield connection. By this means, the QPI-8 is capable of providing EMI filtering of converters in far less space than standard passive filters and can provide filtering over the entire EN55022 class B range.

EMI Management

The more effectively EMI is managed at the source, namely the power converter, the less EMI attenuation the filter will have to do. The addition of "Y" capacitors to the input and output power nodes of the converter will help to limit the amount of EMI that will propagate to the input source.

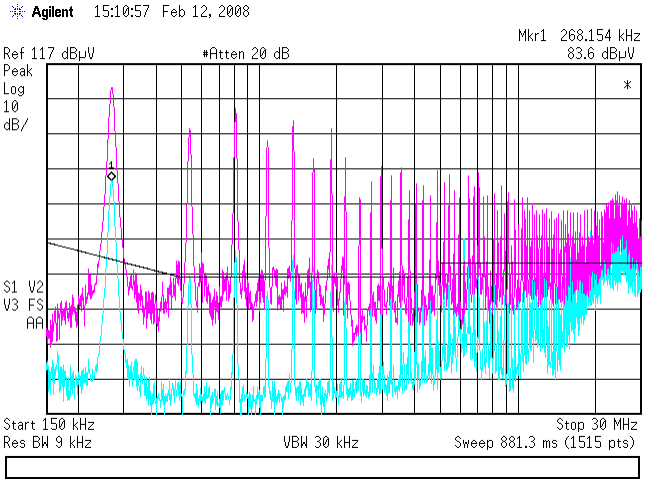


Figure 4 – *An unfiltered converter's response to "open-frame" (light blue) and "base-plate" (purple) EMI configurations.*

There are two basic topologies for the connection of the re-circulating "Y" capacitors, referred to as "open-frame" and "base-plate". Figure 4 illustrates how a converter can favor one topology versus another. The EMI generated by the "base-plate" configuration is much greater than that generated by the "open-frame". Selecting the right topology will greatly reduce the amount of EMI signal that needs to be filtered.

Figure 2 shows the base-plate topology of re-circulating "Y" caps. Here, CY1 to CY4 are connected to each power node of the dc-dc converter, and then are commoned together on a copper shield plane created under the converter. The addition of the copper shield plane helps in the containment of the radiated EMI, converting it back to conducted EMI and shunting it back to its source.

The RY resistor, connected between the shield plane and the QPI's shield pin, provides an impedance that makes the QPI's common mode noise cancelation signal more effective at removing the common mode noise that would normally return to the shield/earth connection. It is important when laying out the QPI that the RY resistor connects to the QPI's shield pin before making the connection to earth ground.

In Figure 5, the open-frame topology is shown where the "Y" capacitors (CY1 and CY2) re-circulate the EMI signals between the positive input and output, and the negative input and output nodes of the power conversion stage.

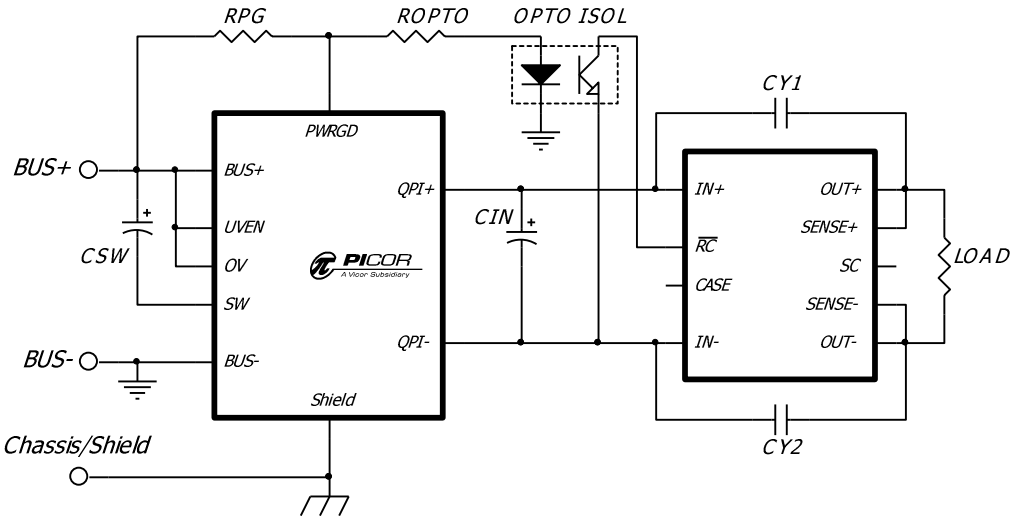


Figure 5 - *Typical 'open-frame" application using a converter with "low" enable.*

Attenuation Test Setups:

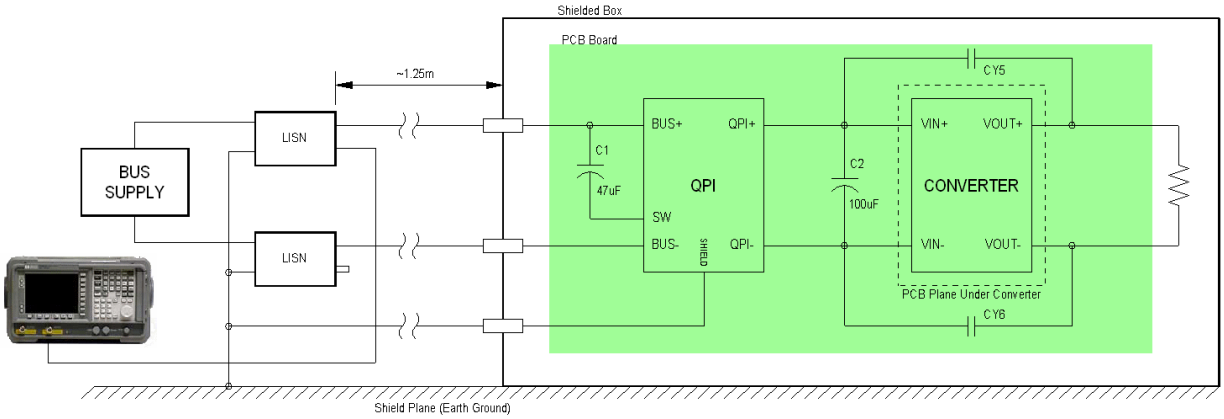


***Figure 6** - Open-frame EMI test setup using the QPI-8-EVAL1 carrier board with 48V converter.*

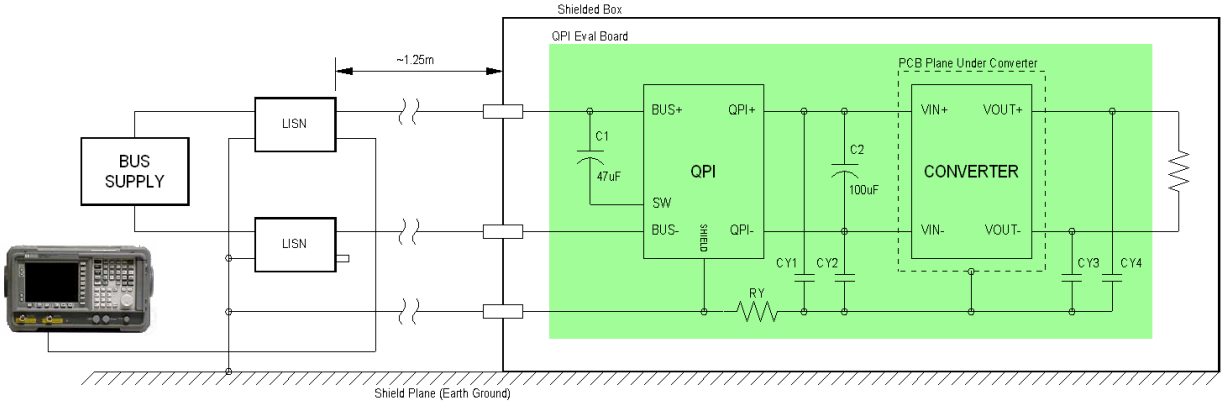


***Figure 7** - Base-plate EMI test setup using the QPI-8-EVAL1 carrier board with 48V converter.*

In Figures 6 and 7, C1 is the required 47uF capacitor (United Chemi-Con EMVE101ARA470MKE0S or equivalent), C2 is a converter input cap (value dependant on converter), and CY caps are 4.7nF ceramic (Murata GRM31BR73A472KW01L or equivalent).

Attenuation Plots:

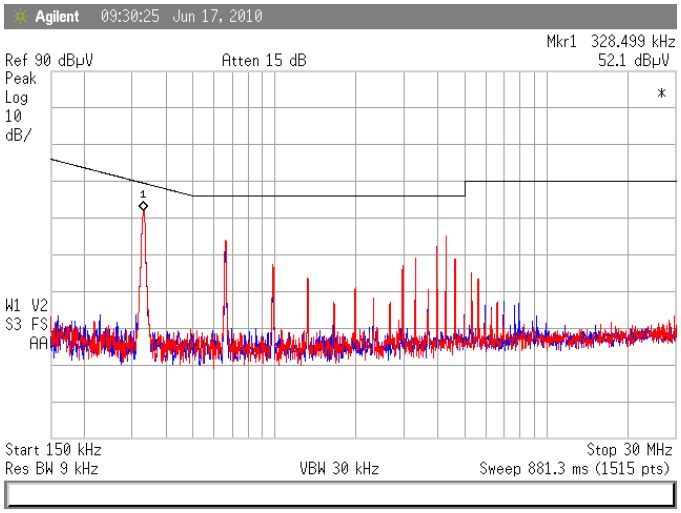


***Figure 8** - V48B12C250BN using base-plate "Y" capacitors with a 162W load.*

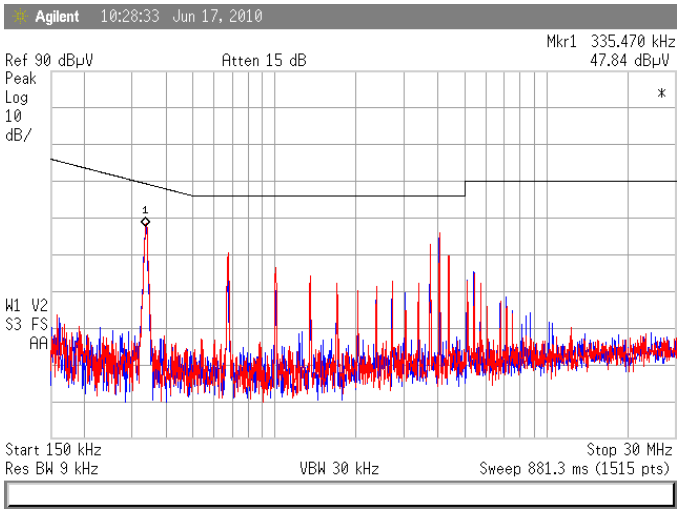


***Figure 9 –** V48B3V3C150BN using base-plate "Y" capacitors with a 141W load.*

Hot-Swap Function

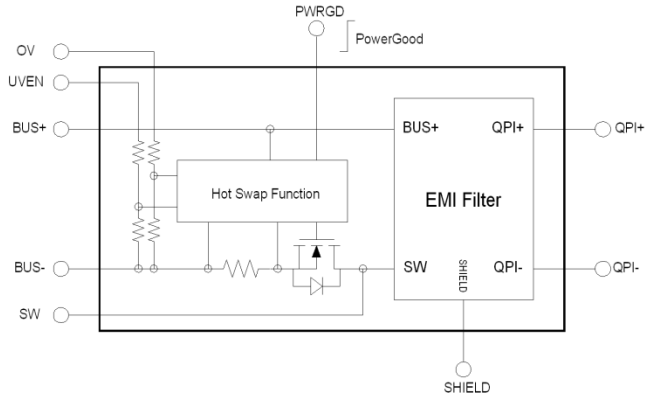


Figure 10 *- QPI-8 Block Diagram*

The hot-swap of the QPI-8 sits before the active EMI filter and is designed to align with the AdvancedTCA™ PICMG3.0® guidelines of 48V, 200W boards. Its 6A circuit breaker current rating allows the QPI-8 to provide 200W of power down to the minimum bus voltage of 36V. Its 12A maximum current limit allows for fast charging of a converter's input bulk storage capacitance. Its ability to "retry" after a circuit breaker fault time-out enables the QPI-8 to charge large amounts of bulk capacitance through multiple 12A current pulses before signaling that power is "good" via the PWRGD pin. This signal should be used to enable the QPI-8's load converter.

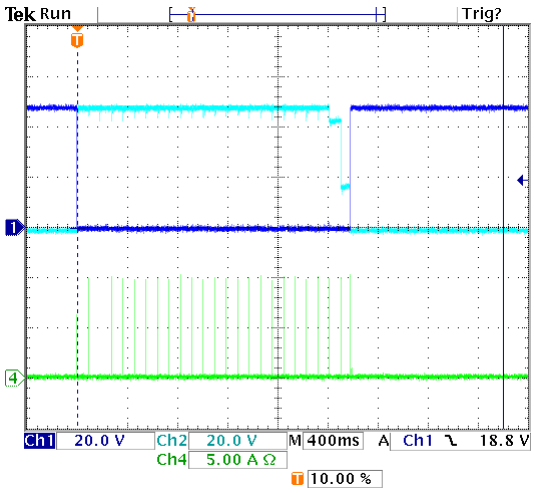


Figure 11 *- 2 second short applied across QPI-8's outputs.*

The waveforms shown in Figure 11 are of a running QPI-8 that has a short applied across its output for a 2 second duration. The *PWRGD* signal (blue, CH1) is initially high, the *VSW* voltage (light blue, CH2) is low with respect to *BUS-*, and the input current (green, CH4) is at a minimum load.

With a short applied, *PWRGD* drops to a low value and the voltage on *VSW* returns to the *BUS+* value. The QPI-8 detects a current fault and begins a cycle of trying to charge the bulk capacitors, then waiting. Once the short is lifted, the QPI-8 charges the bulk capacitor by the third pulse of current, also signaling that power is once again good. During the short circuit the input current is limited to 12A peaks, with an "on" duty cycle of about 1%.

The QPI-8 has a default under-voltage limit of 34V to turn on, and 32V to turn off. The over-voltage limit is 76V to turn off, 72V to turn on. The high-side of each resistor string is brought out to allow the user to trim up one or both of the voltage limits, or the pins can be connected directly to *BUS+* for the default under and over voltage limits. The equations in Figure 12 provide the new trip point voltages for a given added series resistor, R_{UVEN} and/or R_{OV}, as is shown in Figure 13.

Figure 12 – *Resulting UVEN and OV voltage equations based on selected series resistors.*

Having access to the high side of the internal resistor divider string enables the user to filter one or both nodes, allowing the QPI-8 to pass various transient requirements of PICMG3.0®.

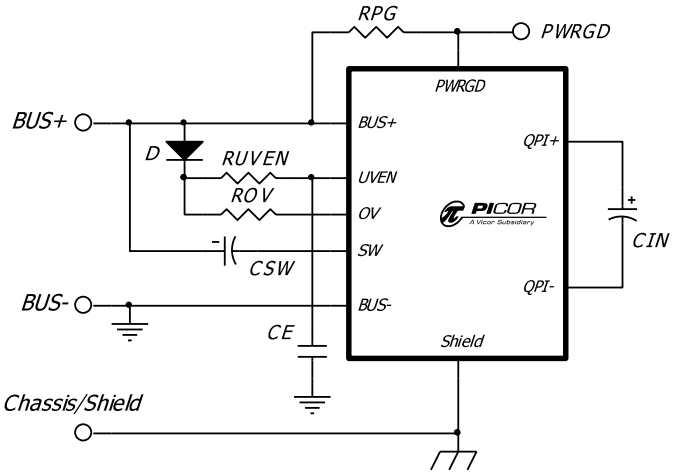


Figure 13 *- UVEN filtering for Zero-Volt BUS transients.*

The normal response of the QPI-8 to a BUS supply transient which drops below the UV limit is to assert the *PWRGD* pin low and shut off its pass FET. When the UV requirements are

once again satisfied the QPI-8 then will require ~16ms to restart and turn the pass FET back on, charging the bulk capacitance. The *PWRGD* signal will be low during the whole time of the transient, the 16ms delay and the time required to restore the BUS voltage across the bulk capacitors. See Figure 18 for a detailed description of the under and over voltage fault event timings.

The ATCA guidelines have a 5ms, zero-volt bus transient requirement that must be met. The circuit in Figure 13 shows that with the addition of a series diode (*D*), resistor (*RUVEN*) and a capacitor (*CE*), the *UVEN* pin can be filtered from reacting immediately to a transient loss of power, thereby maintaining a high *PWRGD* status and allowing the converter to run off of its bulk capacitors.

There is a practical limit to the amount of bulk capacitance that can be used as an energy source during a low voltage bus transient event. Upon recovery from the transient, the QPI-8 has to supply the current to charge the capacitors back to the BUS+ voltage value and provide the current for the converter in less time that the fault delay, about 1.2ms. If the caps cannot be completely charged prior to the fault time-out, then the QPI-8 will shut off its pass FET, assert the PWRGD pin low, and then retry about 95ms later.

For example: A system with a bus voltage of 48V and a 4A bus current has a drop in the bus voltage to 40V and then quickly recovers back to 48V. While at 40V the bus current increases to 4.8A to maintain the output load. To restore the bulk capacitor back to the 48V bus voltage the amount of bus current available, limited by the QPI-8's current limit of 12A, will be the 12A minus the average converter load current (4.4A). Without regard to tolerances, the equation to calculate the maximum amount of capacitance that can be charged within the 12A pulse period (1.2ms) is:

$$C = \frac{I \cdot \Delta t}{\Delta V}$$

Where $I = 4.4A$
$\Delta t = 1.2ms$
$\Delta V = 8V$

The value of the bulk capacitor is 1140µF; to maintain some margin for capacitor tolerance a 1000uF capacitor or smaller should be used.

Another option is to use a current limiting charge circuit to restore the capacitors. In Figure 14, the bulk storage capacitor (*CHOLD-UP*) is charged through *RC* after *PWRGD* has been released from its active low state and *QHOLD-UP* is allowed to turn on. The time it takes for *CHOLD-UP* to charge up to the bus supply voltage is dependent on the value of *RC* and *CHOLD-UP*. If the bus supply were to be removed, the energy stored in *CHOLD-UP* will be released through the diode *D* and the *QHOLD-UP* FET, which will conduct either by being actively turned on by *PWRGD* or through its body diode. Once the bus voltage is restored, *CHOLD-UP* will start to re-charge back to the bus supply voltage.

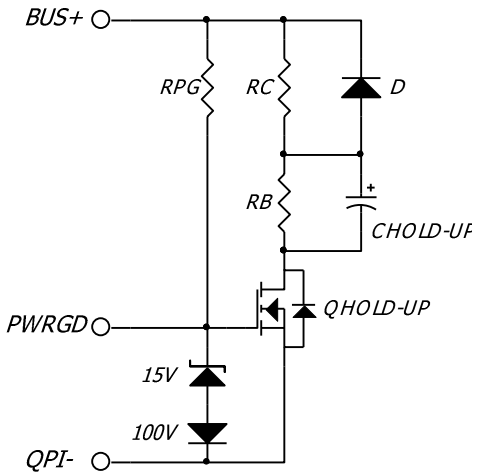


Figure 14 *- Powergood controlled, auxiliary bulk storage capacitor charging circuit.*

The amount of capacitance required can be determined using the following equation:

$$C = \frac{2E}{V_{BUS}^2 - V_{UVLO}^2}$$

Where: E = Hold-up energy
V_{BUS} = BUS supply voltage
V_{UVLO} = converter's UVLO limit

The 15V zener and 100V diodes are used to protect the FET's gate to source maximum voltage limit and to protect the QPI-8's *PWRGD* pin. At start-up, the voltage on *QPI-* is equal to *BUS+* with respect to *BUS-*. If the 100V diode were not present, then the *PWRGD* pin would be pulled up to the *BUS+* voltage minus the diode drop of zener. At start-up, the *PWRGD* pin is in an active low state and will get damaged being forced to the *BUS+* voltage. The zener diode protects against the FET's maximum gate to source voltage being exceeded.

The alternative to adding large amounts of bulk capacitors to the converter's input is to create a voltage supply greater than that of the bus supply. This takes advantage of the increased stored energy of a capacitor at higher voltages.

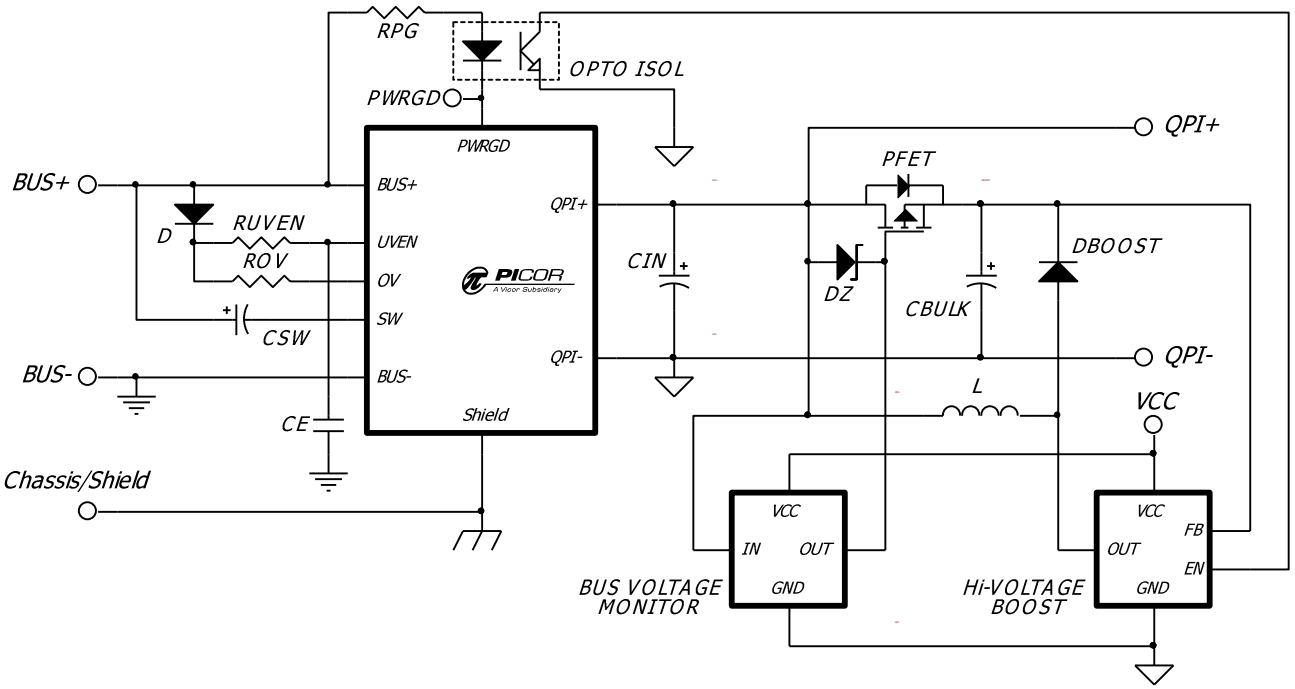


Figure 15 *- Simplified Hi-Voltage Boost Circuit for Charging Bulk Storage Capacitors.*

The circuit in Figure 15 shows a simplified version of a *PWRGD* enabled boost circuit. The bulk storage capacitance (*CBULK*) is initially charged to *BUS+*, along with the *CIN* capacitor, through the body diode of the PFET. Once these capacitors are fully charged, *PWRGD* enables the boost converter to slowly charge the bulk capacitance to the desired hi-voltage. When a low *QPI+* voltage is detected, the *BUS VOLTAGE MONITOR* circuit enables the PFET to discharge some of its energy into the load converter's *CIN* capacitor and to the load. When the *QPI+* rail reaches a pre-determined limit, it shuts off the PFET and the rail starts to drop again. This circuit acts much like a ripple regulator and will maintain the output load until either the BUS voltage is restored or the energy of the bulk capacitor is depleted.

The QPI-8 has a current sensing circuit that shuts off the internal pass FET if a high di/dt is sensed across its internal inductor. To avoid triggering this function, the PFET should be turned on in its linear region. Typically, a zener diode can be used to regulate the V_{G-S} of the PFET and the amount of energy discharged from the bulk capacitance. The waveforms in Figure 16 demonstrate a zero-volt bus transient and the response of the hi-voltage boost circuit. The storage caps provide energy to sustain the load, while the bus is at zero for 5ms. The input current (green, CH4) drops to zero while the load current (violet, CH3) remains constant. The voltage across the bulk storage caps (light blue, CH2) slowly decays while input voltage to the converter (blue, CH1) is regulated.

It is critical to keep the load current on the converter's input capacitor to less than 25mA during the initial start-up. This limit is set by the current limit level and the duty cycle of the circuit breaker timer, which is about 99% off time. An excessive load will discharge the bulk capacitors during the off time to a level where the on time charging current will never charge the capacitor to the full bus voltage. Only after Powergood has been established should the load be enabled.

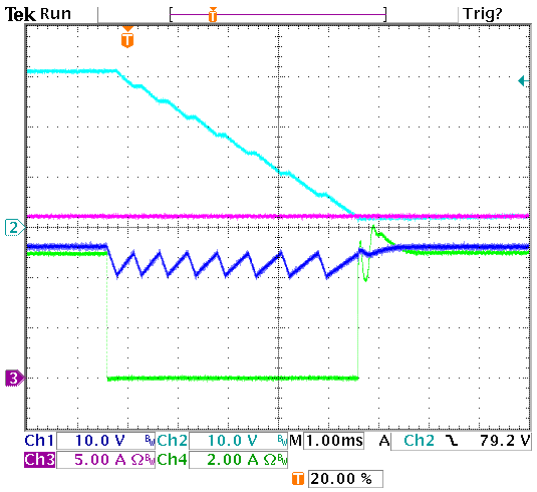


Figure 16 *- 5ms, 0V transient with 200W Load. CH1 and CH2 are offset by 50V DC.*

QPI-8 Timing Waveforms

The waveforms in Figure 17 are the typical start-up waveforms that would be seen in a system where two current pulses are required to completely charge the bulk capacitance to the bus voltage. The GATE waveform is an internal signal and cannot be measured externally; it is shown only for reference.

Once VIN is established and the UV and OV thresholds are satisfied, the internal FET's gate will start to get driven high after a 15ms delay. This delay allows for insertion de-bouncing. As the FET turns "on" and allows the passing of current the magnitude of the current is monitored. Once it reaches the 6A circuit breaker threshold an internal fault timer is started and the current is limited to a 12A maximum value. If the current does not drop to a value below the 6A circuit breaker limit before the fault timer ends then the gate is shut "off" and remains off for about 95ms. After this time the gate is again turned on and current is allowed to pass. Once the current is below the circuit breaker limit, the FET is fully turned "on" to its minimum r_{ds} value and the Powergood pin is released (open drain).

The change in voltage across *VSW* is dependent upon the value of the bulk capacitance that the QPI-8 is charging. The circuit breaker fault time is 300us when the voltage on *VSW* is greater than 40V, referenced to *BUS-*; or if there is no voltage change across *VSW* during the 12A current pulse, indicating a short across the bulk capacitor. Once below the 40V limit, and a decreasing voltage across *VSW*, the fault time is increased to 1.2ms to charge the bulk capacitors faster.

The timing waveforms for an OV (Over-voltage) and UV (Under-voltage) events are shown in Figure 18. After the initial start-up delay, the internal FET's gate is turned on. Once its gate-to-source voltage reaches 8V it releases the *PWRGD* pin and allows it to get pulled up to VIN.

In the event of an OV fault, the QPI-8 will turn off its internal FET and it will remain off until the OV fault is cleared. Once cleared, the gate immediately starts to turn back on. With an UV fault, the FET is again turned off, but the gate is not turned back on until 15ms after the UV fault has been cleared.

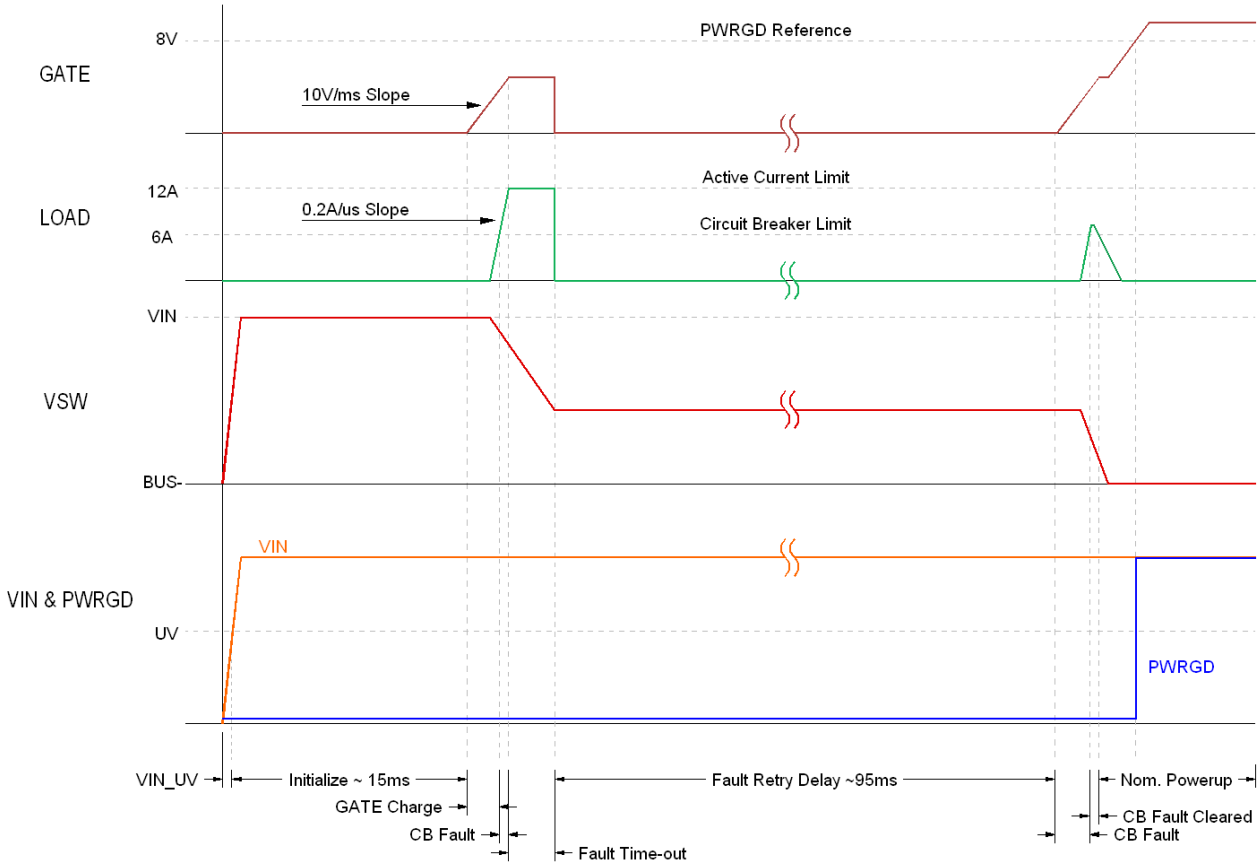


Figure 17 *- QPI-8 current fault timing diagram.*

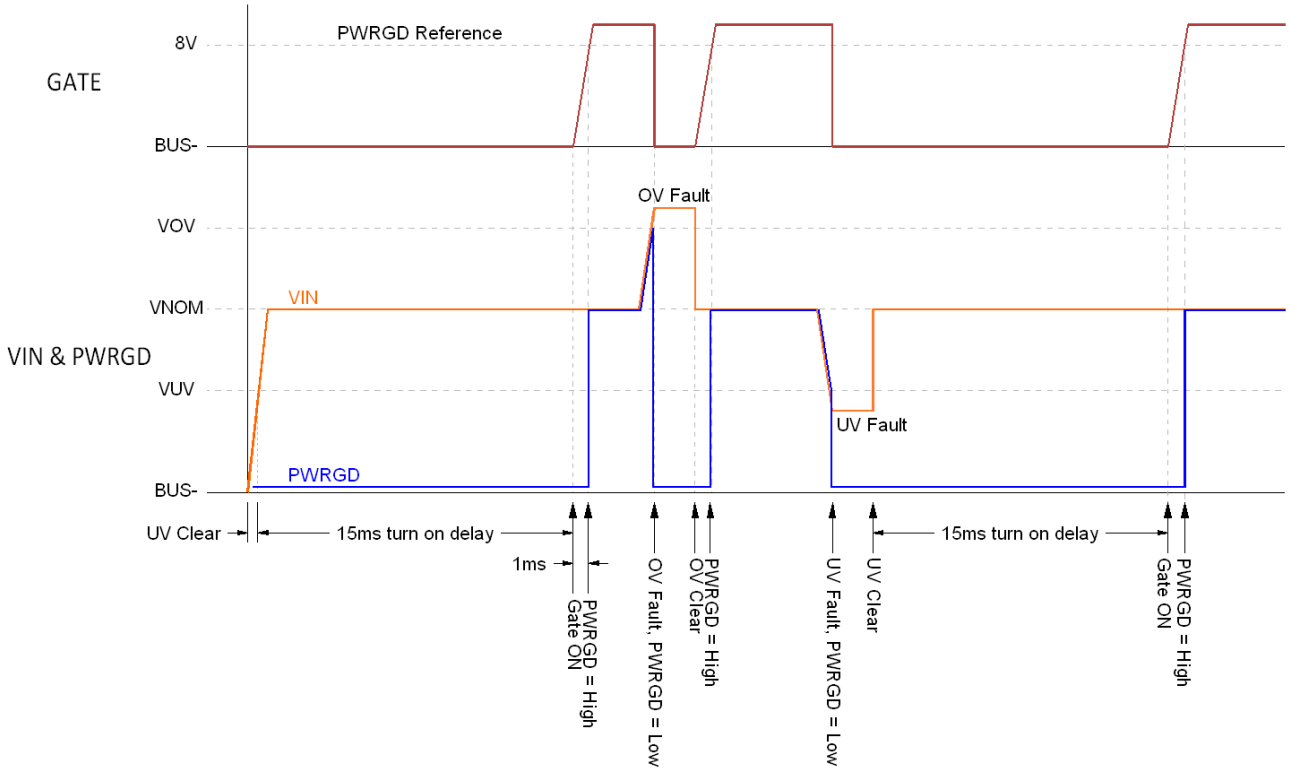


Figure 18 *– QPI-8 UV and OV fault timing diagram.*

Current De-Rating: *mounted to QPI-8-EVAL1 evaluation board.*

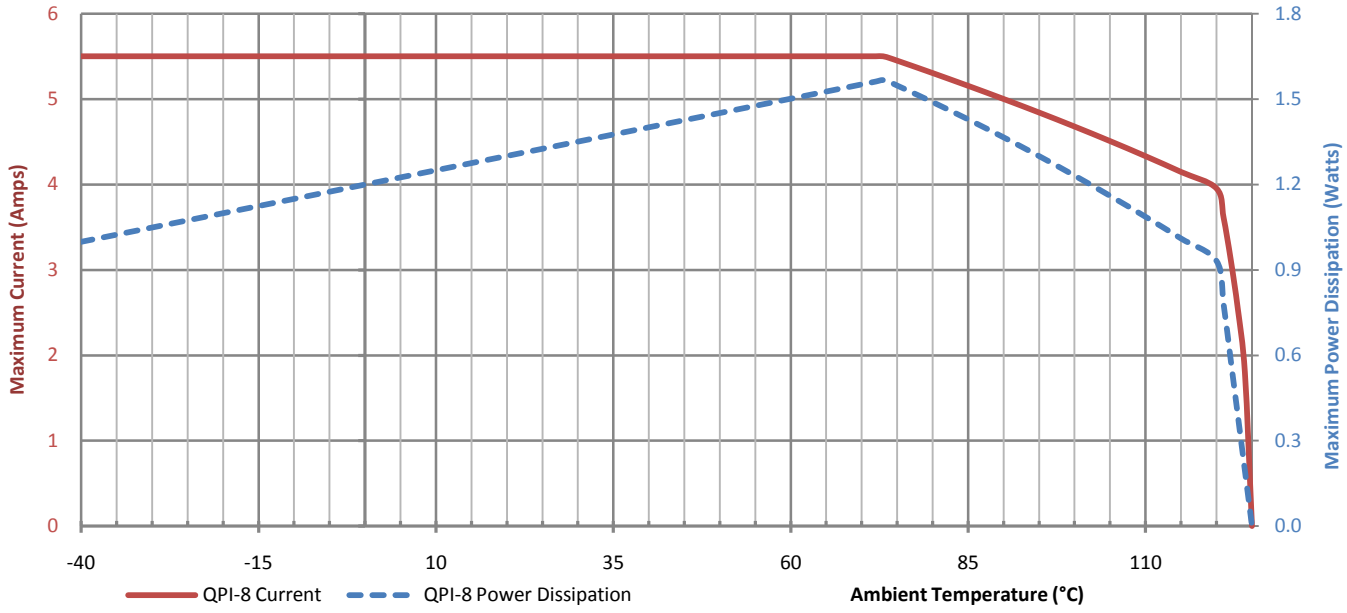


Figure 19 *- Current de-rating and power dissipation over ambient temperature range.*

The de-rating curve in Figure 19 is based on the maximum allowable internal component temperature and the 5.5A maximum rating of the QPI-8. The power dissipation curve is based on the current squared multiplied by the internal resistance between the inputs and outputs of the filter. The internal resistance value is temperature compensated for the power dissipation curve. The left axis (current) is in amps for the solid trace, the right axis (power) is in watts for the dashed trace.

QPI Application Circuits:

Filtering Dual Converters

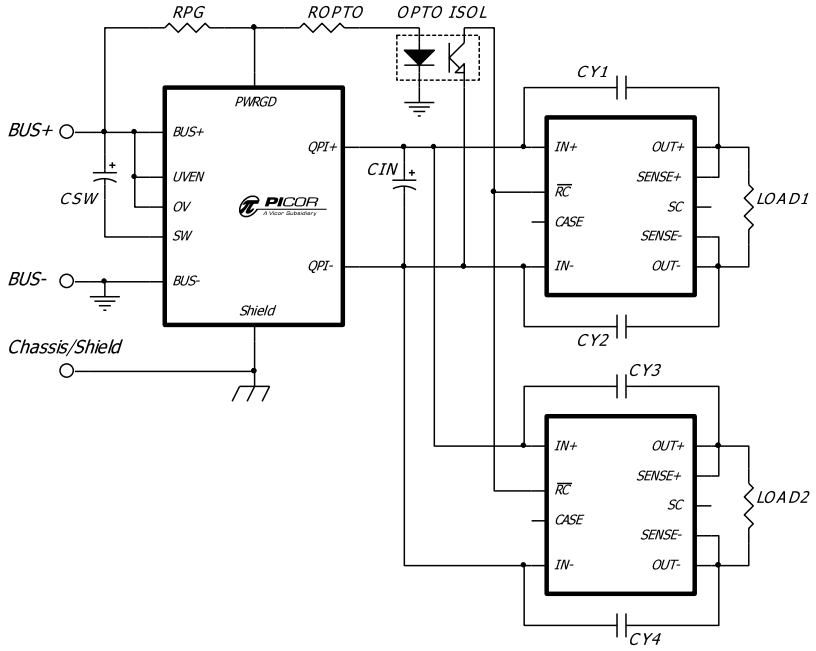


Figure 20 – *The QPI-8 filtering dual supplies, using an open frame topology.* [4]

Filtering Parallel Converters

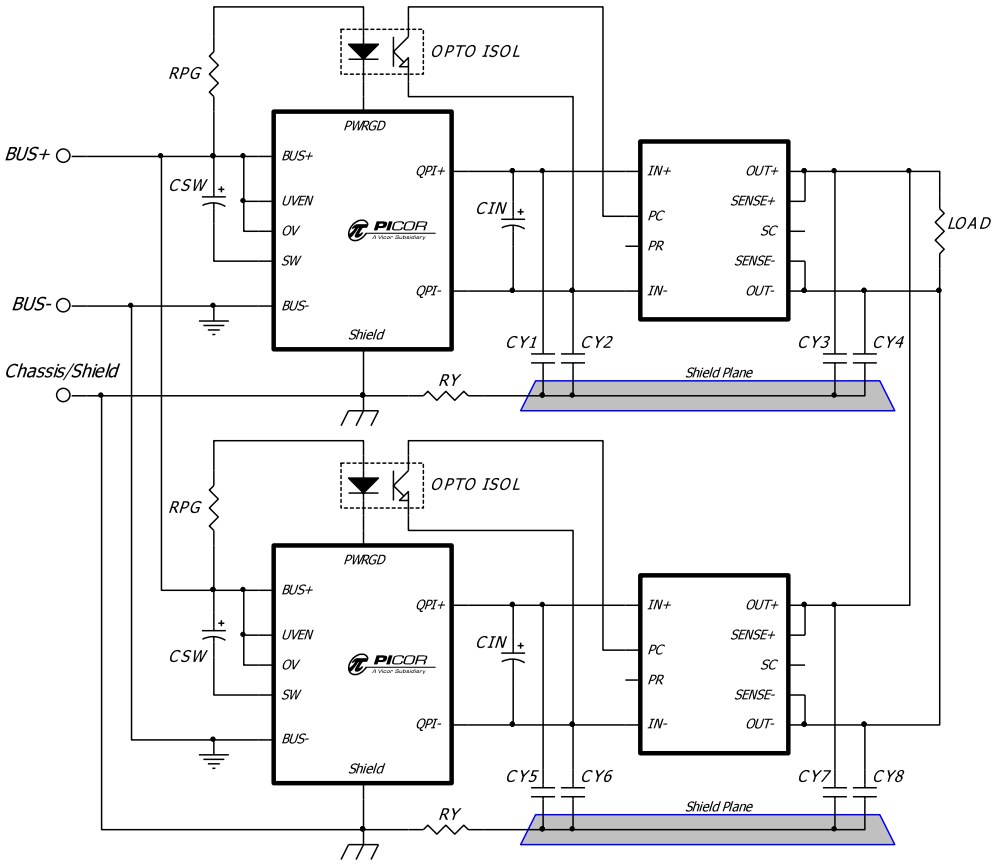


Figure 21 – *Dual QPI-8's filtering paralleled converters feeding a common load.* [4]

Note 4: *In Figures 12 and 13; CIN1 and CIN2, CY1 through CY8, should be the value and voltage rating recommended by the converter's manufacturer.*

The shield plane under the two converters in Figure 20 should be one contiguous plane under both. The circuit in Figure 20 is capable of filtering more converters than shown, up to the maximum current limit of the QPI-8. In Figure 21, a separate shield plane is required for each converter along with a separate RY resistor.

The QPI-8 is not designed to be used in parallel with another QPI-8 to achieve a higher current rating, but it can be used multiple times within a system design.

Output to Chassis Connection Using the QPI-8

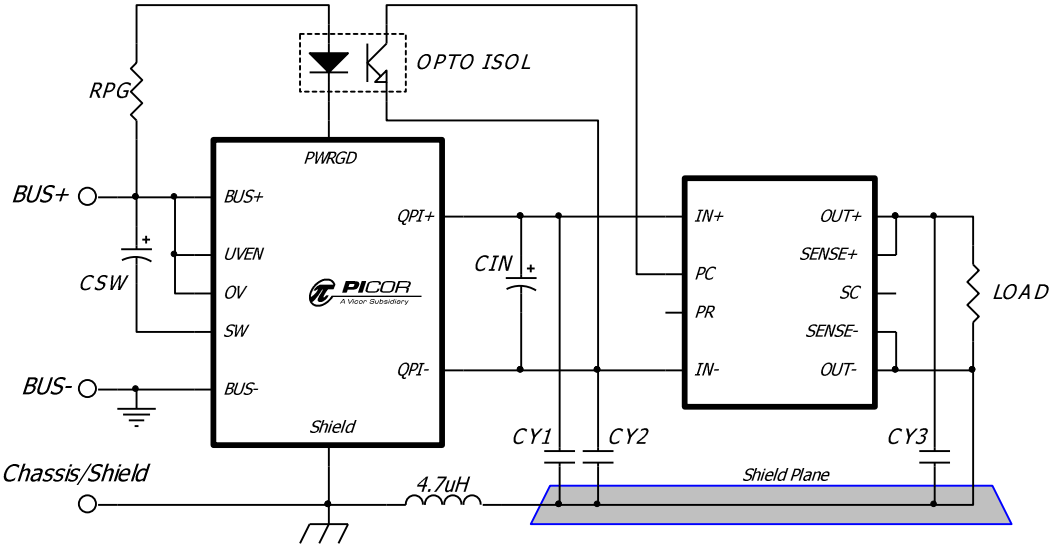


Figure 22 – *Connecting the converter's output ground to chassis through an inductor.* [4]

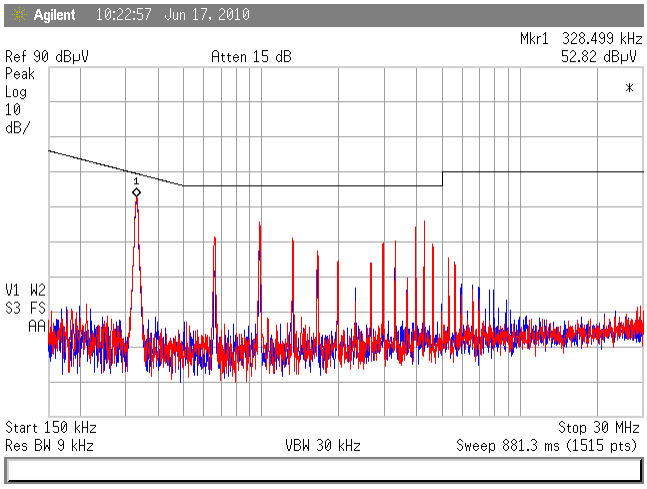
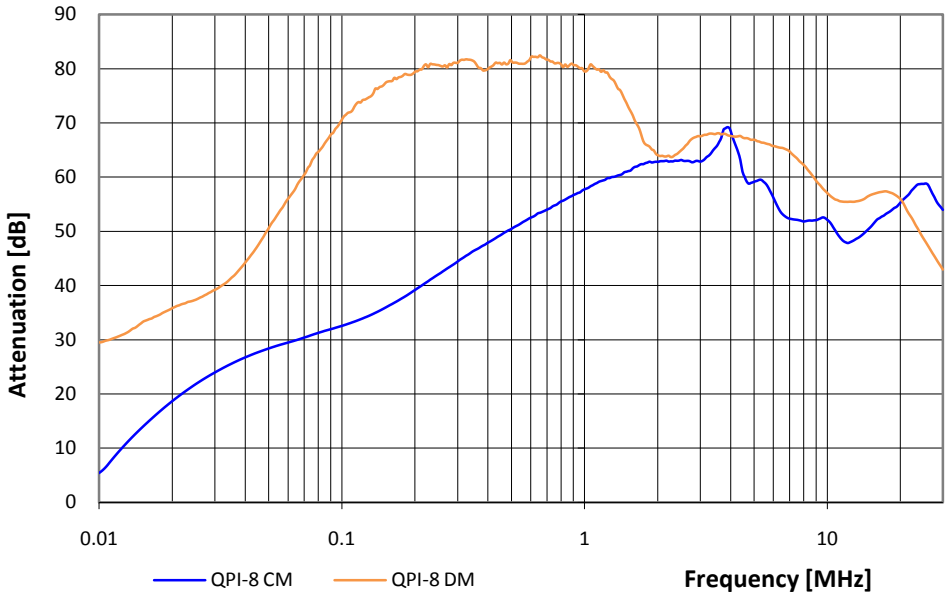


Figure 23 *-Total Noise EMI Plots of Vicor's V48B12C250BN, connected as shown in Figure 22*

The direct connection of the converter's output to the earth/chassis will degrade the EMI attenuation performance of the QPI-8. Picor recommends that the connection to the earth be made through a series inductor, rated to the maximum output current of the converter, as shown in Figure 22. The EMI plot shown in Figure 23 is of the same converter as in Figure 8, but uses an inductor in place of RY and has the converter's output ground connected to the shield plane.

The connection of the shield plane directly to the chassis/earth will also degrade EMI attenuation by the QPI-8 and is therefore not recommended.

QPI Insertion Loss Measurements



QPI Insertion Loss Equation:

Figure 24 *- Attenuation curves into a 50Ω line impedance, bias from a 48V bus.*

QPI Insertion Loss Test Circuits

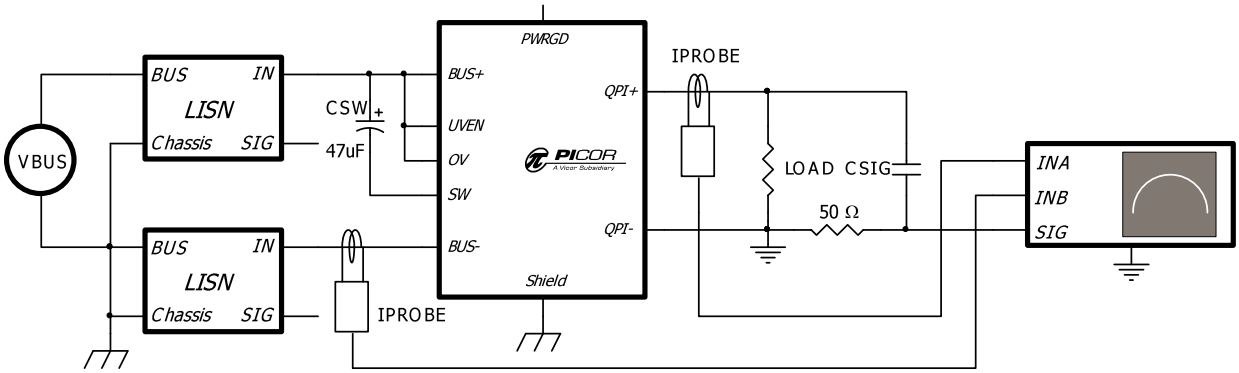


Figure 25 – *Test Set-up to measure Differential Mode EMI currents in Figure 24.*

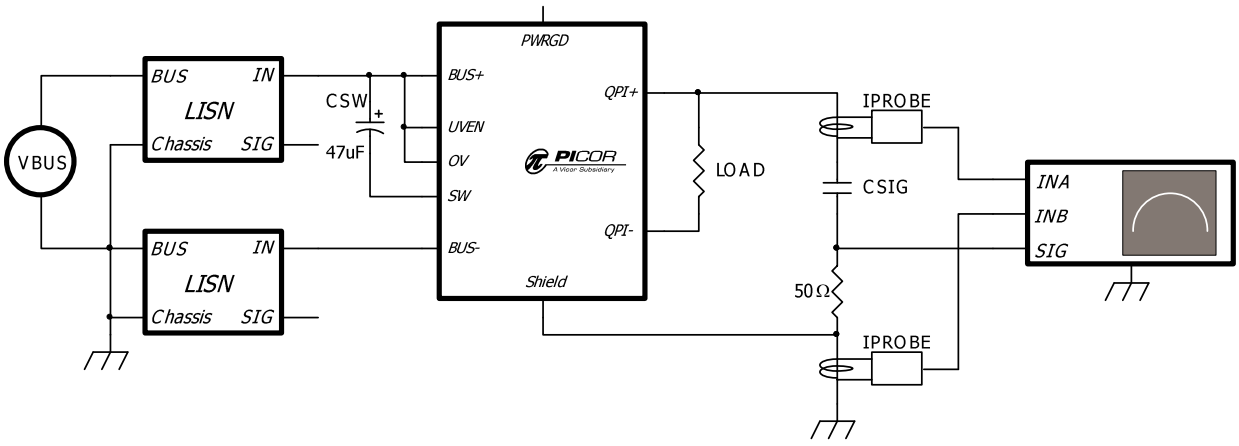


Figure 26 *- Test Set-up to measure Common Mode EMI currents in Figure 24.*

Mechanicals

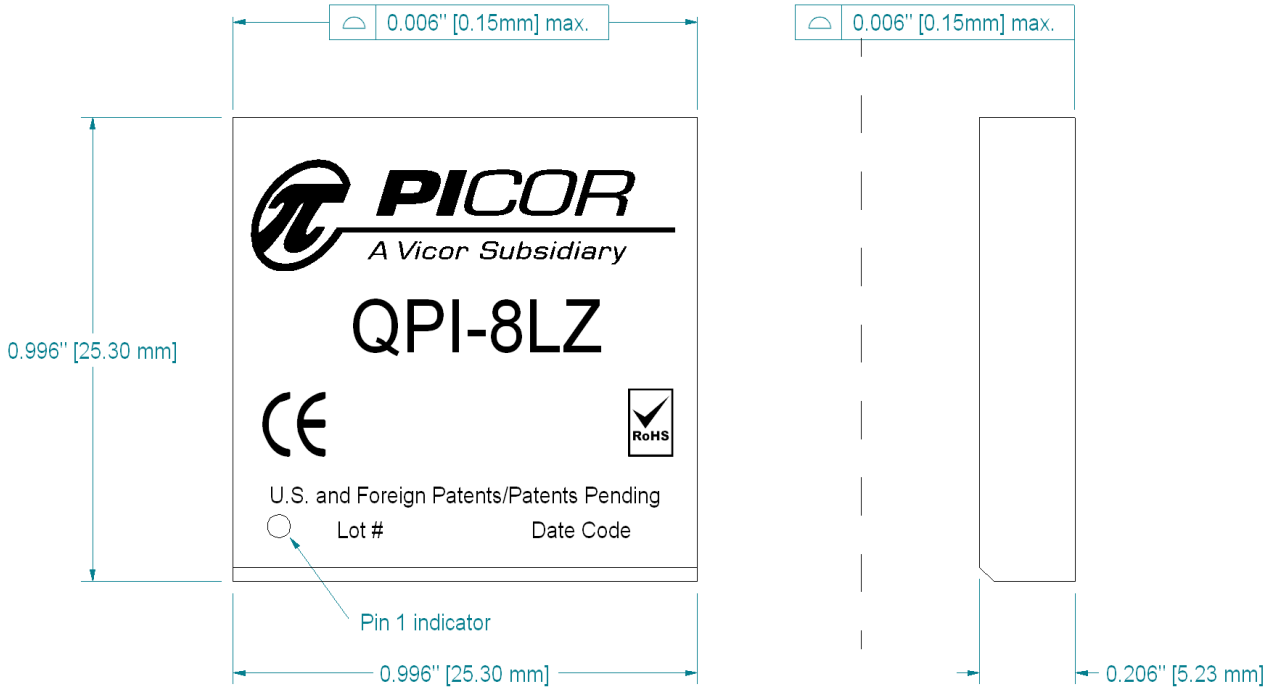


***Figure 27** - Lidded Package Dimensions, tolerance of ±0.004”*

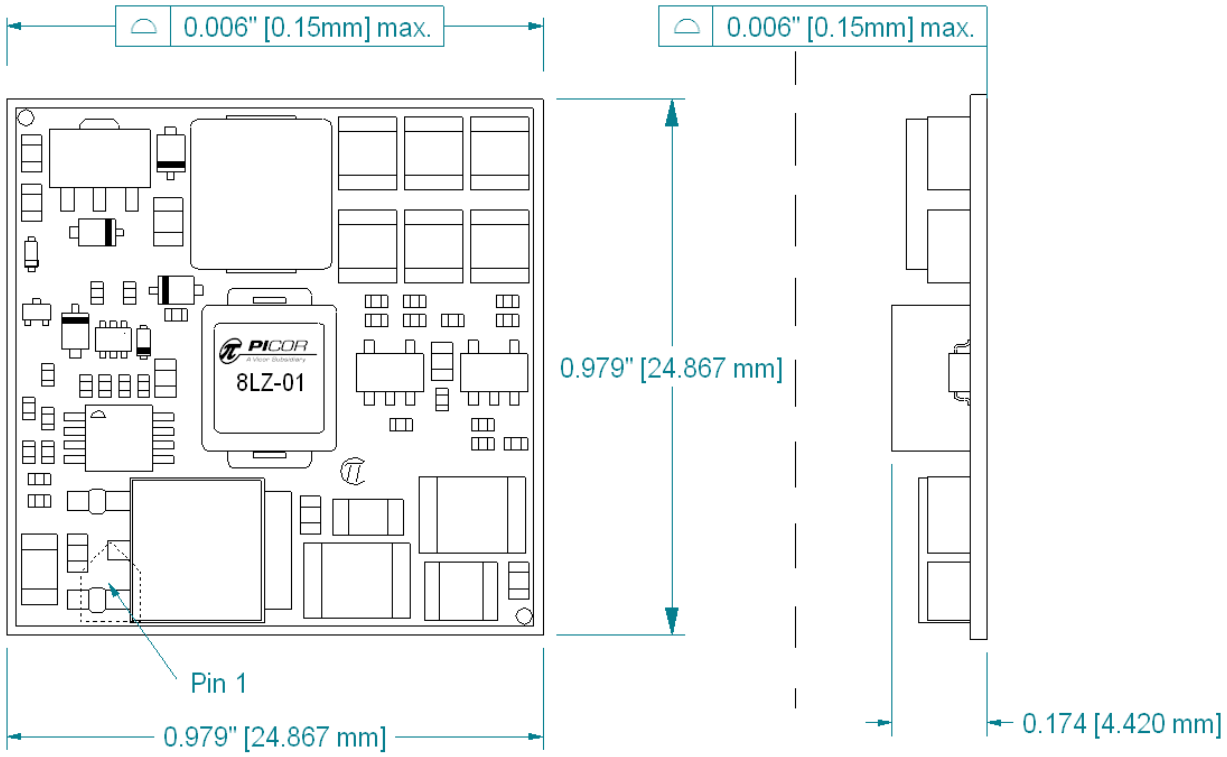


***Figure 28** - Open-frame Package dimensions, tolerance of ±0.004”. Pick and Place from label center.*

Pad and Stencil Definitions:

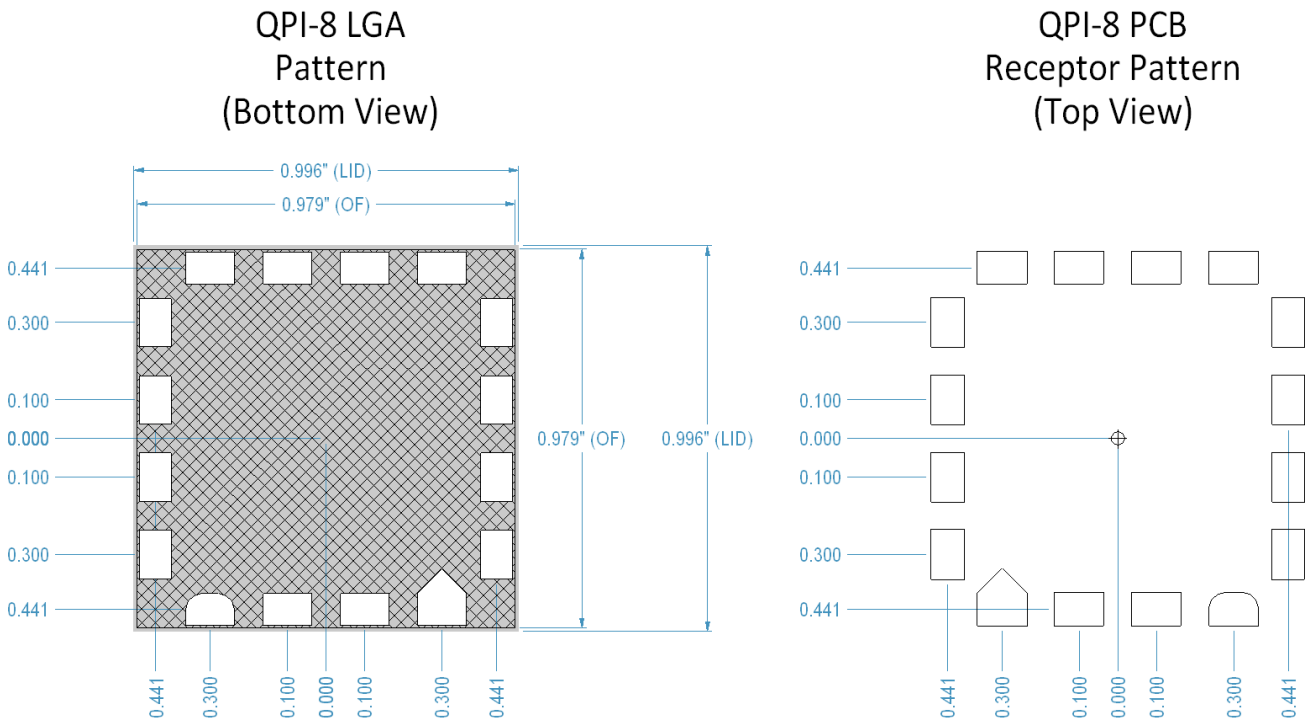


Figure 29 - *Bottom view of open-frame (OF) and lidded (LID) products. (All dimensions are in inches.)*

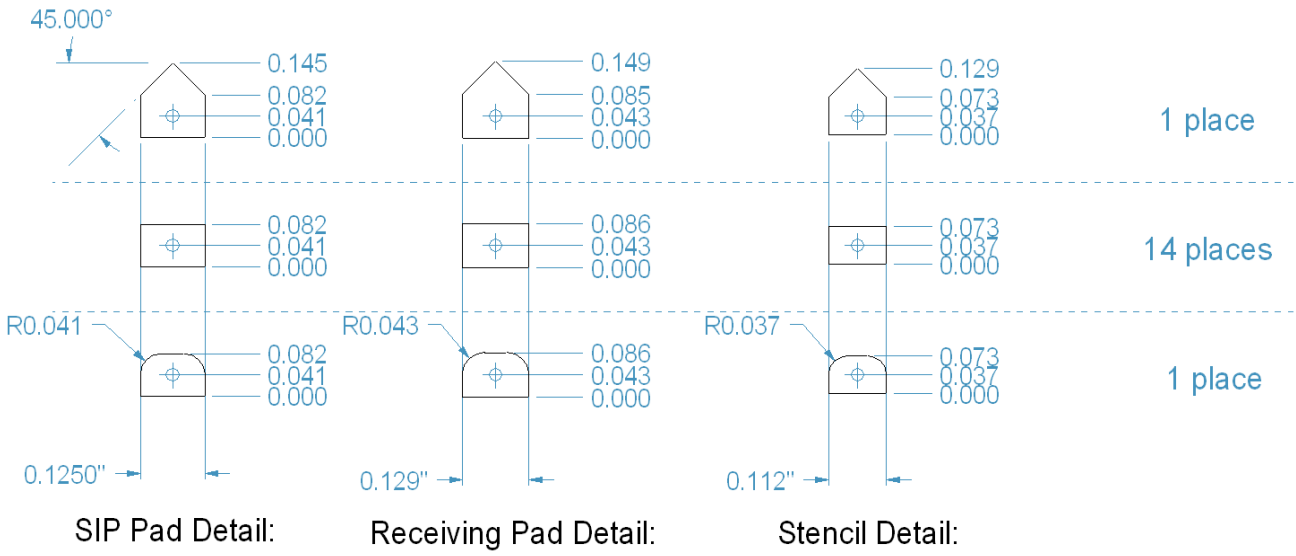


Figure 30 - *Recommended receptor and stencil patterns. (All dimensions are in inches.)*

Stencil definition is based on a 6mil stencil thickness, 80% of LGA pad area coverage. LGA Package dimensions are for both the Open-Frame and Lidded versions of the QPI-8.

QPI-8 PCB Layout Recommendations:

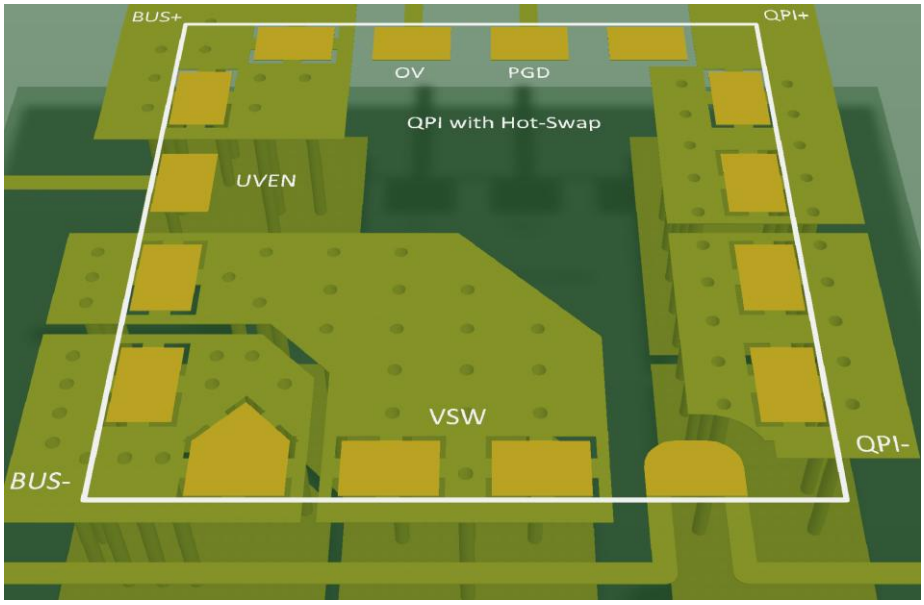


Figure 31 *- 3D view of paralleling planes underneath the QPI-8.*

PCB Layout

When laying out the QPI-8 EMI filter it is important for the designer to be aware of the radiated EMI field that all converters emit and to place the QPI-8 outside of this field area. It is also recommended that the bus lines feeding into the QPI filter are not routed such that they lie between the QPI and the converter, or that their copper planes over-lap on inner layers. This can cause EMI noise to be coupled from input to output via the parasitic capacitance between the planes. In Figure 31, the QPI-8 is located ~1.5 inches from the converter's input pins to keep the radiated EMI from by-passing the filter and coupling directly to the BUS feeds.

Post Solder Cleaning

Picor's LZ version QP SIPs are not hermetically sealed and must not be exposed to liquid, including but not limited to cleaning solvents, aqueous washing solutions or pressurized sprays. When soldering, it is recommended that no-clean flux solder be used, as this will ensure that potentially corrosive mobile ions will not remain on, around, or under the module following the soldering process. For applications where the end product must be cleaned in a liquid solvent, Picor recommends using the QPI-8LZ-01, open-frame version of the EMI filter.

QPI-8 Mechanical Data

Datum	Units	QPI-8LZ	QPI-8LZ-01	Notes
FITS	Failure/Billion Hrs.	330	330	FITS based on the BellCore Standard TR-332
MTBF	Million Hrs.	3	3	MTBFs based on the BellCore Standard TR-332
Weight	grams	4.7	3.4	
MSL		3	3	
Peak reflow Temperature	°C/20 seconds	245	245	IPC/JEDEC J-STD-020D

QPI-8 Evaluation Boards	
Part #	**Description:**
QPI-8-EVAL1	A QPI-8LZ mounted on a small evaluation board with screw terminal blocks to allow for easy connection into an existing system.
QPI-8-CB1	A QPI-8LZ mounted on a carrier board designed for use with DOSA compliant footprint dc-dc converters. Screw terminal blocks to allow for easy connection into an existing system.

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Vicor Corporation
25 Frontage Road
Andover, MA 01810
USA

Picor Corporation
51 Industrial Drive
North Smithfield, RI 02896
USA

Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com
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