

## N-CHANNEL

PART #	$V_{(BR)DS}$ (V)	$r_{DS(ON)}$ ( $\Omega$ )	$V_{GS(th)}$ (V)	$t_{ON}$ (ns)	$C_{iss}$ (pF)	$I_D$ (mA)	PD
<b>14-PIN CERAMIC (P) &amp; PLASTIC (J)</b>							
VQ1001J	30	1	2.5	30	38	0.85	2
VQ1001P	30	1	2.5	30	38	0.85	2
VQ1004P	60	3.5	2.5	10	35	0.46	2
VQ1004J	60	3.5	2.5	10	35	0.46	2
VQ1000J	60	5.5	2.5	10	16	0.23	2
VQ1000P	60	5.5	2.5	10	16	0.23	2
VQ1006P	90	4.5	2.5	10	35	0.40	2
VQ1006J	90	4.5	2.5	10	35	0.40	2
<b>SOT-23</b>							
VN0603T	60	4	3.0	15	16	0.22	0.36
VN0605T	60	5	3.0	20	16	0.18	0.36
2N7002	60	8	2.5	20	16	0.12	0.2
2N7001	240	45	2.5	30	15	0.05	0.2
VN45350T	450	350	4.5	25	5	0.02	0.35
VN50300T	500	300	4.5	20	5	0.02	0.35
<b>TO-205AD (TO-39)</b>							
VN0300B	30	1.2	2.5	30	38	1.51	5
2N6659	35	1.8	2.0	10	38	1.40	6.25
2N6660JANTX	60	3	2.0	10	30	0.99	6.25
2N6660	60	3	2.0	10	38	1.10	6.25
VN67AB	60	3.5	2.5	15	35	0.79	5
2N6661JANTX	90	4	2.0	10	30	0.86	6.25
2N6661	90	4	2.0	10	35	0.90	6.25
VN90AB	90	5	2.0	10	35	0.67	5
VN1206B	120	6	2.0	16	35	0.22	5
VN1706B	170	6	2.0	16	105	0.63	6.25
VN2406B	240	6	2.0	16	110	0.63	6.25
VN4012B	400	12	1.8	40	80	0.42	0.8
<b>TO-206AC (TO-52)</b>							
VN10LE	60	5	2.5	10	16	0.38	1.5
VN10KE	60	5	2.5	10	38	0.17	0.3

# 2N7002

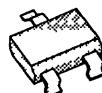
**Siliconix**  
incorporated

N-Channel Enhancement-Mode MOS Transistor

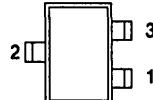
## PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ ( $\Omega$ )	$I_D$ (A)	PACKAGE
60	7.5	0.115	SOT-23

SOT-23



TOP VIEW



1 GATE  
2 DRAIN  
3 SOURCE

Performance Curves VNDS06 (See Section 7)

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	2N7002	UNITS
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 40$	
Continuous Drain Current	$I_D$	$\pm 0.115$	A
		$\pm 0.073$	
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	0.8	mW
Power Dissipation	$P_D$	200	
		80	
Operating Junction Temperature	$T_J$	-55 to 150	
Storage Temperature	$T_{stg}$	-55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)	$T_L$	300	

## THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N7002	UNITS
Junction-to-Ambient	$R_{thJA}$	625	°C/W

<sup>1</sup>Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS <sup>1</sup>			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP <sup>2</sup>	2N7002		UNIT
				MIN	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 μA	70	60		V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 0.25 mA	2.15	1	2.5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V V <sub>GS</sub> = ±20 V	±1		±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 60 V	0.02		1	μA
On-State Drain Current <sup>3</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> ≥ 2 V <sub>DS(ON)</sub> , V <sub>GS</sub> = 10 V	1000	500		mA
Drain-Source On-Resistance <sup>3</sup>	r <sub>DS(ON)</sub>	V <sub>GS</sub> = 5 V I <sub>D</sub> = 50 mA	5		7.5	
		T <sub>C</sub> = 125°C	9		13.5	Ω
		V <sub>GS</sub> = 10 V I <sub>D</sub> = 0.5 A	2.5		7.5	
Drain-Source On-Voltage <sup>3</sup>	V <sub>DS(ON)</sub>	T <sub>C</sub> = 125°C	4.4		13.5	
		V <sub>GS</sub> = 5 V, I <sub>D</sub> = 50 mA	0.25		0.375	V
		V <sub>GS</sub> = 10 V I <sub>D</sub> = 0.5 A	1.25		3.75	
Forward Transconductance <sup>3</sup>	g <sub>fs</sub>	4T <sub>C</sub> = 125°C	2.2		6.75	
		V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.2 A f = 1 kHz	170	80		μs
Common Source Output Conductance <sup>3,4</sup>	g <sub>os</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 50 mA	500			μs
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V V <sub>GS</sub> = 0 V f = 1 MHz	16		50	
Output Capacitance	C <sub>oss</sub>		11		25	pF
Reverse Transfer Capacitance	C <sub>rss</sub>		2		5	
<b>SWITCHING</b>						
Turn-On Time	t <sub>ON</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 150 Ω I <sub>D</sub> = 0.2 A, V <sub>GEN</sub> = 10 V R <sub>G</sub> = 25 Ω (Switching time is essentially independent of operating temperature)	7		20	
Turn-Off Time	t <sub>OFF</sub>		7		20	ns

NOTES 1 T<sub>C</sub> = 25 °C unless otherwise noted

2 For design aid only, not subject to production testing

3 Pulse test, PW = 80 μs, duty cycle ≤ 1%

4 This parameter not registered with JEDEC

## N-Channel Enhancement-Mode MOSFET

### DESIGNED FOR:

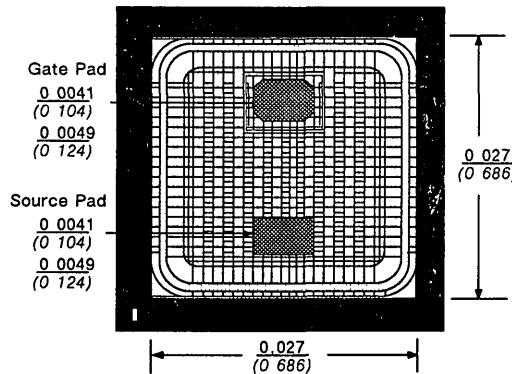
Switching  
Amplification

### FEATURES

- Low  $r_{DS(on)} < 10 \Omega$
- Low Cost
- Surface Mount Package SOT-23

TYPE	PACKAGE	DEVICE
Single	TO-206AC	• VN10LE
	TO-92	• 2N7000, 2N7008 VN0603L, VN0610LL VN2222LL
	TO-237	• VN2222LM
	SOT-23	• VN0603T, VN0605T 2N7002
Quad	14-Pin Plastic	• VQ1000J
	14-Pin Dual-In- Line	• VQ1000P
	Chip	• Available as above specifications

### GEOMETRY DIAGRAM



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