Powered-off Protection, 0.85 Ω, 1.8 V to 5.5 V, SPDT Analog Switch (2:1 Multiplexer)

DESCRIPTION

The DG2001E is a high performance single-pole, double-throw (SPDT) analog switch designed for 1.8 V to 5.5 V operation with a single power rail.

Fabricated with high density CMOS technology, the device achieves low on resistance of 0.85 Ω at a 5 V power supply, low power consumption, and fast switching speeds.

The DG2001E can handle both analog and digital signals and permits signals with amplitudes of up to V+ to be transmitted in either direction. Its control logic inputs can go over V+ up to 5.5 V. The control logic input high threshold is guaranteed as low as 1.8 V over the power supply range up to 5.5 V. It features break before make switching performance.

A powered-off protection circuit is built into the switch to prevent an abnormal current flow from COM pin to V+ during the power-down condition. Each output pin can withstand greater than 7 kV (human body model).

Operation temperature is specified from -40 °C to +85 °C. The DG2001E is available in TSOP-6 package.

FEATURES

- Low switch on-resistance (0.85 Ω)
- 1.8 V to 5.5 V single supply operation
- Isolation in powered-off mode
- Guaranteed 1.8 V logic high
- Control logic inputs can go over V+
- Low charge injection (8 pC)
- Break before make switching
- Latch-up performance exceeds 300 mA per JESD 78
- ESD tested
  - 7000 V human body model (JS-001)
  - 1000 V charge device model (JS-002)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
**HALOGEN FREE**

APPLICATIONS

- Consumer and computing
- Portable instrumentation
- Medical equipment
- Battery operated systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

TSOP-6

IN	1		6	NO (source₁)
V+	2		5	COM
GND	3		4	NC (source₂)

Top view

Device marking: H1

Pin 1 → H1XXX
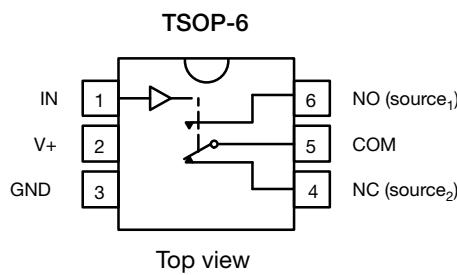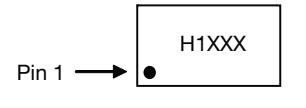
Device marking: H1XXX
XXX = date / lot traceability code

TRUTH TABLE

LOGIC	NC	NO
0	On	Off
1	Off	On

ORDERING INFORMATION

TEMP RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	TSOP-6	DG2001EDV-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		LIMIT	UNIT
V+, COM, NC, NO, IN reference to GND		-0.3 to 6	V
Continuous current (any terminal)		± 50	mA
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage temperature (D suffix)		-65 to +125	°C
Power dissipation (packages) [a]	TSOP-6 [b]	570	mW
ESD / HBM	JS-001	7000	V
ESD / CDM	JS-002	1000	
Latch up	Per JESD78 with 1.5 x voltage clamp	300	mA

Notes

a. All leads welded or soldered to PC board
b. Derate 7 mW/°C above 25 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 5 V)

| PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, ± 10 % V_{IN} = 0.8 V or 2.4 V [e]	TEMP. [a]	LIMITS -40 °C to +85 °C MIN. [b]	TYP. [c]	MAX. [b]	UNIT
Analog Switch							
Analog signal range [d]	V_{NO}, V_{NC} V_{COM}		Full	0	-	V+	V
On-resistance	R_{ON}	V+ = 4.5 V V_{COM} = 3 V, I_{NO}, I_{NC} = 10 mA	Room	-	0.85	1.6	Ω
			Full	-	-	1.8	
R_{ON} flatness [d]	R_{ON} Flatness	V+ = 4.5 V V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 10 mA	Room	-	0.3	-	
Switch off leakage current [g]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V / 4.5 V, V_{COM} = 4.5 V / 1 V	Room	-5	-	5	nA
			Full	-30	-	30	
	$I_{COM(off)}$		Room	-5	-	5	
			Full	-30	-	30	
Channel-on leakage current [g]	$I_{COM(on)}$	V+ = 5.5 V V_{NO}, V_{NC} = V_{COM} = 1 V / 4.5 V	Room	-5	-	5	
			Full	-30	-	30	
Power down leakage	$I_{COM(PD)}$	V+ = 0 V, V_{COM} = 4.5 V, V_{IN} = GND	Full [d]	-	-	1	µA
Digital Control							
Input high voltage	V_{INH}		Full	2.4	-	-	V
Input low voltage	V_{INL}		Full	-	-	0.8	
Input capacitance	C_{IN}		Full	-	3	-	pF
Input current	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	-1	-	1	µA
Dynamic Characteristics							
Turn-on time	t_{ON}	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF	Room	-	15	32	ns
			Full	-	-	35	
Turn-off time	t_{OFF}		Room	-	6	26	
			Full	-	-	31	
Break-before-make time	t_d		Room	1	4	-	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	-	8	-	pC
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-63	-	dB
Crosstalk [d]	X_{TALK}		Room	-	-63	-	
Source-off capacitance [d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 V or V+, f = 1 MHz	Room	-	16	-	pF
Channel-on capacitance [d]	C_{ON}		Room	-	53	-	
Power Supply							
Power supply current	I+	V_{IN} = 0 V or V+	Full	-	0.0003	1	µA

SPECIFICATIONS (V+ = 3 V)

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, ± 10 % V_{IN} = 0.4 V or 2 V [e]	TEMP. [a]	LIMITS -40 °C to +85 °C MIN. [b]	TYP. [c]	MAX. [b]	UNIT
Analog Switch							
Analog signal range [d]	V_{NO}, V_{NC}, V_{COM}		Full	0	-	V+	V
On-resistance	R_{ON}	V+ = 2.7 V V_{COM} = 1.5 V, I_{NO}, I_{NC} = 10 mA	Room	-	1.6	2.2	Ω
			Full	-	-	2.6	
R_{ON} flatness [d]	R_{ON} Flatness	V+ = 2.7 V V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 10 mA	Room	-	0.6	-	
Switch off leakage current [g]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 1 V / 3 V, V_{COM} = 3 V / 1 V	Room	-5	-	5	nA
			Full	-15	-	15	
	$I_{COM(off)}$		Room	-5	-	5	
			Full	-15	-	15	
Channel-on leakage current [g]	$I_{COM(on)}$	V+ = 3.3 V V_{NO}, V_{NC} = V_{COM} = 1 V / 3 V	Room	-5	-	5	
			Full	-15	-	15	
Digital Control							
Input high voltage	V_{INH}		Full	2	-	-	V
Input low voltage	V_{INL}		Full	-	-	0.4	
Input capacitance	C_{IN}		Full	-	-	-	pF
Input current	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	-1	-	1	µA
Dynamic Characteristics							
Turn-on time	t_{ON}	V_{NO} or V_{NC} = 2 V, R_L = 300 Ω, C_L = 35 pF	Room	-	21	42	ns
			Full	-	-	47	
Turn-off time	t_{OFF}		Room	-	9	32	
			Full	-	-	35	
Break-before-make time	t_d		Room	1	7	-	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	-	6	-	pC
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-63	-	dB
Crosstalk [d]	X_{TALK}		Room	-	-63	-	
N_O, N_C off capacitance [d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 V or V+, f = 1 MHz	Room	-	16	-	pF
Channel-on capacitance [d]	C_{ON}		Room	-	54	-	
Power Supply							
Power supply current	I+	V_{IN} = 0 V or V+	Full	-	0.00002	1	µA

SPECIFICATIONS (V+ = 2 V)

| PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 2 V, ± 10 % V_{IN} = 0.4 V or 1.6 V [e]	TEMP. [a]	LIMITS -40 °C to +85 °C MIN. [b]	TYP. [c]	MAX. [b]	UNIT
Analog Switch							
Analog signal range [d]	V_{NO}, V_{NC} V_{COM}		Full	0	-	V+	V
On-resistance	R_{ON}	V+ = 1.8 V V_{COM} = 1 V, I_{NO}, I_{NC} = 10 mA	Room	-	6	8	Ω
			Full	-	-	10	
R_{ON} flatness [d]	R_{ON} Flatness	V+ = 1.8 V V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 10 mA	Room	-	6	-	
Switch off leakage current [g]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 2.2 V V_{NO}, V_{NC} = 0.5 V / 1.5 V, V_{COM} = 1.5 V / 0.5 V	Room	-0.5	-	0.5	nA
			Full	-5	-	5	
	$I_{COM(off)}$		Room	-0.5	-	0.5	
			Full	-5	-	5	
Channel-on leakage current [g]	$I_{COM(on)}$	V+ = 2.2 V V_{NO}, V_{NC} = V_{COM} = 0.5 V / 1.5 V	Room	-0.5	-	0.5	
			Full	-5	-	5	
Digital Control							
Input high voltage	V_{INH}		Full	1.6	-	-	V
Input low voltage	V_{INL}		Full	-	-	0.4	
Input capacitance	C_{IN}		Full	-	3	-	pF
Input current	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	-1	-	1	µA
Dynamic Characteristics							
Turn-on time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 300 Ω, C_L = 35 pF	Room	-	36	51	ns
			Full	-	-	62	
Turn-off time	t_{OFF}		Room	-	16	40	
			Full	-	-	43	
Break-before-make time	t_d		Room	1	16	-	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	-	21	-	pC
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-63	-	dB
Crosstalk [d]	X_{TALK}		Room	-	-63	-	
N_O, N_C off capacitance [d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 V or V+, f = 1 MHz	Room	-	16	-	pF
Channel-on capacitance [d]	C_{ON}		Room	-	52	-	
Power Supply							
Power supply current	I+	V_{IN} = 0 V or V+	Full	-	0.00001	1	µA

Notes

a. Room = 25 °C, full = as determined by the operating suffix
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
c. Typical values are for design aid only, not guaranteed nor subject to production testing
d. Guarantee by design, nor subjected to production test
e. V_{IN} = input voltage to perform proper function
f. Guaranteed by 5 V leakage testing, not production tested

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)
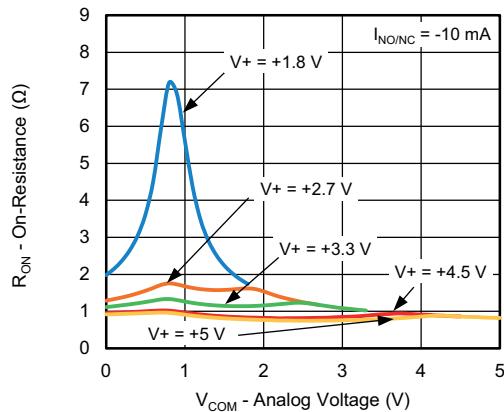
R$_{DS(on)}$ vs. V$_{COM}$ and Supply Voltage
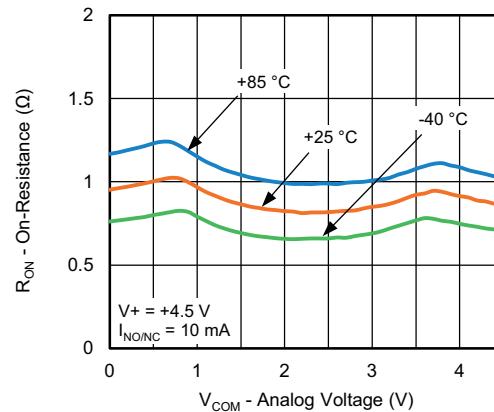
R$_{DS(on)}$ vs. V$_{COM}$ and Temperature
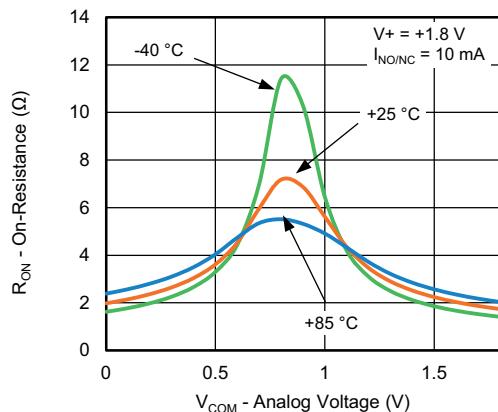
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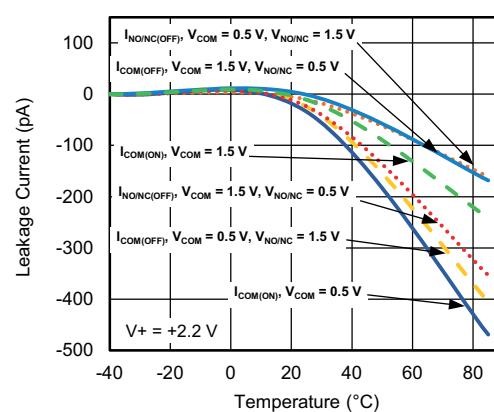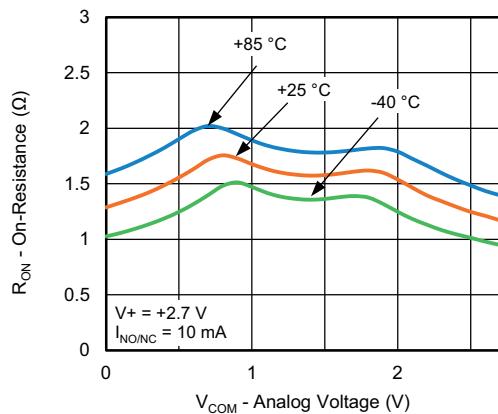

Leakage Current vs. Temperature

R$_{DS(on)}$ vs. V$_{COM}$ and Temperature


Leakage Current vs. Temperature

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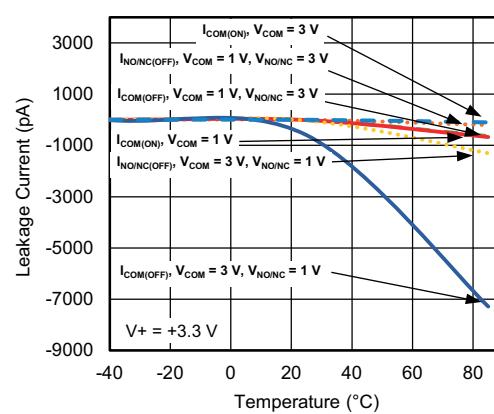
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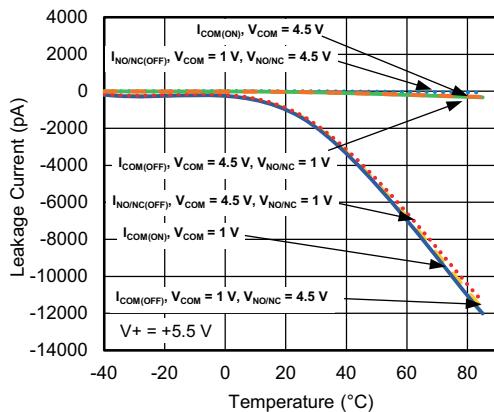
Leakage Current vs. Temperature
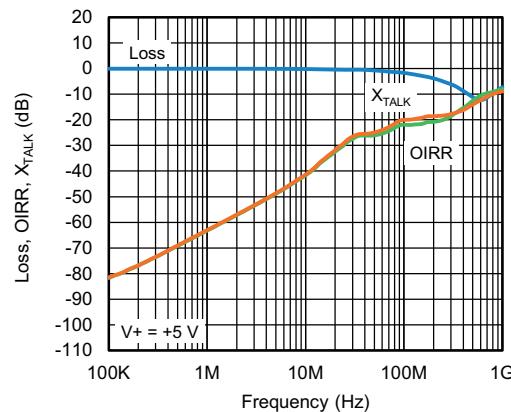
Insertion Loss, Off-Isolation Crosstalk vs. Frequency
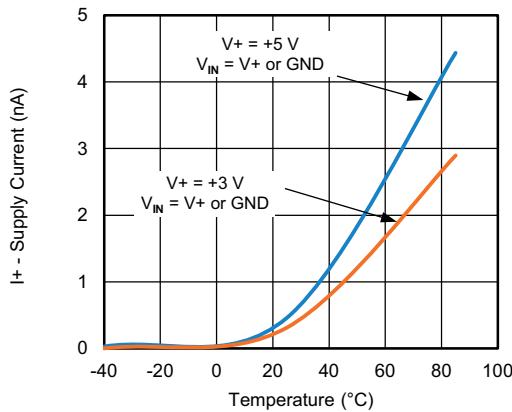
Supply Current vs. Temperature
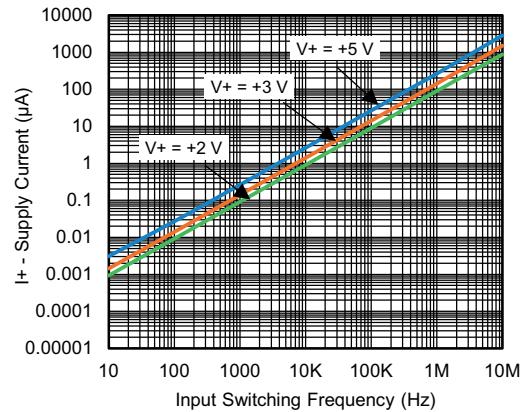
Supply Current vs. Input Switching Frequency
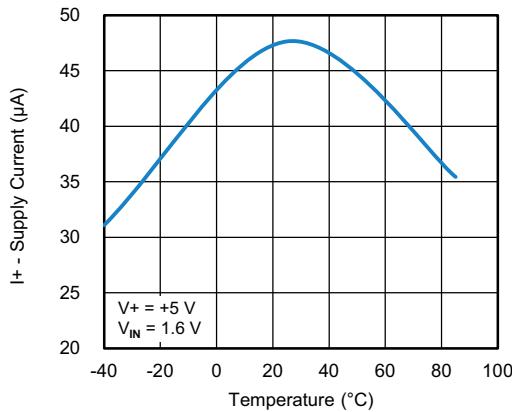

Supply Current vs. Temperature
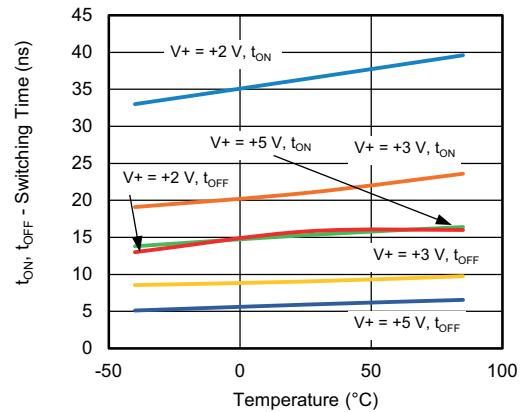

Switching Time vs. Temperature and Supply Voltage

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## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)
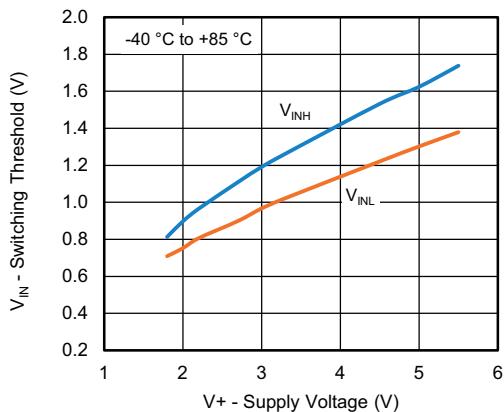
**Switching Threshold vs. Supply Voltage**
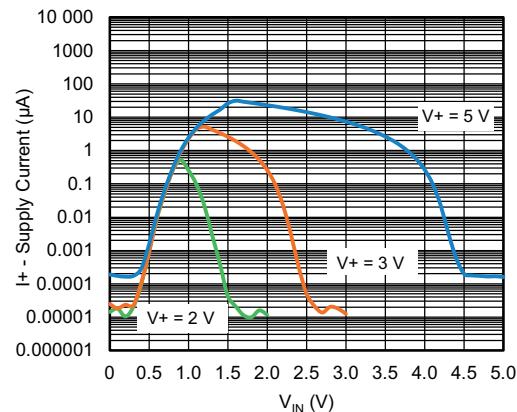
Supply Current vs. Enable Input Voltage
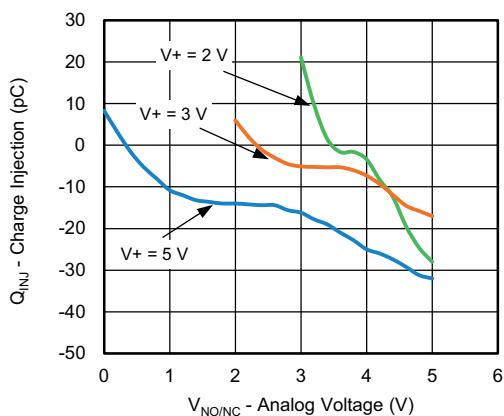

Charge Injection vs. Analog Voltage
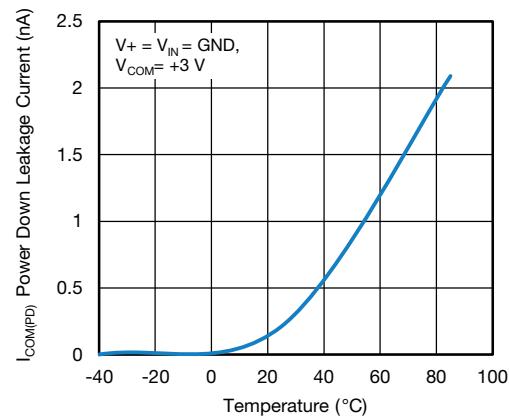

Power Down Leakage Current vs. Temperature
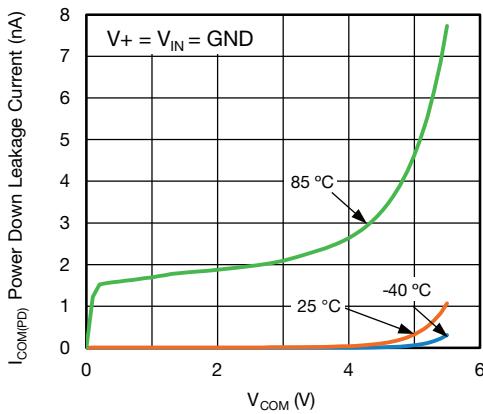

Power Down Leakage Current vs. V$_{COM}$

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TEST CIRCUITS

V+

V+

Switch
Input — NO or NC ⌐ COM — Switch Output — V_{OUT}

IN

Logic
Input

GND

0 V

R_L 300 Ω C_L 35 pF
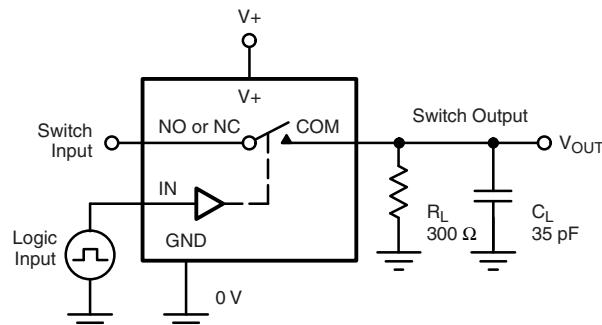
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Fig. 1 - Switching Time

+ 3 V

Logic
Input   50 % $t_r < 20$ ns
                      $t_f < 20$ ns
0 V

Switch
Output   0.9 x V_{OUT}

0 V

t_{ON} t_{OFF}
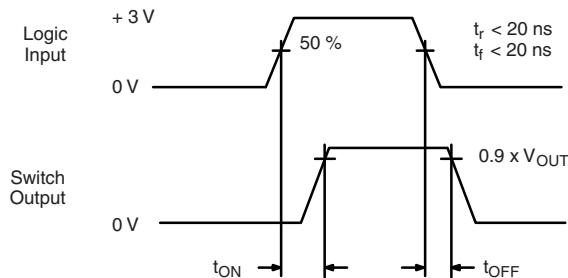
Logic "1" = Switch On
Logic input waveforms inverted for switches that have
the opposite logic sense.

V+

V+

V_{NO} — NO ⌐ COM — V_O

V_{NC} — NC

IN

GND

R_L 300 Ω C_L 35 pF
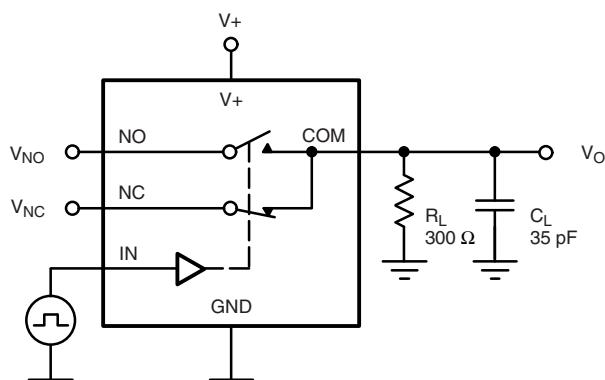
C_L (includes fixture and stray capacitance)
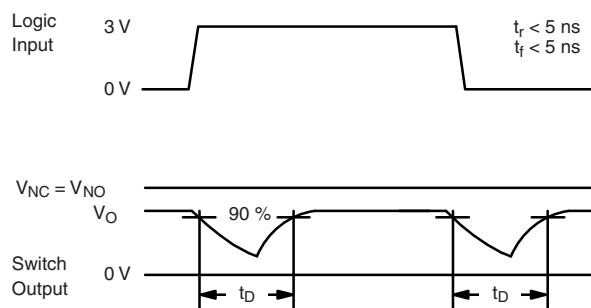
Fig. 2 - Break-Before-Make Interval

Logic
Input   3 V $t_r < 5$ ns
                               $t_f < 5$ ns
0 V

$V_{NC} = V_{NO}$
V_O 90 %
Switch
Output   0 V

t_D t_D

V+

V+

R_{gen} NC or NO ⌐ COM — V_{OUT}

V_{gen} +   IN

3 V

GND C_L

Fig. 3 - Charge Injection

V_{OUT} ΔV_{OUT}

IN   On   Off   On

$Q = \Delta V_{OUT} \times C_L$
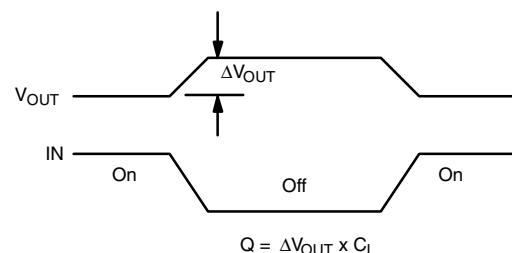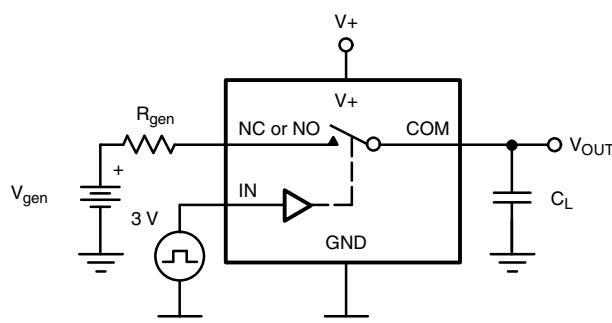
IN depends on switch configuration: input polarity
determined by sense of switch.

TEST CIRCUITS

Fig. 4 - Off-Isolation

$$\text{Off Isolation} = 20 \log \frac{V_{NC/NO}}{V_{COM}}$$
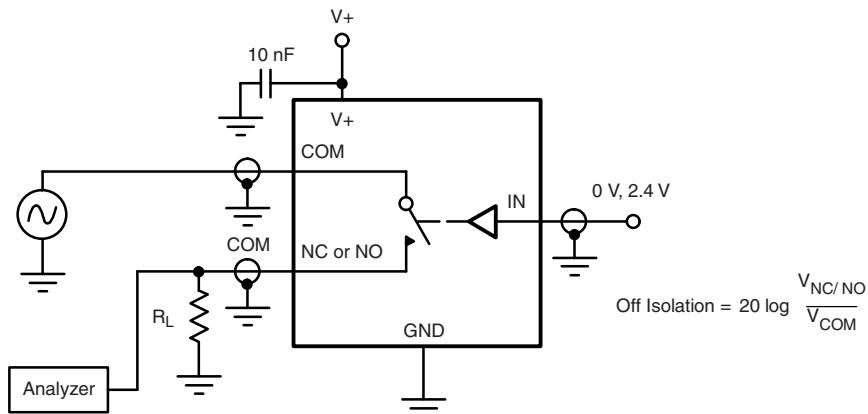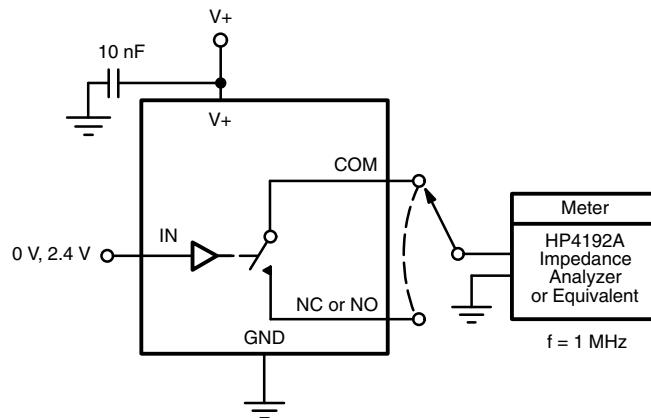
**Fig. 5 - Channel Off/On Capacitance**

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For technical questions, contact: analogswitchtechsupport@vishay.com

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TSOP: 5/6–LEAD
JEDEC Part Number: MO-193C
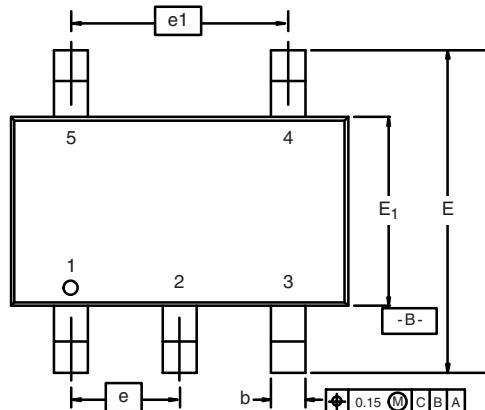
5-LEAD TSOP
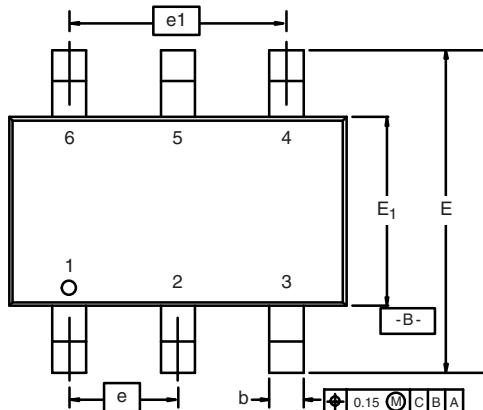
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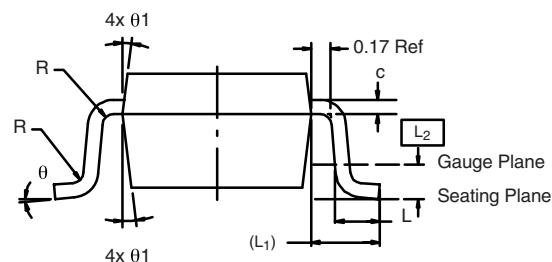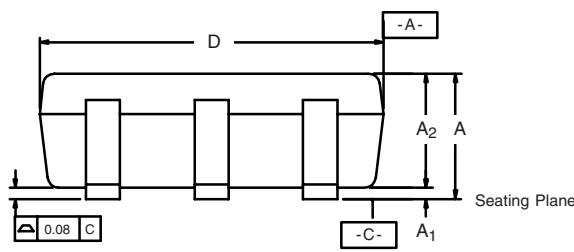
Dim	MILLIMETERS			INCHES		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.91	-	1.10	0.036	-	0.043
A₁	0.01	-	0.10	0.0004	-	0.004
A₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L₁	0.60 Ref			0.024 Ref		
L₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

RECOMMENDED MINIMUM PADS FOR TSOP-6

Recommended Minimum Pads
Dimensions in Inches/(mm)
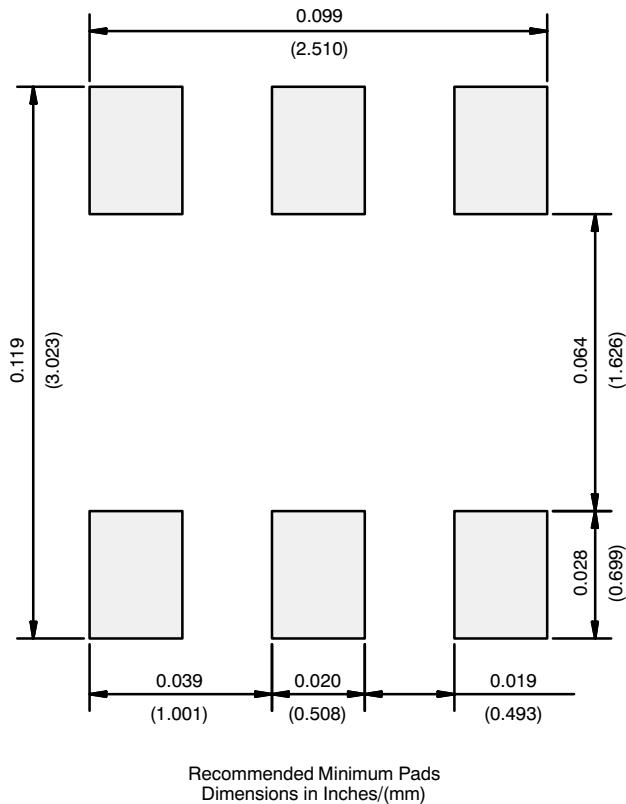
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