# Monolithic Dual SPST CMOS Analog Switch

## DESCRIPTION

The DG200B is a dual, single-pole, single-throw analog switch designed to provide general purpose switching of analog signals. This device is ideally suited for designs requiring a wide analog voltage range coupled with low on-resistance.

The DG200B is designed on Vishay Siliconix' improved PLUS-40 CMOS process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. In the on condition, this bi-directional switch introduces no offset voltage of its own.

## FEATURES

- ± 15 V Input Signal Range
- 44 V Maximum Supply Ranges
- On-Resistance: 45 Ω
- TTL and CMOS Compatibility

Pb-free Available

**RoHS*** COMPLIANT

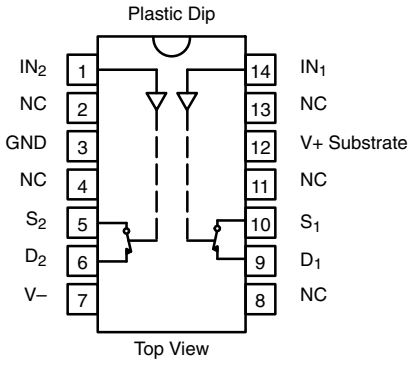
## BENEFITS

- Wide Dynamic Range
- Simple Interfacing
- Reduced External Component Count

## APPLICATIONS

- Servo Control Switching
- Programmable Gain Amplifiers
- Audio Switching
- Programmable Filters

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION




| TRUTH TABLE | |
|---|---|
| **Logic** | **Switch** |
| 0 | ON |
| 1 | OFF |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

| ORDERING INFORMATION | | |
|---|---|---|
| **Temp Range** | **Package** | **Part Number** |
| - 40 to 85 °C | 14-Pin Plastic DIP | DG200BDJ<br>DG200BDJ-E3 |

* Pb containing terminations are not RoHS compliant, exemptions may apply

| **ABSOLUTE MAXIMUM RATINGS** $T_A$ = 25°C, unless otherwise noted | | | |
|---|---|---|---|
| **Parameter** | | **Limit** | **Unit** |
| V+ to V- | | 44 | V |
| GND to V- | | 25 | |
| Digital Inputs[a], $V_S$, $V_D$ | | (V-) - 2 V to (V+) + 2 V<br>or 30 mA, whichever occurs first | |
| Current (Any Terminal) Continuous | | 30 | mA |
| Current S or D | (Pulsed at 1 ms, 10 % Duty Cycle Max) | 100 | |
| Storage Temperature | | - 65 to 150 | °C |
| Power Dissipation (Package)[b] | 14-Pin Plastic DIP[c] | 470 | mW |

Notes:
a. Signals on $S_X$, $D_X$, or $IN_X$ exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 25 °C.

## SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

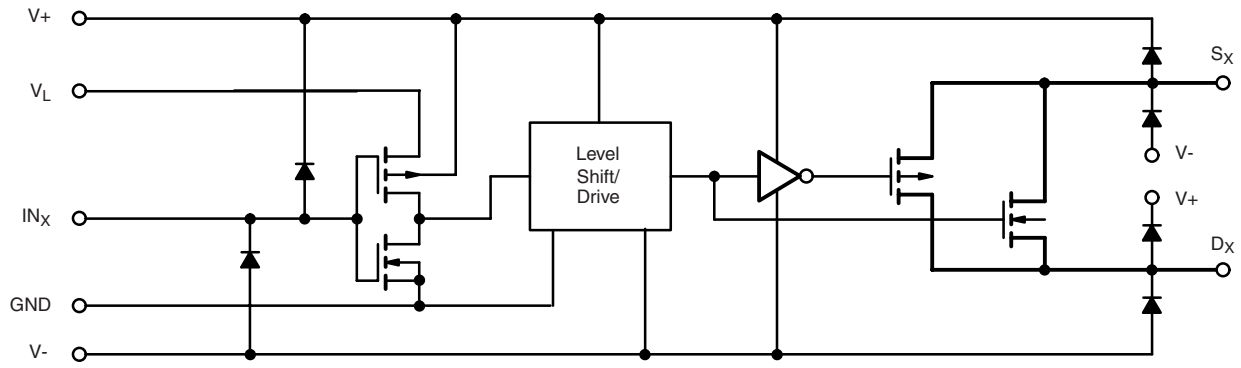



**Figure 1.**

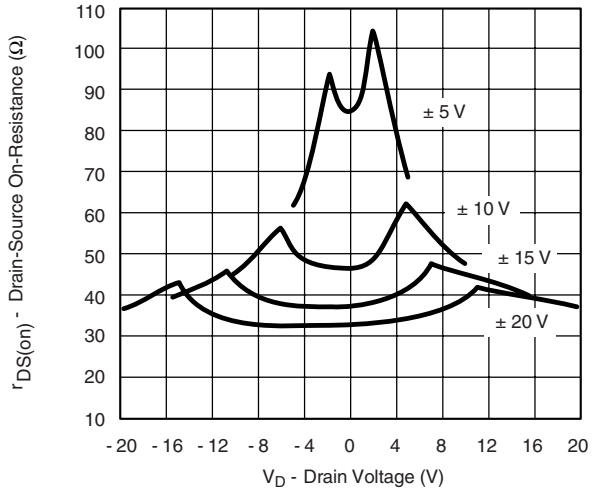
## SPECIFICATIONS[a]

| Parameter | Symbol | Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V $V_{IN}$ = 2.4 V, 0.8 V[f] | Temp[b] | Limits - 40 to 85 °C Min[c] | Typ[d] | Max[c] | Unit |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog Signal Range[e] | $V_{ANALOG}$ | | Full | - 15 | | 15 | V |
| Drain-Source On-Resistance | $r_{DS(on)}$ | $V_D$ = ± 10 V, $I_S$ = - 1 mA | Room<br>Full | | 45 | 85<br>100 | Ω |
| Source Off Leakage Current | $I_{S(off)}$ | $V_S$ = ± 14 V, $V_D$ = ∓ 14 V | Room<br>Full | - 2<br>- 100 | ± 0.01 | 2<br>100 | nA |
| Drain Off Leakage Current | $I_{D(off)}$ | $V_D$ = ± 14 V, $V_S$ = ∓ 14 V | Room<br>Full | - 2<br>- 100 | ± 0.01 | 2<br>100 | |
| Channel On Leakage Current[f] | $I_{D(on)}$ | $V_S$ = $V_D$ = ± 14 V | Room<br>Full | - 2<br>- 200 | ± 0.1 | 2<br>200 | |
| **Digital Control** | | | | | | | |
| Input Current with Input Voltage High | $I_{INH}$ | $V_{IN}$ = 2.4 V | Room<br>Full | - 0.5<br>- 1 | 0.0009 | | µA |
| | | $V_{IN}$ = 15 V | Room<br>Full | | 0.005 | 0.5<br>1 | |
| Input Current with Input Voltage Low | $I_{INL}$ | $V_{IN}$ = 0 V | Room<br>Full | - 0.5<br>- 1 | - 0.0015 | | |
| **Dynamic Characteristics** | | | | | | | |
| Turn-On Time | $t_{ON}$ | See Switching Time Test Circuit | Room | | 300 | 1000 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room | | 200 | 425 | |
| Charge Injection | Q | $C_L$ = 1000 pF, $R_g$ = 0 Ω, $V_g$ = 0 V | Room | | 1 | | pC |
| Source Off Capacitance | $C_{S(off)}$ | f = 140 kHz, $V_{IN}$ = 5 V, $V_S$ = 0 V | Room | | 5 | | pF |
| Drain Off Capacitance | $C_{D(off)}$ | f = 140 kHz, $V_{IN}$ = 5 V, $V_D$ = 0 V | Room | | 5 | | |
| Channel-On Capacitance | $C_{D(on)}$+ $C_{S(on)}$ | $V_S$ = $V_D$ = 0 V, $V_{IN}$ = 0 V | Room | | 16 | | |
| Off Isolation | OIRR | $V_{IN}$ = 5 V, $R_L$ = 75 Ω, $V_S$ = 2 V, f = 1 MHz | Room | | 90 | | dB |
| Crosstalk (Channel-to-Channel) | $X_{TALK}$ | | Room | | 95 | | |
| **Power Supplies** | | | | | | | |
| Positive Supply Current | I+ | Both Channels On or Off, $V_{IN}$ = 0 V and 5.0 V | Room | | | 50 | µA |
| Negative Supply Current | I- | | Room | - 10 | | | |

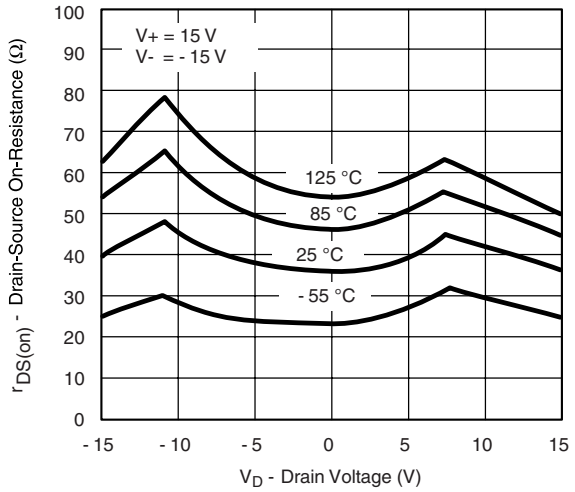
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. $V_{IN}$ = input voltage to perform proper function.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

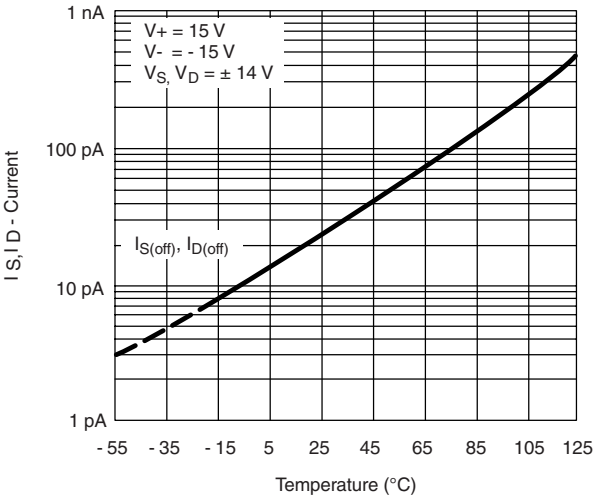
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



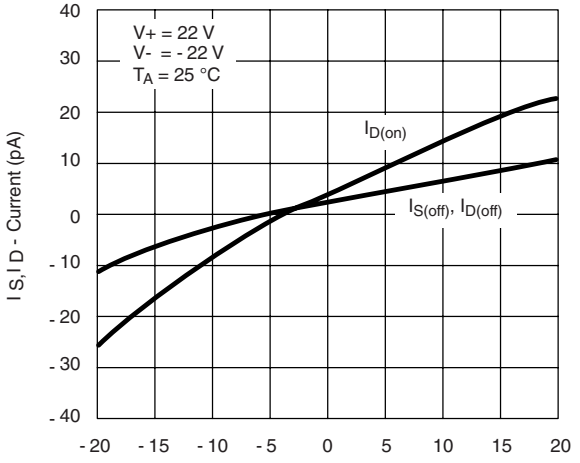

**$r_{DS(on)}$ vs. $V_D$ and Power Supply Voltages**




**$r_{DS(on)}$ vs. $V_D$ and Temperature**




**Leakage Current vs. Temperature**




**Leakage Currents vs. Analog Voltage**

## TEST CIRCUITS

$V_O$ is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

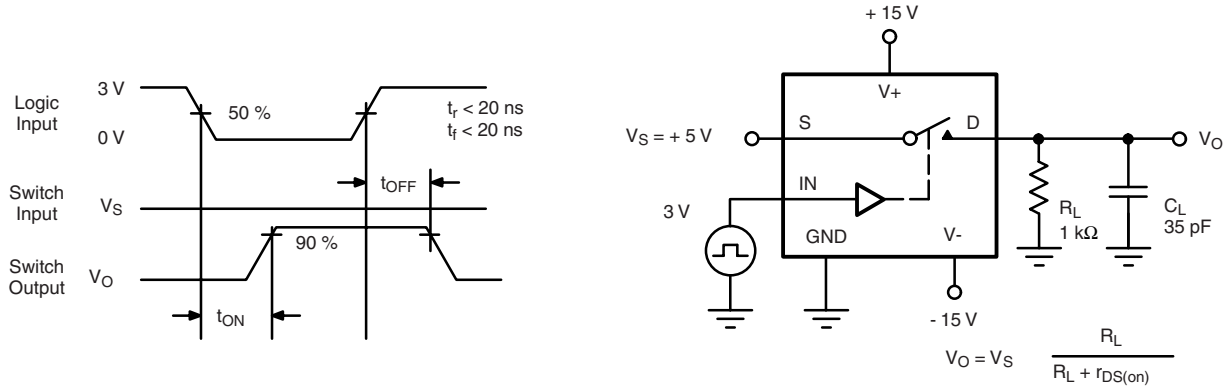



**Figure 2. Switching Time**

## TEST CIRCUITS

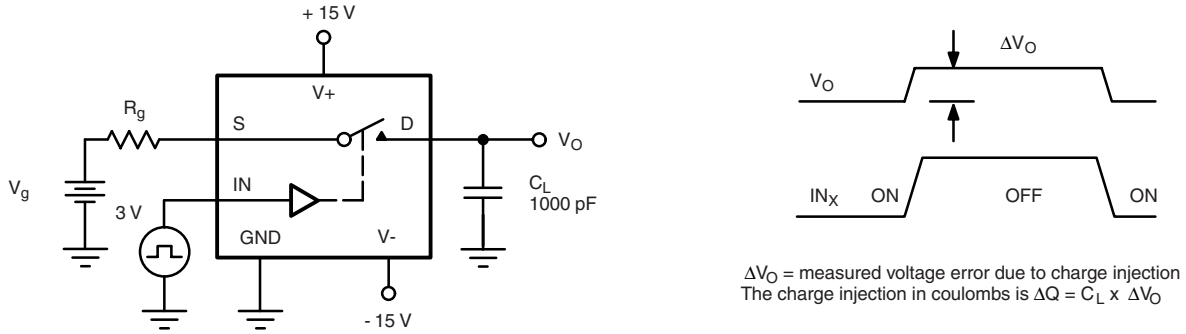



**Figure 3. Charge Injection**

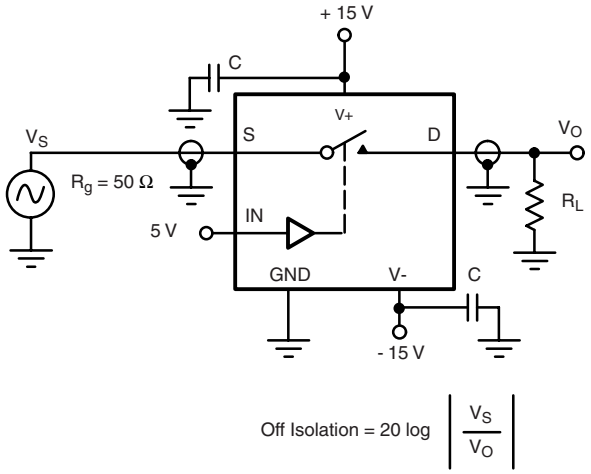



**Figure 4. Off Isolation**

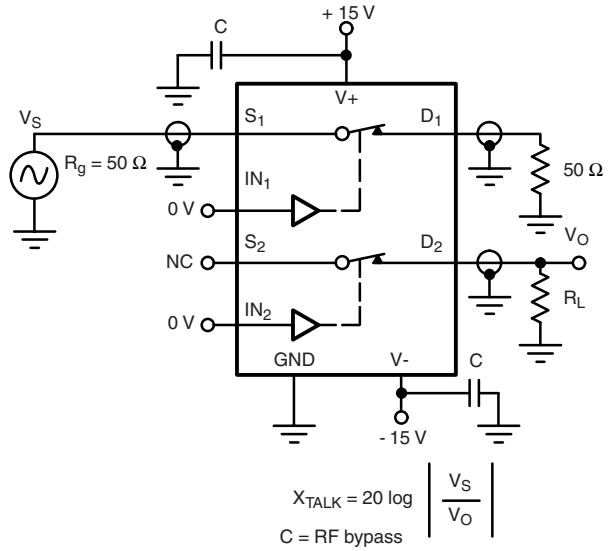



**Figure 5. Channel-to-Channel Crosstalk**

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